Operation of time-to-voltage converter*

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1 Introduction

Measurement of time interval between two events (represented by the electronic signal(s) generated by them) is one of the most important tasks of any data acquisition system, be it in a small or large scale physics experiment. This information is useful both during the on-line as well as the off-line analysis of a particular physics phenomenon creating that signature and forming the trigger. Examples are in determining the angle of incidence of an air shower generated by High Energy Cosmic Rays, in identifying slowly moving particles such as magnetic monopoles in underground experiments, in filtering the Cosmic Ray background, stray triggers due to surrounding radioactivity etc. in accelerator based physics experiments.

2 Principle of a time-to-voltage converter

A Time-to-Voltage Converter (TVC) is one of the simplest timing instruments to setup and operate. The input signals are provided direct from discriminators with no critical adjustments of amplitude or width being required. In the actual commercial Time-to-Digital Converters (TDCs), the operation is accomplished in two stages. A capacitor is charged up by a constant current source initiated by the START pulse and terminated by the STOP pulse. The total charge delivered to the capacitor is then an analog representation of the time interval to be measured. An analog-to-digital conversion is then performed on the voltage held

*Lecture notes for the first SERC School on Experimental High Energy Physics held at T.I.F.R, Bombay during January 1995 by the capacitor. During this stage, the charge is removed from the capacitor at a constant rate during which time pulses from an oscillator are gated into a scaler. The final count is thus proportional to the time interval measured.

The first stage of the TDC is essentially a TVC. By fabricating this simple circuit separately, one can eliminate the need for a separate TDC. Since even a modest experiment makes use of an Analog-to-Digital Converter (ADC) module, the TVC then can also be read by the same, thus obtaining both the ionisation as well as the timing information through the ADC unit channels.

3 Circuit operation

A simplified version of the design which is being employed in the D0 Experiment at Fermilab, USA, is used to demonstrate the operating principle of a TVC circuit. Though in actual data acquisition systems, the START and STOP pulses to the TVC are generated by different sources, in case of this model circuit, they are manipulated from a single pulse given from an external pulse generator. In fact, a small offset in the measurement of time interval also had to be accommodated because of this simplification of the circuit.

A true (positive logic) TTL pulse is fed to the flip-flop (74S74) from the pulse generator. Where as, it is given directly to the CLEAR ($START$) input, the same is delayed by about 25 nS (using two stages of 7404) and given to the CLOCK ($START$) input of the flip-flop. The Q output of the flip-flop is normally LOW when there is no input pulse, thus keeping the transistor Q_2 ON. The current supplied by the constant current generator (formed by transistor Q_1) is thus continuously drained by Q_2 during this period. At this time, transistor Q_3 is OFF because the $\bar{\mathrm{Q}}$ ouput of the flip-flop is high. It may be noted that the transistors Q_2 and Q_3 are configured as simple switches.

When a pulse is applied to the circuit, $\bar{\mathrm{Q}}$ of the flip-flop turns LOW at the leading edge of this pulse, thus making the transistor Q_3 ON, which then starts charging the capacitor C_1. Q output of the flip-flop again goes LOW when the input pulse ends. Thus, essentially the capacitor charged by the constant current supplied by Q_1 for the duration of the input pulse. It is easy to see that the voltage built-up across the capacitor is proportinal to the time for which it is charged.

If a CONSTANT current (i, Amperes) is supplied to a capacitor of capacitance (C, Farads) for a duration of time (t, Seconds), then the total charge (q, Coulombs) accumulated in the capacitor is given by,

$$q = C * V$$

or

$$i * t = C * V$$

Where, V is the voltage across its plates.

So,

$$V = \frac{i * t}{C}$$

or

For a given capacitor and current, we have

$$V \propto t$$

The voltage held across the capacitor C_1 is then buffered by a driver U_1 and held by the sample-hold amplifier (voltage gain of 2) formed by U_2 along with capacitor C_2.

The constant current supplied by Q_1 is given by the following relation.

$$i = \frac{VCC_e - V_f - REFERENCE}{R_e}$$

Where,
VCC_e is the supply voltage to the emitter,
V_f is the emitter to base forward bias drop (0.7V for the transistor used)
R_e is the emitter resistance.

REFERENCE may be adjusted using the trim pot provided for this purpose. It is kept at 10.0 volts at present. The current for this REFERENCE value then is about 870 micro amperes. It may also be seen that the charging current determines the dynamic range of the converter.

In parallel with C_1 is the reset switch SW to discharge the same between two measurements.

4 Studies and measurements

1. Understand the operating principle and the component layout of the circuit.
2. Connect the TTL output (positive logic) of the pulse generator to the circuit input. Also connect $\overline{TTL}$ (complimentary logic) output of the same to an oscilloscope (Channel 1) for input pulse width measurements.
3. Connect the circuit output to the oscilloscope (Channel 2).
4. Keep the GENERATOR MODE of the pulse generator in CONTinuous mode and adjust the pulse width to the desired value (about 200 nS to start with), using PULSE WIDTH and its vernier control knobs.
5. Turn the GENERATOR MODE to TRIGger mode.
6. Discharge any residual charge held by the capacitor by pressing the RESET push button switch and apply a single pulse using the MANUAL TRIGGER toggle switch.
7. Measure the circuit output voltage on the oscilloscope.
8. Repeat steps 6 & 7 a few times for each measurement for obtaining a better average of the voltage readings. This is particularly relevant due to stray (dis)charging of the capacitor through even high resistance paths of the circuit.
9. Increase the input pulse width by steps of 200-300 nS and repeat the steps 4-8 till the saturation (which is due to Operation Amplifier drivers following the capacitor).
10. Plot the readings (Pulse width Versus Voltage output) and observe the linearity of the circuit.