

Signal processing electronics

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Plan of the course

- Concepts from signals to DAQ systems
- Signal transmission, Amplifiers, Shaping amplifiers, Discriminators and Coincidence circuits
- Analog-to-Digital and Time-to-Digital Converters
- Examples from CMS, ALICE and INO experiments

Part-I

Wednesday, February 18, 2009

Acknowledgements & References: G.Hall, ALICE collaboration,
CMS collaboration, INO collaboration, ATLAS collaboration,
P.W.Nicholson, G.G.Eichholz & J.W.Poston, E.Fenyves & O.Haiman

Signals

- Signal

generalised name for input into instrument system

- Might seem logical to consider signals before sensors but can now see wide range of signal types are possible
 - depend on sensor*
 - depend on any further transformation - eg light to electrical*

- Most common types of signal

short, random pulses, usually current, amplitude carries information
typical of radiation sensors

trains of pulses, often current, usually binary
typical of communication systems

continuous, usually slowly varying, quantity - eg. current or voltage

slow - typical of monitoring instruments

fast - eg cable TV, radio

- terms like "slow", "fast" are very relative!

Signal formation

- **Issues in practical applications**

duration

radiation: depends on transit time through sensor and details of charge induction process in external circuit

linearity

most radiation sensors characterised, or chosen for linearity for commercial components can expect non-linearity, offset and possible saturation

reproducibility

eg. many signals are temperature dependent in magnitude - mobility of charges other effects easily possible

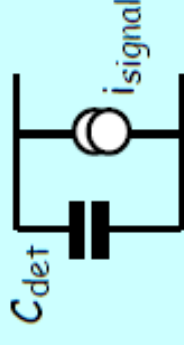
ageing

*sensor signals can change with time for many reasons
natural degradation of sensor, variation in operating conditions, radiation damage,...*

- **all these effects mean one should always be checking or calibrating measurements intended for accuracy as best one can**

Sensor equivalent circuits

- Many of the sensors considered so far can be modelled as



current source + associated capacitance

typical values $\sim$ few pF

but can range from

$\sim 100\text{fF}$ semiconductor pixel

$\sim 10\text{-}20\text{pF}$ gas or Si microstrip, PM anode

$\sim 100\text{pF}$ large area diode

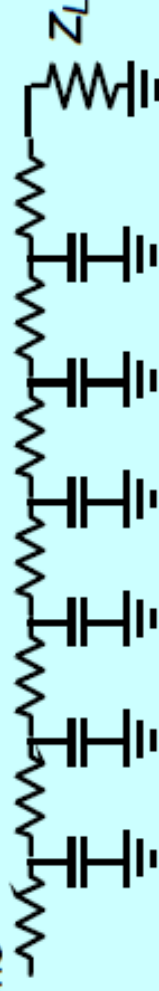
$\sim \mu\text{F}$ wire chamber

usually there is some resistance associated with the sensor, eg leads or metallisation but this has little effect on signal formation or amplification

- Notable exception: microstrips - gas or silicon

the capacitance is distributed, along with the strip resistance

forms a dissipative transmission line



Dynamic range

- In most systems there will be a smallest measurable signal
 - If there is noise present, it is most likely to be related to the smallest signal distinguishable from noise.
 - For example: 3 x rms noise? 5 x rms noise?
 - Or quantisation unit in measurement
- and a largest measurable signal
 - most likely set by apparatus or instrument, eg. saturation
- Dynamic range = ratio of largest to smallest signal often expressed in dB or bits
 - Eg. 8 bits = dynamic range is 256_{10}
 - = 48dB (if signal is voltage)
 - decibels (dB)
 - Signal magnitudes cover wide range so frequently prefer logarithmic scale
 - Number of dB = $10 \log_{10}(P_2/P_1)$
 - Often measuring voltages in system: dB = $20 \log_{10}(V_2/V_1)$
 - Not an absolute unit and sometimes encounter variants
 - dBm: dB with $P_{in} = 1mW$

Precision

- Many measurements involve detection of particle or radiation quantum (photon)
 - Simple presence or absence sometimes sufficient = binary (0 or 1)
 - Other measurements are of energy
- Why do we need such observations?
 - Primary measurement may be energy
 - Eg. medical imaging using gammas or high energy x-rays, astro-particle physics
 - Extra information to improve data quality
 - Removes experimental background, eg. Compton scattered photons mistaken for real signal
 - Optical communications - pressure to increase “bandwidth” – eg. number of telephone calls carried per optical fibre
 - Wavelength division multiplexing - several “colours” or wavelengths in same fibre simultaneously
- What is ultimate limit to precision?

ALICE experiment

- *The ALICE Collaboration is building a dedicated heavy-ion detector to exploit the unique physics potential of nucleus-nucleus interactions at LHC energies. Our aim is to study the physics of strongly interacting matter at extreme energy densities, where the formation of a new phase of matter, the quark-gluon plasma, is expected.*
- *The existence of such a phase and its properties are key issues in QCD for the understanding of confinement and of chiral-symmetry restoration.*
- *For this purpose, we intend to carry out a comprehensive study of the hadrons, electrons, muons and photons produced in the collision of heavy nuclei.*
- *Alice will also study proton-proton collisions both as a comparison with lead-lead collisions and in physics areas where Alice is competitive with other LHC experiments*

Detectors of the ALICE experiment

- The Overview

- First one needs to know the initial conditions, namely how powerful the collision was: this is done by measuring the remnants of the colliding nuclei in detectors made of high density materials located about 100 meters on both sides of ALICE (the [ZDC](#)'s) and by measuring with the [FMD](#), [V0](#) and [To](#) the number of particles produced in the collision and their spatial distribution. [To](#) also measures with high precision the time when the event takes place.

- Tracking particles

- An ensemble of cylindrical detectors (from inside out: [ITS Pixels](#) (ITS Drift, ITS Strips, [TPC](#), [TRD](#)) measures at many points (over 100 just the TPC) the passage of each particle carrying an electric charge, so that its trajectory is precisely known. The ALICE tracking detectors are embedded in a magnetic field (produced by the huge red magnet !) bending the trajectories of the particles: from the curvature of the tracks one can find their momentum. The ITS is so precise that particles which are generated by the decay of other particles with a very short life time can be identified by seeing that they do not originate from the point where the interaction has taken place (the “vertex” of the event) but rather from a point at a distance of as small as a tenth of a millimeter.

- The particles' Identity

- ALICE also wants to know the identity of each particle, whether it is an electron, or a proton, a kaon or a pion. In addition to the information given by ITS and TPC, more specialized detectors are needed: the [IDF](#) measures, with a precision better than a tenth of a billionth of a second, the time that each particle takes to travel from the vertex to reach it, so that one can measure its speed, while the [HMPID](#) measures the faint light patterns generated by fast particles and the TRD measures the special radiation very fast particles emit when crossing different materials, thus allowing to identify electrons. Muons are measured by exploiting the fact that they penetrate matter more easily than most other particles: in the forward region a very thick and complex absorber stops all other particles and muons are measured by a dedicated set of detectors: [the muon spectrometer](#).

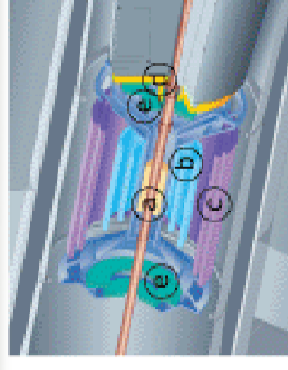
- Catching Photons

- The photons (particles of light), like the light emitted from a hot object, tell us about the temperature of the system. To measure them, special detectors are necessary: the crystals of the [PHOS](#), which are as dense as lead and as transparent as glass, will measure them with fantastic precision in a limited region, while the PMD and in particular the EMCAL will measure them over a very wide area. The EMCAL will also measure groups of close particles (called “jets”) which have a memory of the early phases of the event.

ALICE experiment

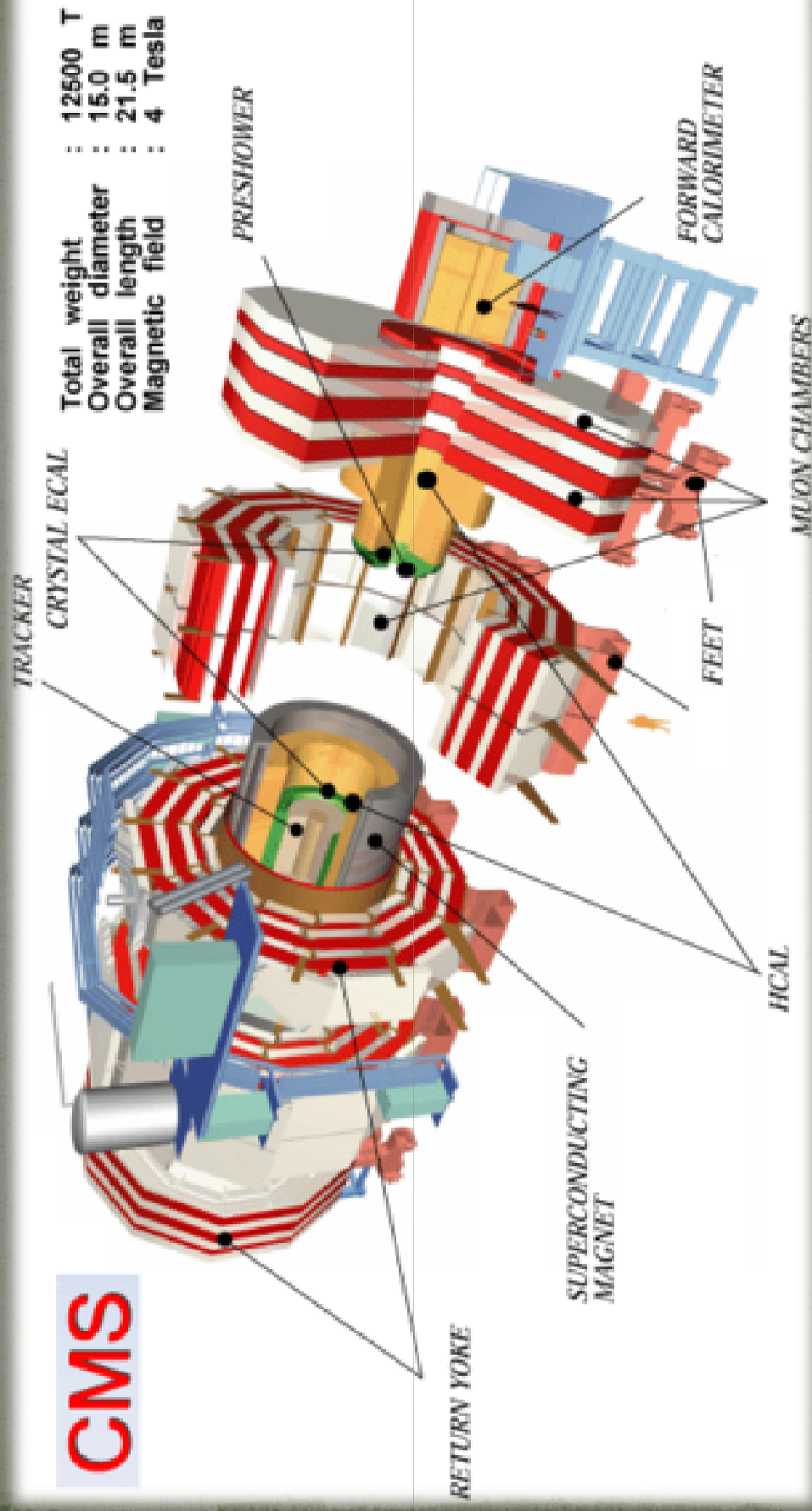
THE ALICE DETECTOR

1. ITS
2. FMD , T0, V0
3. TPC
4. TRD
5. TOF
6. HMPID
7. EMCAL
8. PHOS CPV
9. MAGNET
10. ACORDE
11. ABSORBER
12. MUON TRACKING
13. MUON WALL
14. MUON TRIGGER
15. DIPOLE
16. PMD
17. ZDC

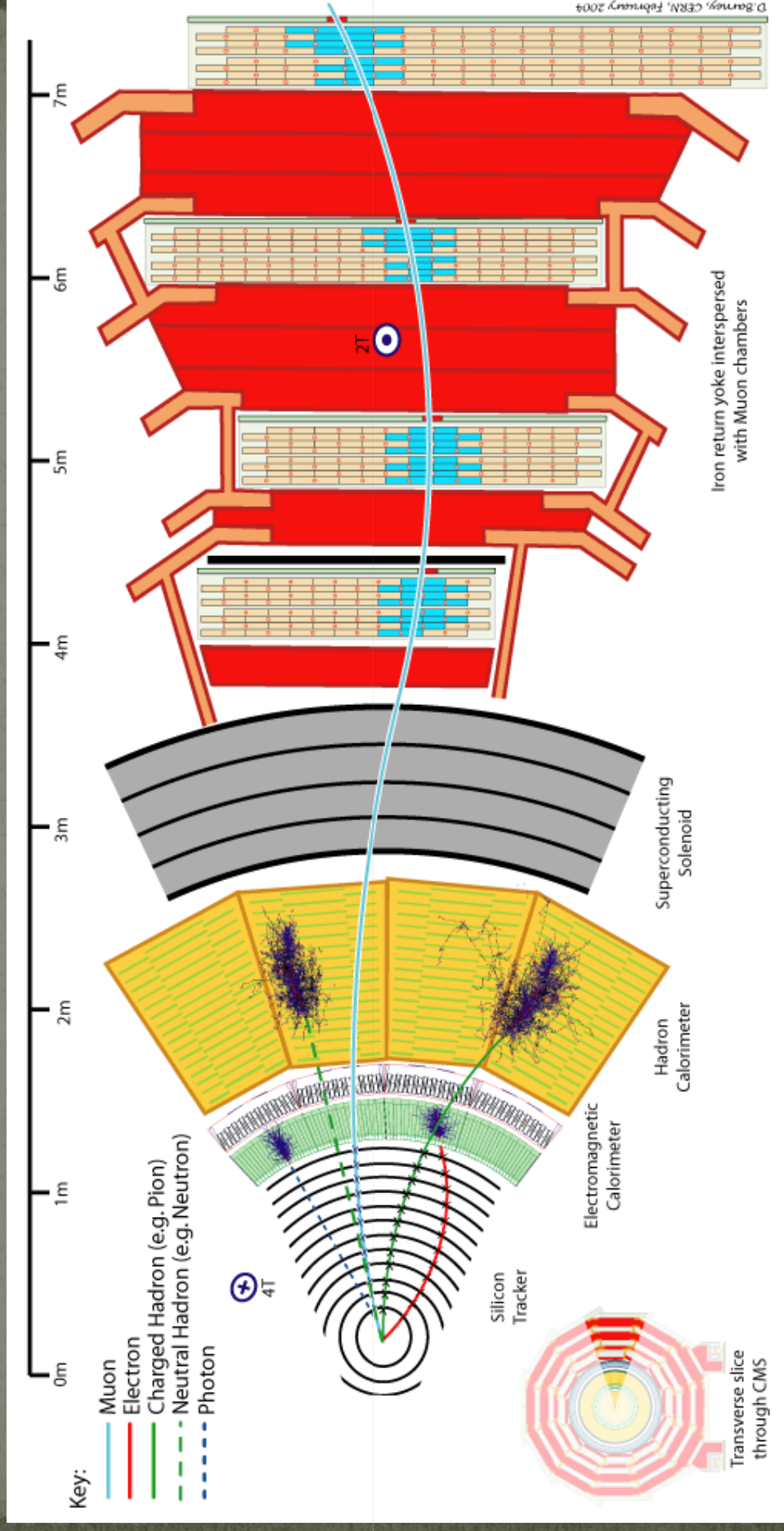


- a. ITS SPD Pixel
- b. ITS SDD Drift
- c. ITS SSD Strip
- d. V0 and T0
- e. FMD

CMS experiment

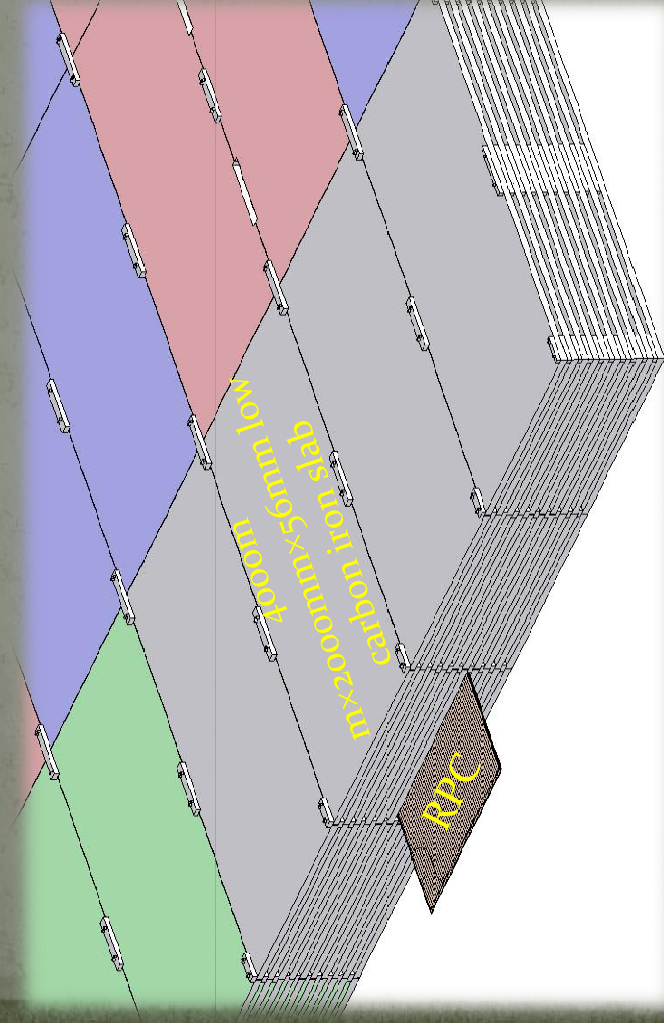


A slice of CMS experiment

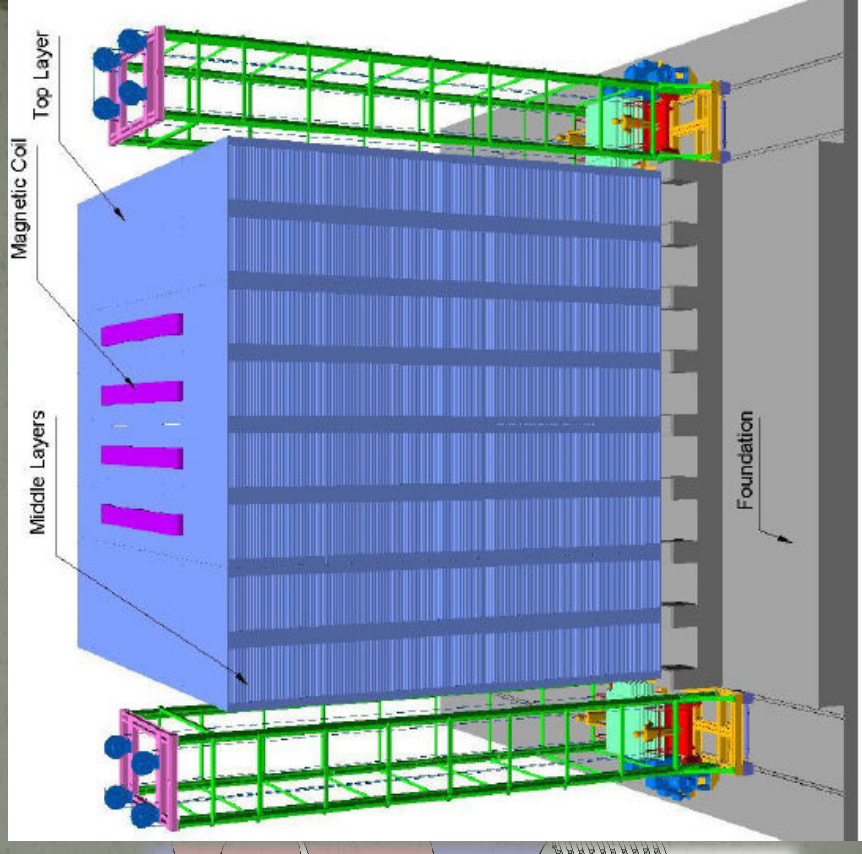


INO's ICAL detector

Detector construction



One of the 3 modules



$16\text{m} \times 16\text{m} \times 14.5\text{m}$

Factsheet of ICAL detector

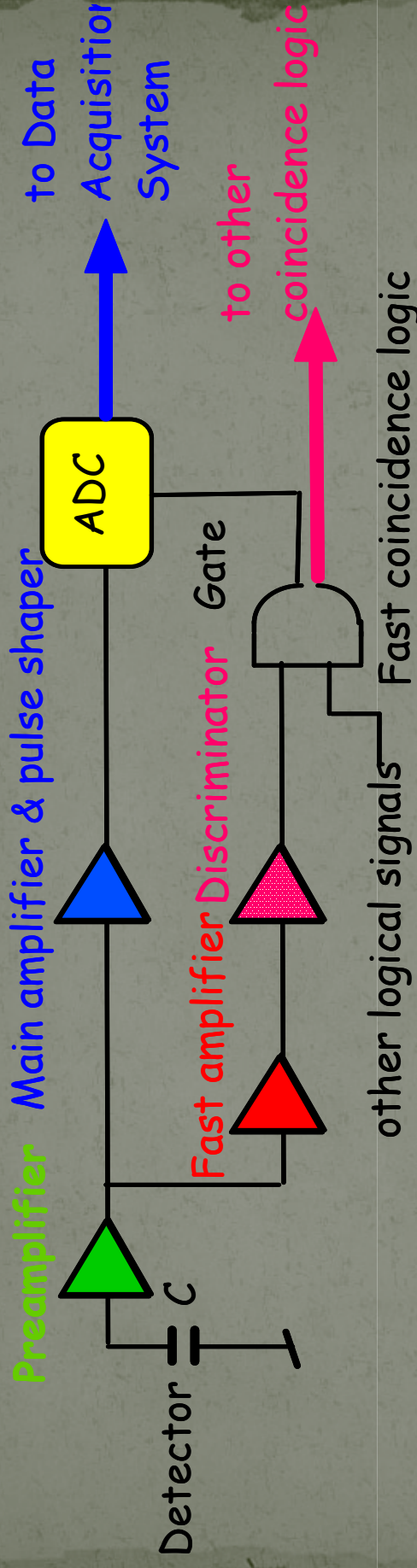
No. of modules	3
Module dimensions	16m × 16m × 14.5m
Detector dimensions	48.4m × 16m × 14.5m
No. of layers	150
Iron plate thickness	56mm
Gap for RPC trays	40mm
Magnetic field	1.3 Tesla
RPC dimensions	1,840mm × 1,840mm × 24mm
Readout strip pitch	3 mm
No. of RPCs/Road/Layer	8
No. of Roads/Layer/Module	8
No. of RPC units/Layer	192
No. of RPC units	28,800 (97,505m ²)
No. of readout strips	3,686,400

Electronic requirements for detectors

Detector	Physics	Technical
Tracking	High spatial precision Large channel count Limited energy precision Limited dynamic range	Low power $\sim$ mW/channel High radiation levels ~ 10 Mrad
Calorimeter	High energy resolution Large energy range Excellent linearity Very stable over time	Intermediate radiation levels ~ 0.5 Mrad Power constraints
Muon	Very large area Moderate spatial resolution Accurate alignment & stability	Low radiation levels

Amplifier systems for spectroscopy

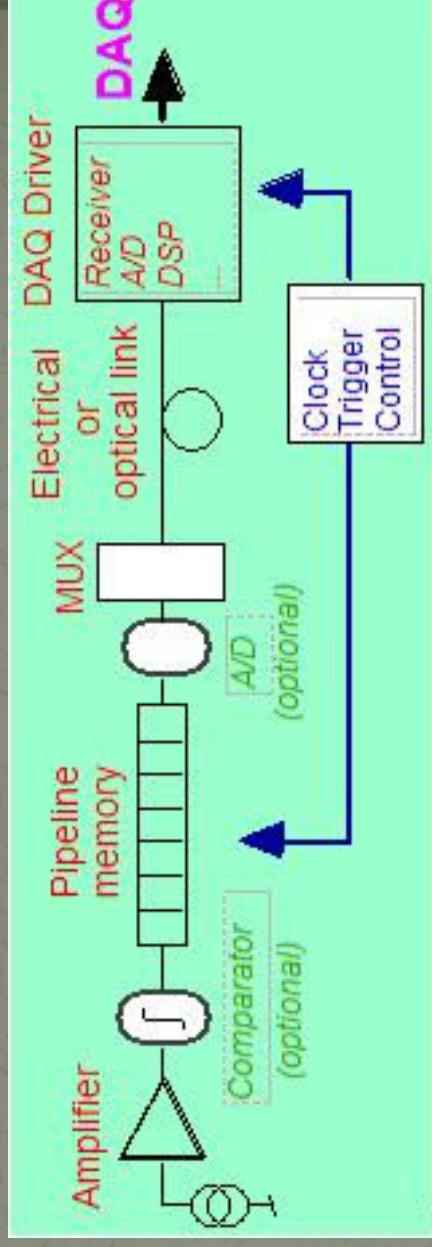
- Typical application - precise measurements of x-ray or gamma-ray energies



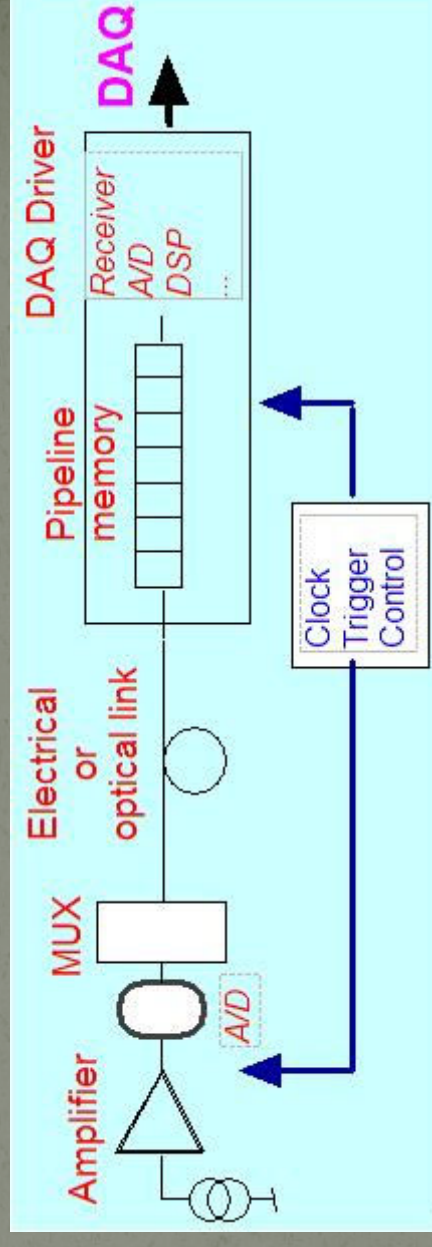
- Pre-amplifier - first stage of amplification
- Main amplifier - adds gain and provides bandwidth limiting
 - ADC - analog to digital conversion - signal amplitude to binary number
- Fast amplifier and logic
 - Start ADC ("gate") and flag interesting "events" to DAQ system
 - Most signals arrive randomly in time.
 - Other logic required to maximise chance of "good" event, eg second detector

Generic detector HEP readout system

- Functions required by all systems
 - Amplification and filtering
 - Analog to digital conversion
 - Association to beam crossing
 - Storage prior to trigger
 - Dead time free readout
 - Pre-DAQ storage
- Calibration
- Control
- Monitoring



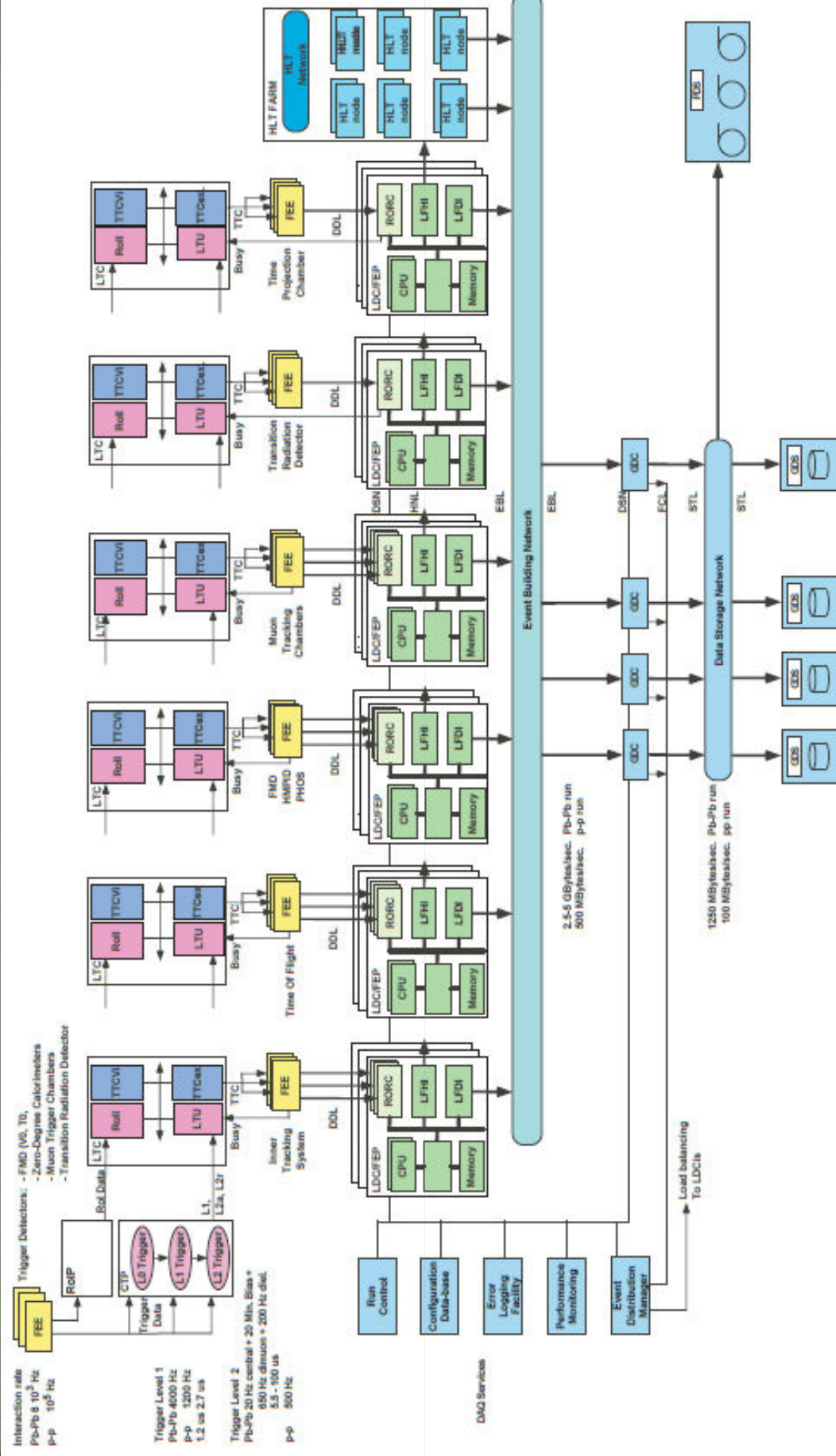
- Calorimeter and muon detector functions
 - First level trigger primitive generation
- Optional
 - Location of digitisation & memory



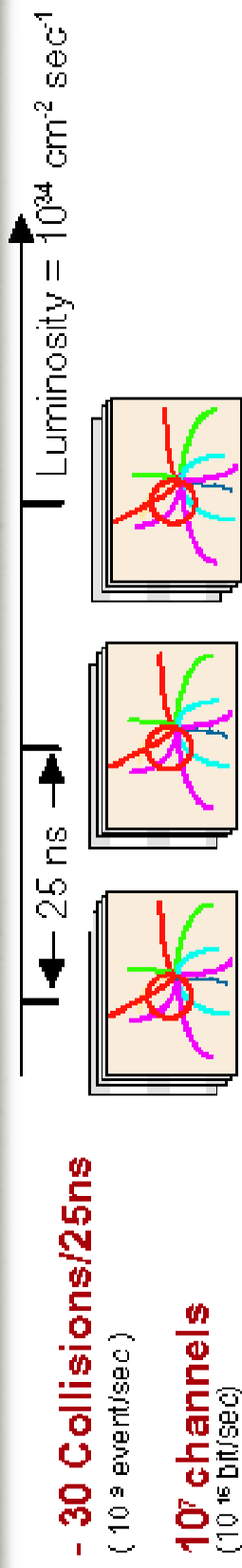
ALICE trigger and DAQ systems

- For every bunch crossing in the LHC machine, the Central Trigger Processor (CTP) decides within less than one microsecond whether to collect the data resulting from a particular collision.
- The trigger decision is distributed to the front-end electronics (FEE) of each detector via the corresponding Local Trigger Unit (LTU) and an optical broadcast system: the Trigger, Timing and Control system (TTC).
- Upon reception of a positive decision, the data are transferred from the detectors over the 400 optical Detector Data Links (DDL) via PCI adapters (RORC) to a farm of 300 individual computers; the Local Data Concentrator/Front-End Processors (LDC/FEP).
- The several hundred different data fragments corresponding to the information from one event are checked for data integrity, processed and assembled into sub events.
- These sub events are then sent over a network for the event building to one of the 40 Global Data Collector computers (GDC), which can process up to 40 different events in parallel.
- 20 Global Data Storage Servers (GDS) store the data locally before their migration and archive in the CERN computing center where they become available for the offline analysis.
- The hardware of the ALICE DAQ system is largely based on commodity components: PC's running Linux and standard Ethernet switches for the event building network. The required performances are achieved by the interconnection of hundreds of these PC's into a large DAQ fabric.
- The software framework of the ALICE DAQ is called DATE (ALICE Data Acquisition and Test Environment). DATE is already in use today, during the construction and testing phase of the experiment, while evolving gradually towards the final production system.

ALICE DAQ system



ATLAS/CMS Trigger architectures



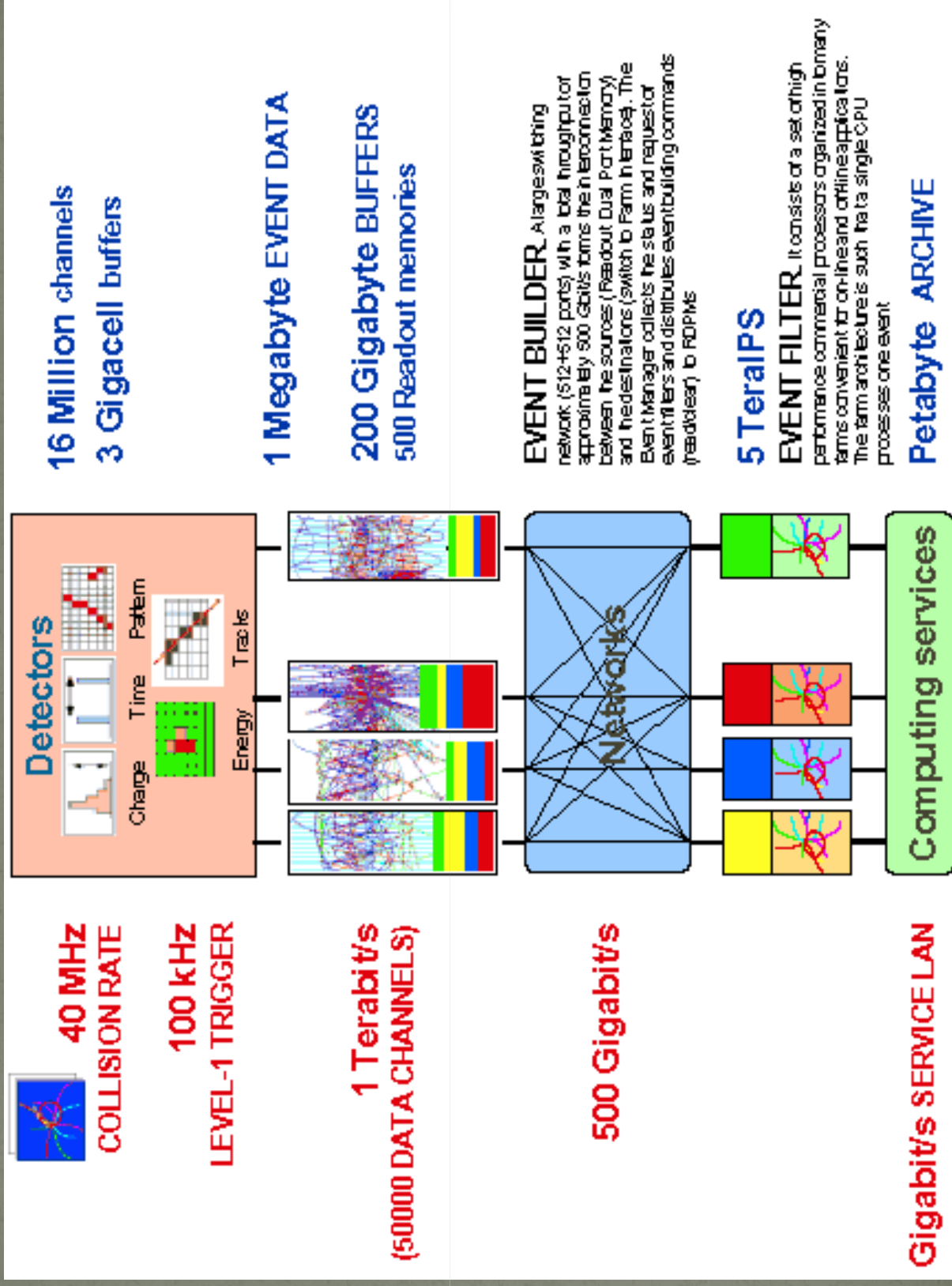
- **30 Collisions/25ns**
(10^9 event/sec.)

10^7 channels
(10^{16} bit/sec)

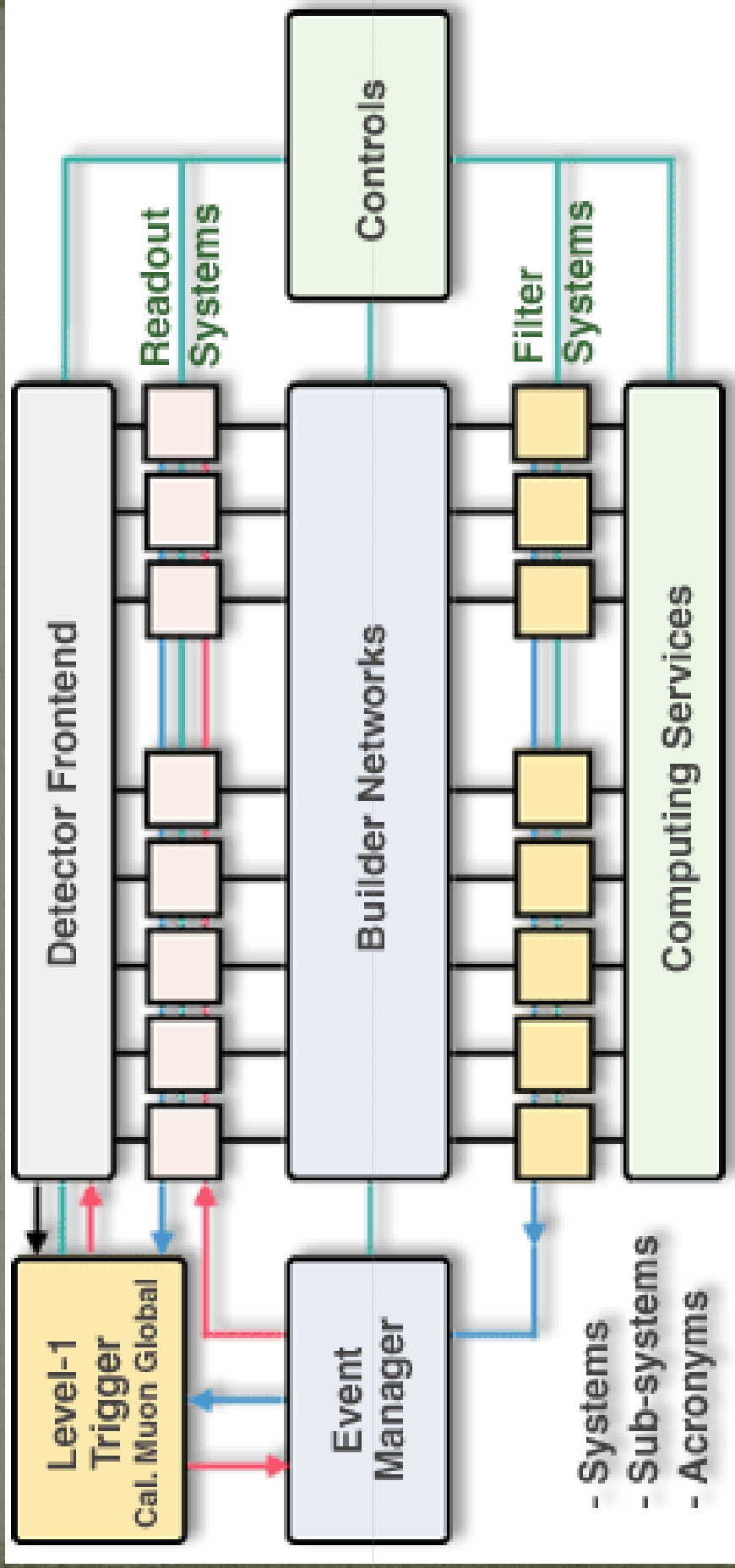
Multilevel trigger and readout systems



Principle of CMS DAQ



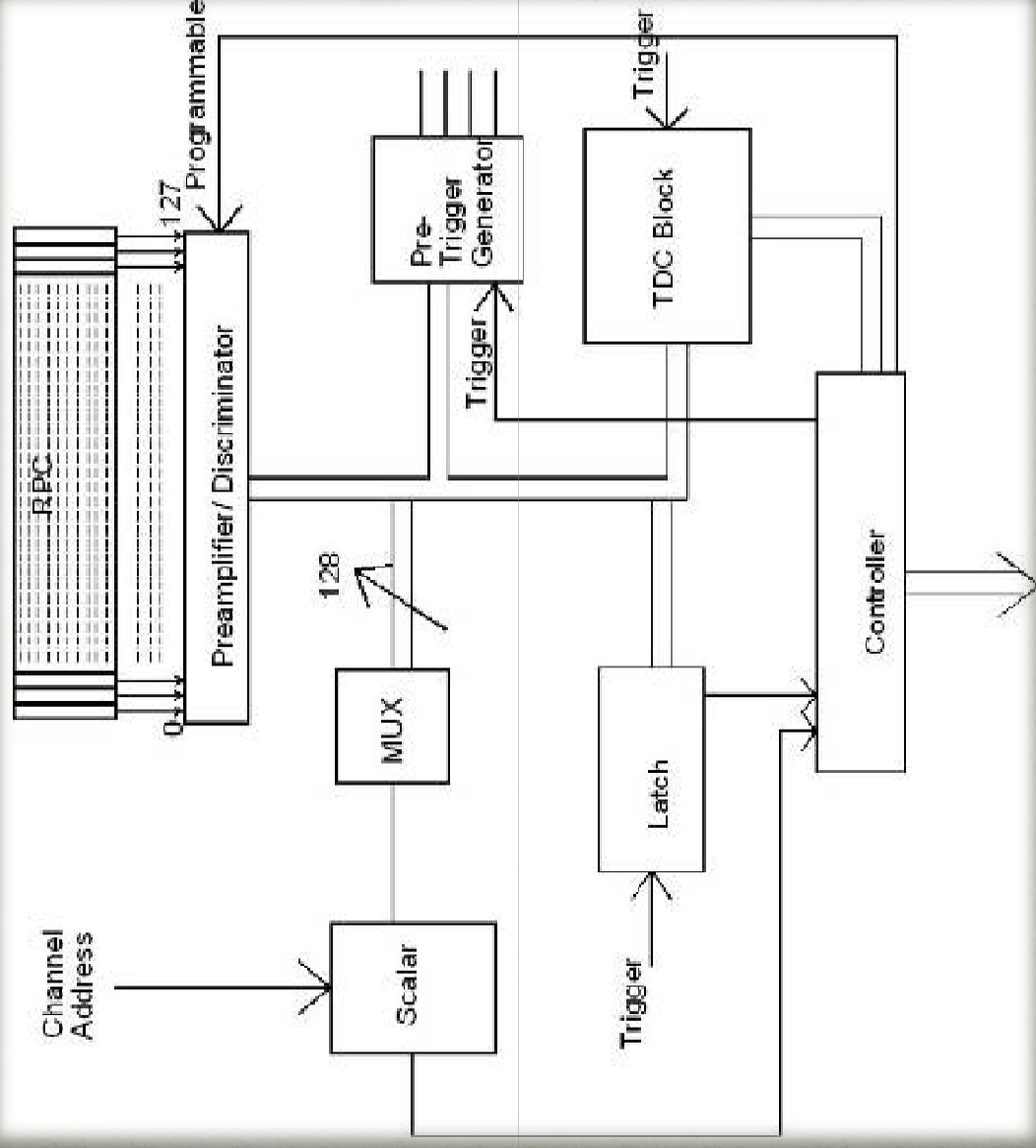
DAQ scheme of CMS experiment



Triggered scheme for ICAL

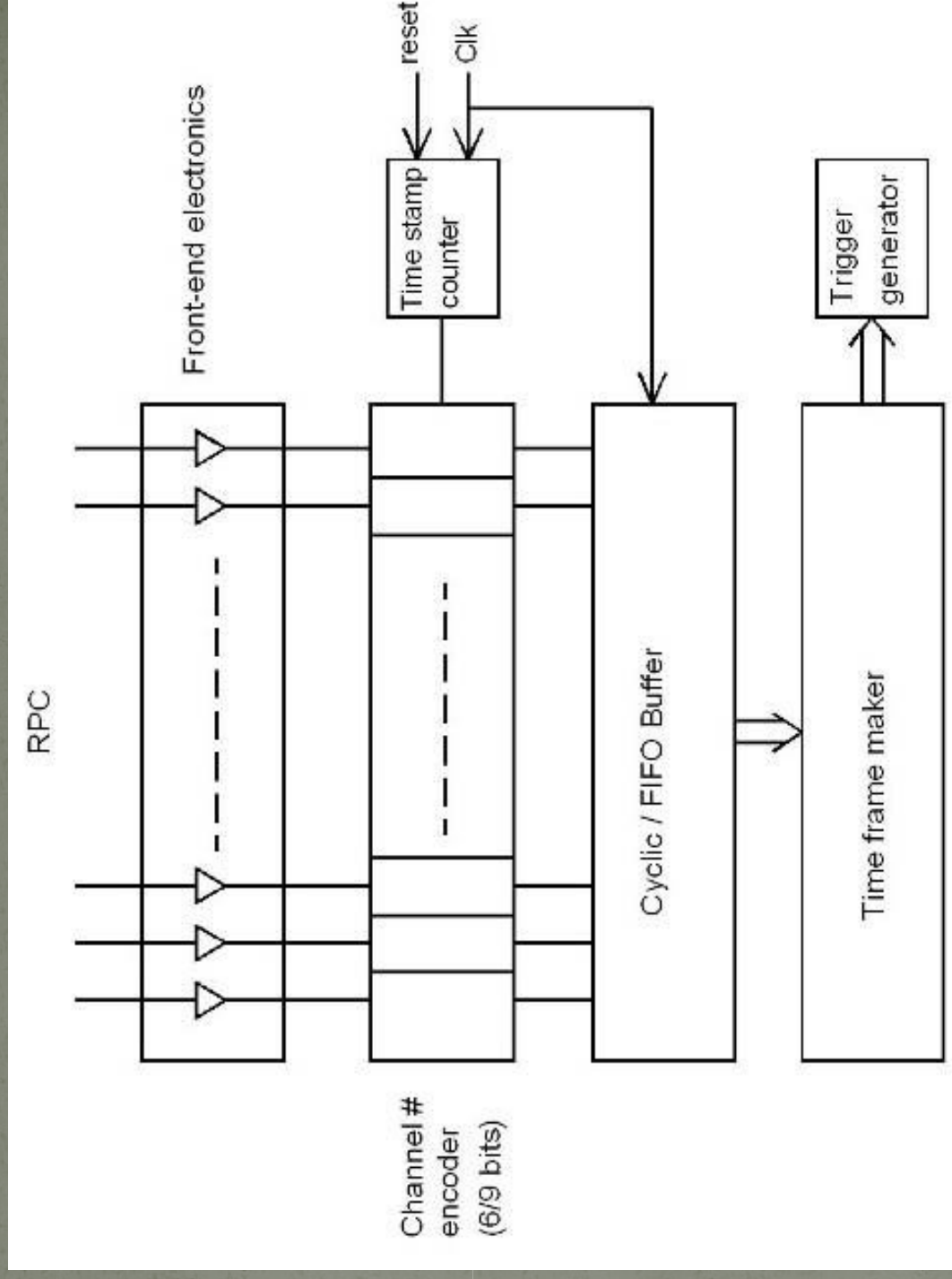
RPC , a unit for front-end processing

- ❖ Conventional architecture
- ❖ Dedicated sub-system blocks for performing various data readout tasks
- ❖ Need for *Hardware based on-line* trigger system
- ❖ Trigger latency issues and how do we take care in implementation
- ❖ Synchronisation of trigger/global clock signals



Trigger-less scheme for ICAL

1. Suitable for low event rate and low background rates
2. On-off control and V_{th} control to disable noisy channels
3. Clock frequency considerations for time stamping



Part-II

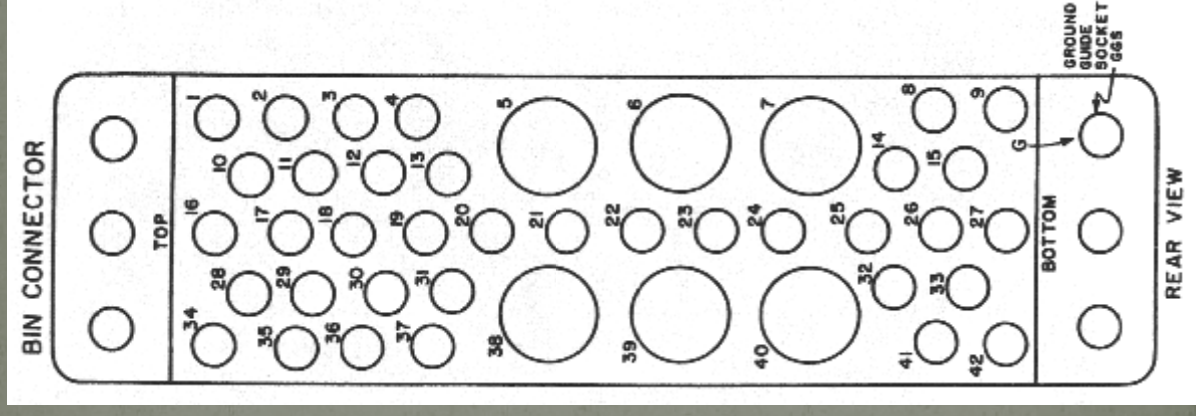
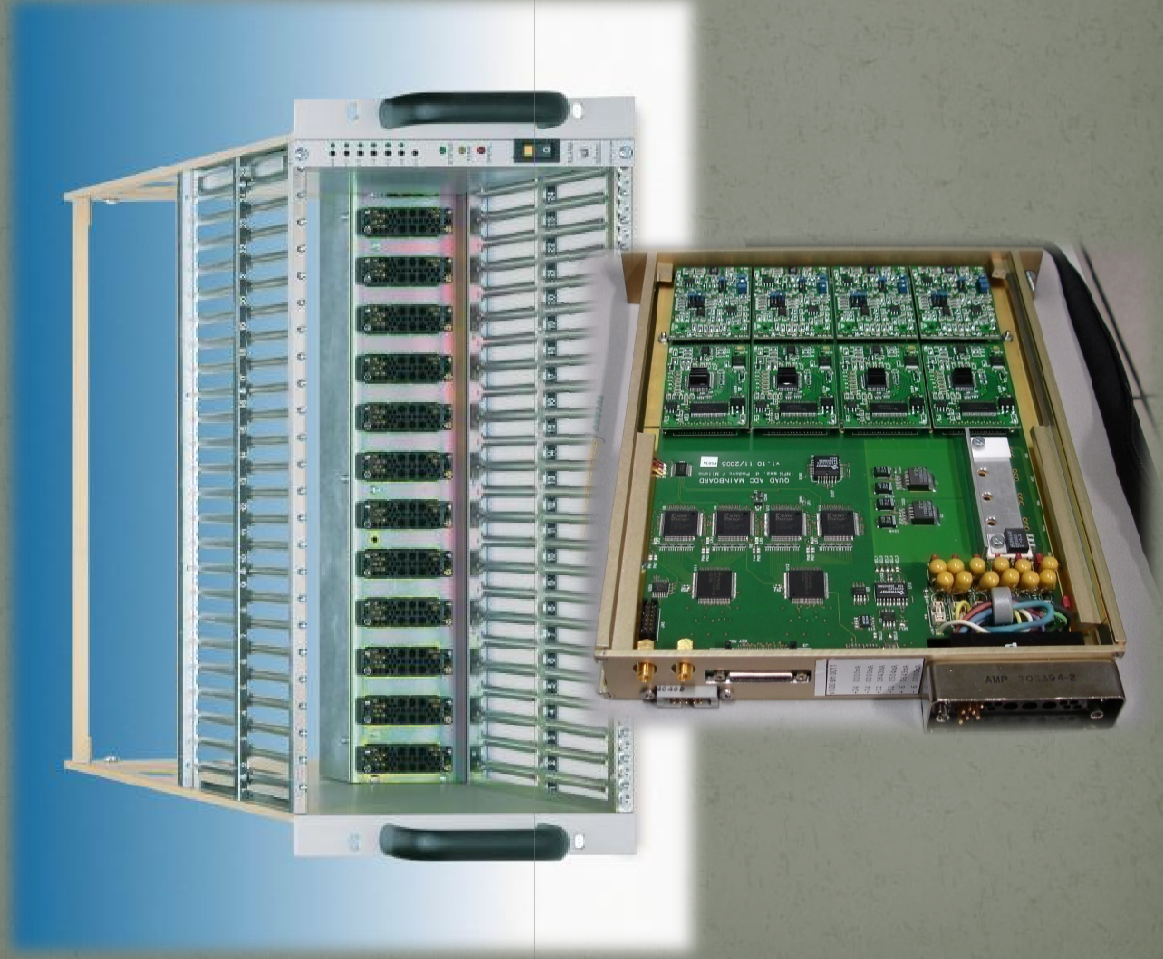
Thursday, February 19, 2009

Acknowledgements & References: G.Hall, W.R.Leo, ALICE collaboration, M.C.S.Williams, L.B.Robinson, G.F.Knoll

Introduction to NIM

- The NIM (Nuclear Instrumentation Methods) standard established in 1964 for the nuclear and high energy physics communities. The goal of NIM was to promote a system that allows for interchangeability of modules.
- Standard NIM modules are required to have a height of 8.75", and must have a width which is a multiple of 1.35". Modules with a width of 1.35" are referred to as single width modules and modules with a width of 2.7" are double width modules, etc. The NIM crate, or NIM bin, is designed for mounting in EIA 19" racks, providing slots for 12 single-width modules. The power supply, which is in general, detachable from the NIM bin, is required to deliver voltages of +6 V, -6 V, +12 V, -12 V, +24 V, and -24 V.
- The NIM standard also specifies three sets of logic levels.
 - In fast-negative logic, usually referred to as NIM logic, logic levels are defined by current ranges. Since the standard also requires 50 ohm input/out impedances, these current ranges correspond to voltages of 0 V and -0.8 V for logic 0 and 1 respectively. Fast-negative logic circuitry can provide NIM signal with rise times of order 1 nsec.
 - Slow-positive logic, is rarely used in fast-pulse electronics due to the slow rise times involved.
 - Specifications for ECL (emitter-coupled logic) voltage levels and interconnections have been added to the NIM subsequently.

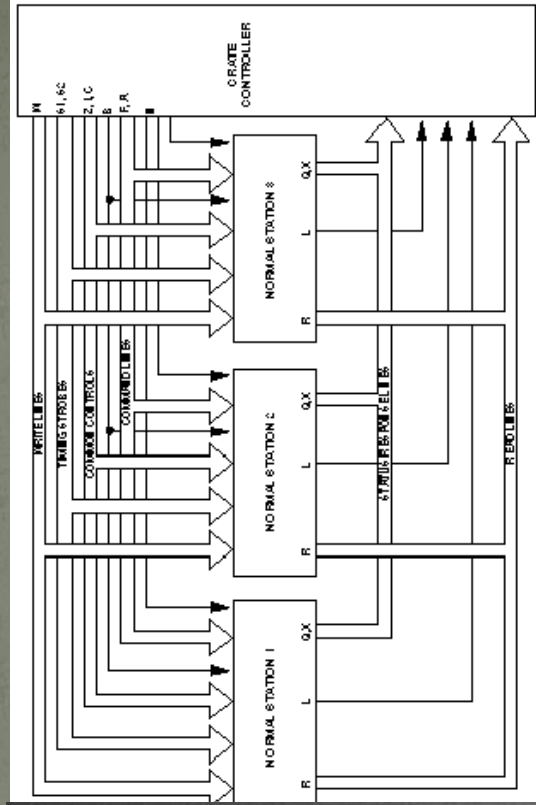
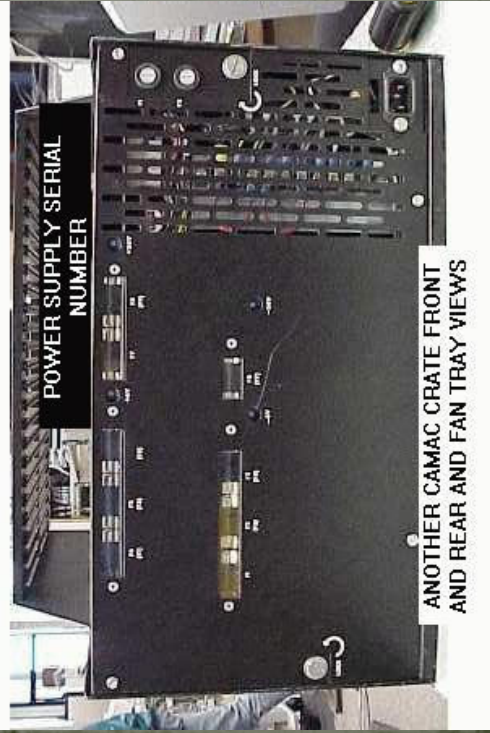
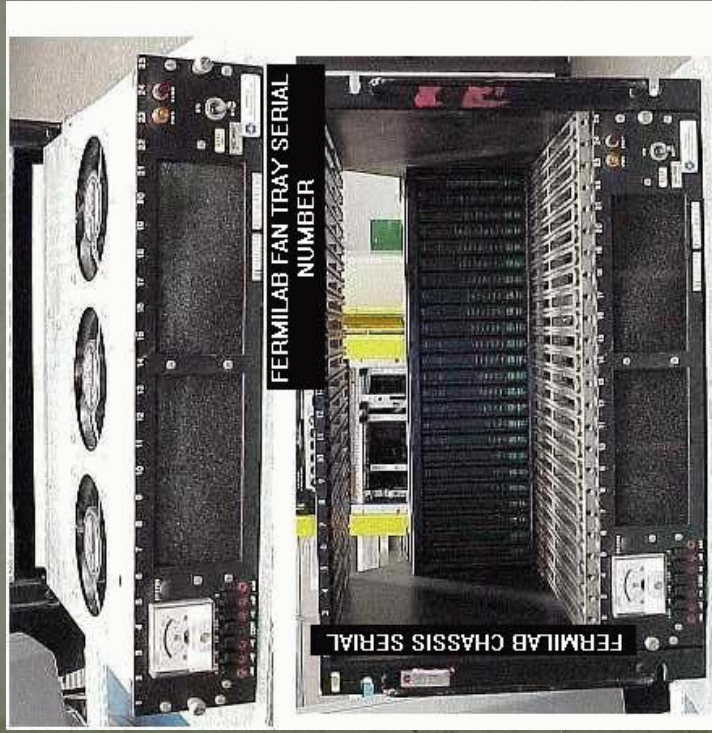
NIM crate and power supplies



PIN	FUNCTION
1	RESERVED
2	RESERVED
3	BIN GATE
4	RESERVED
5	
6	
7	
8	+200 V D.C.
9	SPARE
* 10	+6 V
* 11	-6 V
12	RESERVED
13	SPARE
14	SPARE
15	RESERVED
* 16	+12 V
* 17	-12 V
18	SPARE
19	RESERVED
20	SPARE
21	SPARE
22	RESERVED
23	RESERVED
24	RESERVED
25	RESERVED
26	SPARE
27	SPARE
* 28	+24 V
* 29	-24 V
30	SPARE
31	SPARE
32	SPARE
33	117 V A.C. (HOT)
* 34	POWER RETURN GND
* 35	RESET
36	GATE
37	SPARE
38	
39	
40	
* 41	117 V A.C. (NEUTRAL)
* 42	HIGH QUALITY GND
G	GROUND GUIDE PIN

* Must be bussed to all bin connectors GPIB through PG12B.

CAMAC hardware and signals



TITLE		CAM- DESIGRATION		TACS		USE AT A MODULE	
Command		N		1		Selects the module (individual line from control station).	
Sub-address		A1, 2, 4, 8		4		Selects a section of the module.	
Function		F1, 2, 4, 8, 16		5		Defines the function to be performed in the module.	
Timing		S1		1		Controls first phase of operation. (Dataway signals may change.)	
S1		S2		1		Controls second phase. (Dataway signals may change.)	
Data		W1-M24		24		Bring information to the module.	
Write		R1-R24		24		Take information from the module.	
Status		L		1		Indicates request for service (individual line to control station).	
Look-active		B		1		Indicates that Dataway operation is in progress.	
Busy		Q		1		Indicates status of feature selected by command.	
Response		X		1		Indicates that module is able to perform action required by the command.	
Command Assigned							
Common Controls						Operate on all stations connected to them, no command required.	
Initialize		Z		1		Sets module to a defined state. (Accompanied by S2 and S3).	
Inhibit		I		1		Disables features for duration of signal.	
Clear		C		1		Clears registers (accompanied by S2 and S3).	
Non-Standard Connections		P1, P2		2		For specified use.	
Free bus-lines		P3-P5		3		For unspecified interconnections.	
Path Controls						No Dataway lines.	
Mandatory Power Lines							
+5V DC		+5V DC		1		Power return.	
+12V DC		+12V DC		1			
-12V DC		-12V DC		1			
-24V DC		-24V DC		1			
0V		0V		2			
Additional Power Lines							
+12V DC		+12V DC		1		Lines are reserved for the following power supplies.	
-12V DC		-12V DC		1		Low current for indicators, etc.	
Clean Earth		Clean Earth		1		Reference for circuits requiring clean earth.	
Reserved V1, V2		Reserved V1, V2		2		Reserved for future allocation.	

CAMAC dataway timing charts

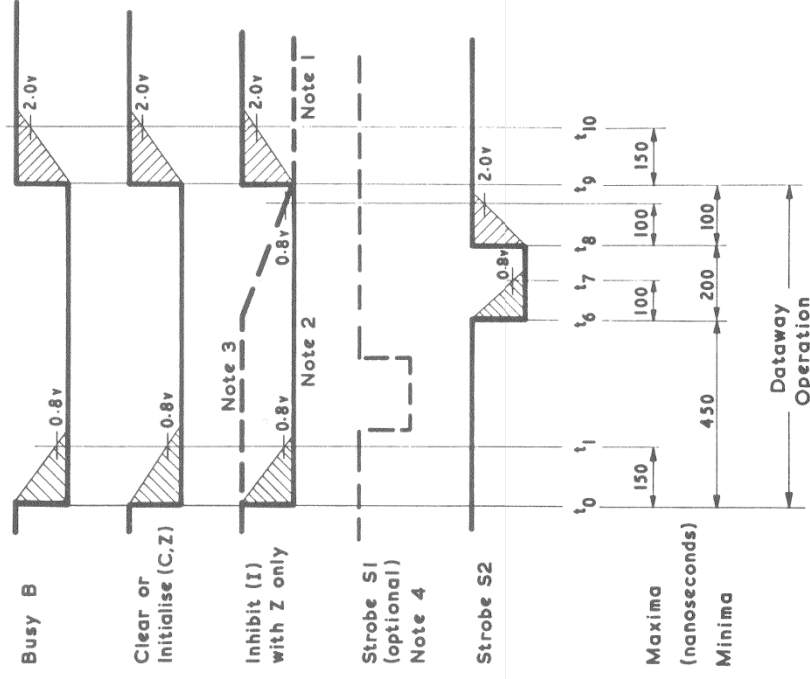


Fig. 2.17.
Timing of a dataway unaddressed operation.

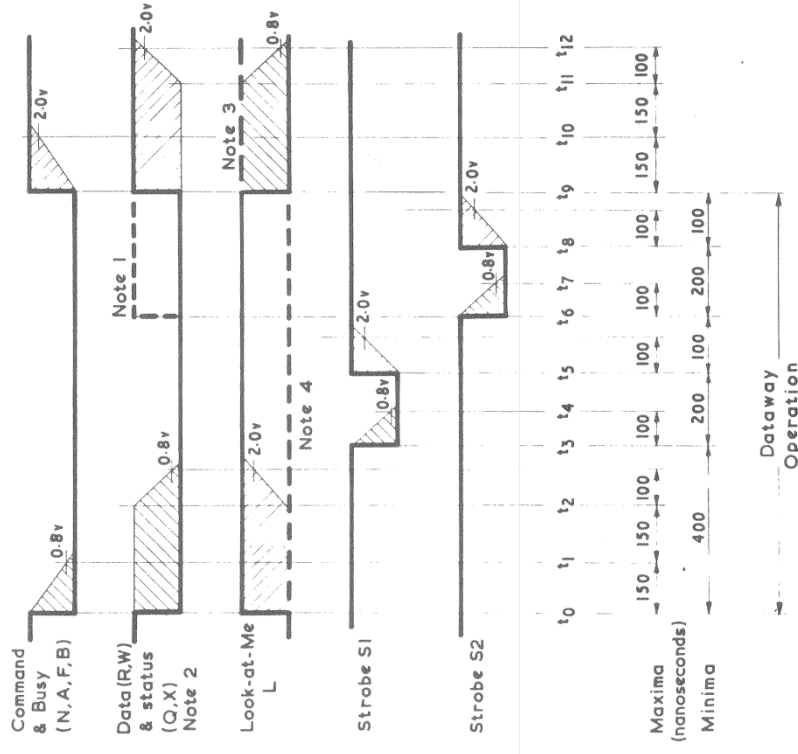


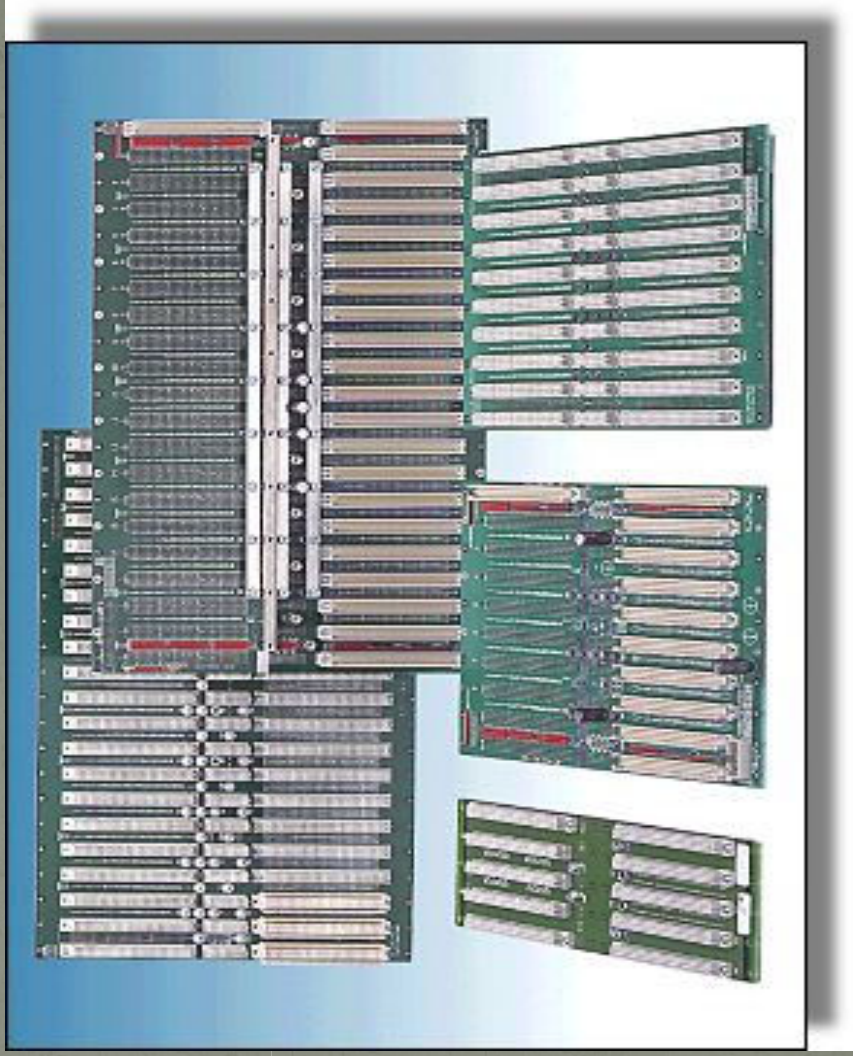
Fig. 2.16.
Timing of a dataway command operation.

CAMAC system development



VME system hardware components

A modern fast, high density, modular, scientific instrumentation standard



Transmission of data

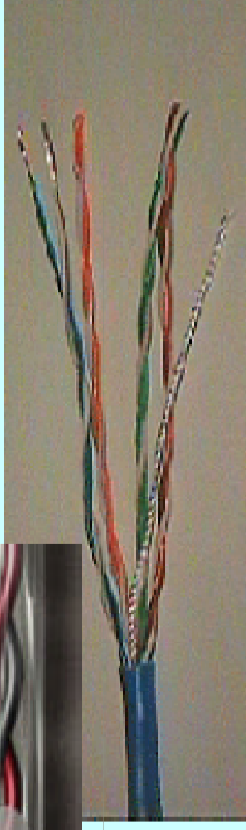
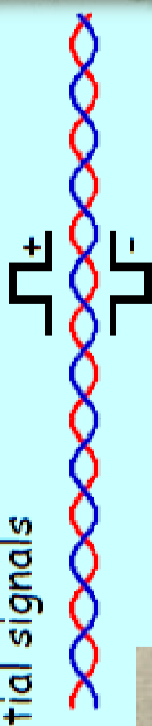
- Real systems are often distributed
- **Data source is remote from signal processing**
- Instruments in hazardous or very remote environment
 - Eg. satellites, HEP, nuclear reactors,...
- But also applies to much shorter distances - like nearby labs or instruments in the same room
- Need to transfer data from source to receiver
- And usually send messages (eg. control signals) back
- Need to understand
 - Practical ways of doing this
 - Issues: power, speed, noise,... other physical constraints
- Methods - a mixture
 - Electrical, but increasing use of optical fibres,
 - Radio for satellites and space, mobile telephones,...

Cables

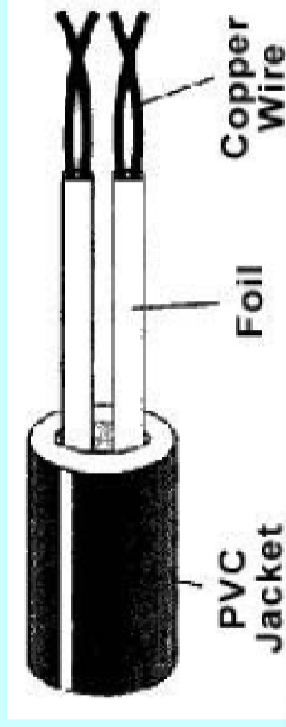
- Any wire has inductance, capacitance and resistance
so when is it a transmission line?

- Twisted pair

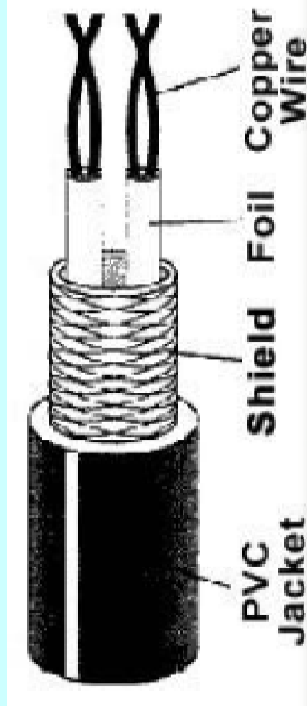
simple pair of wires, mainly intended for differential signals



Can also be unshielded...



or shielded



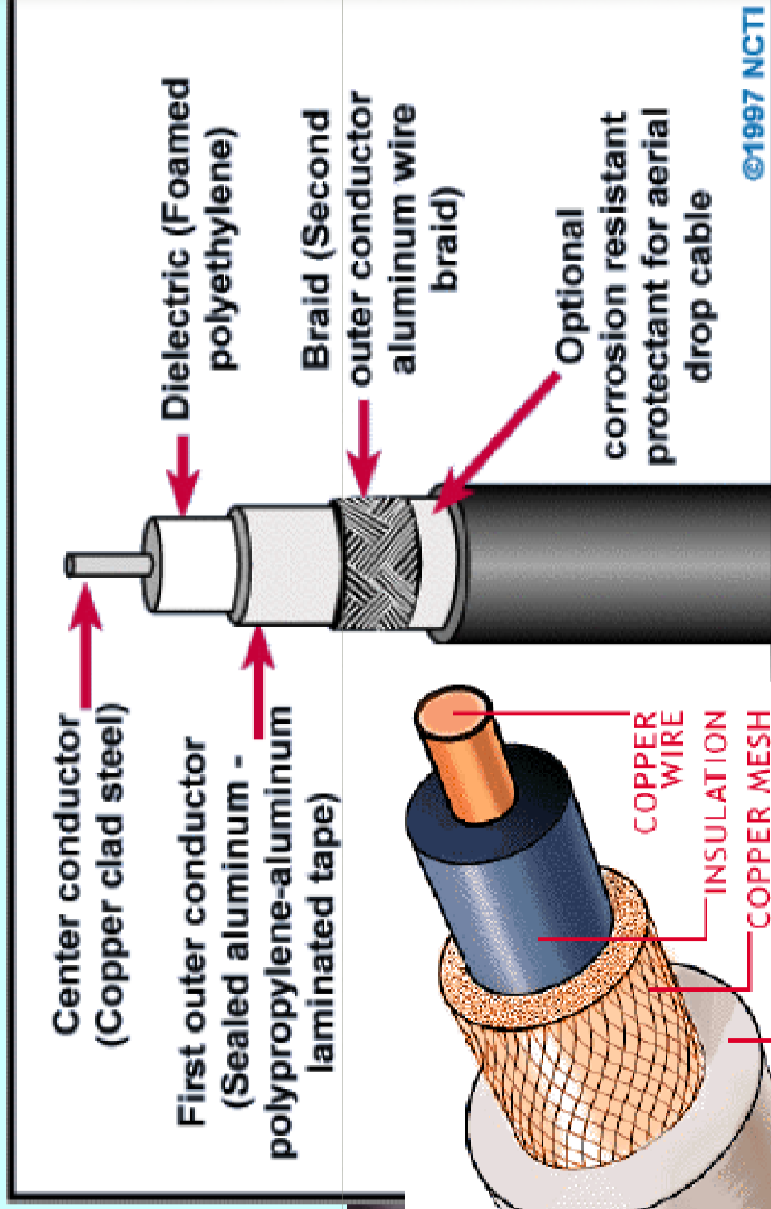
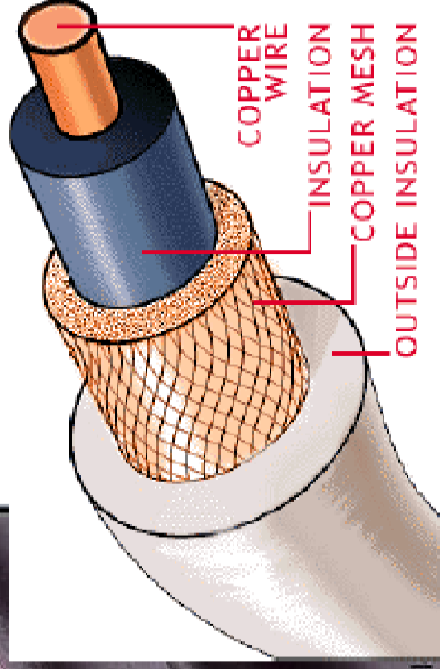
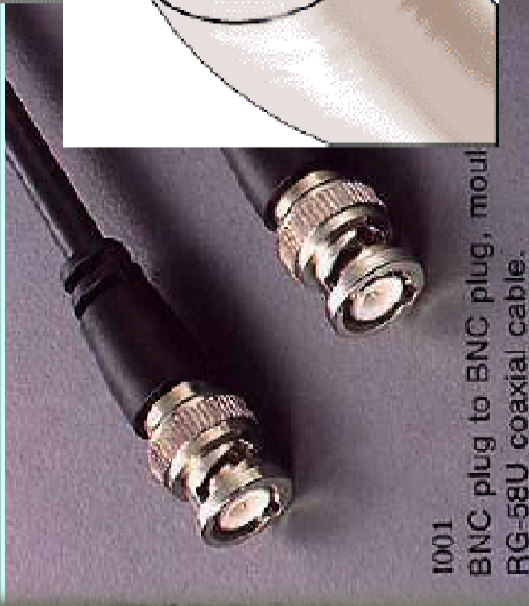
Coaxial cable

central copper core radius r_1 , with plastic dielectric, braided metal shield in cylindrical geometry radius r_2

$$C_0 = 2\pi\epsilon/\ln(r_2/r_1) \quad L_0 = (\mu_0/2\pi).\ln(r_2/r_1) \quad \text{see lecture 1 notes}$$

•Design

Cu braid connected to ground provides electrical shield use special connectors



Termination and Matching

Termination and Matching

- boundary conditions at termination

$$I_{inc} + I_{ref} = I_L \quad \& \quad V_{inc} + V_{ref} = V_L$$

apply them (NB $V_{ref} = -I_{ref}Z_0$)

$$V_{ref}/V_{inc} = (Z_L - Z_0)/(Z_L + Z_0)$$

$$V_L/V_{inc} = 2Z_L/(Z_L + Z_0)$$

- open circuit termination $Z_L = \infty$

$$V_{ref}/V_{inc} = +1 \quad V_L/V_{inc} = 2 \quad \text{reflected signal} = \text{incident signal}$$

- short circuit termination $Z_L = 0$

$$V_{ref}/V_{inc} = -1 \quad V_L/V_{inc} = 0 \quad \text{inverted fully reflected signal}$$

- matched termination $Z_L = Z_0$

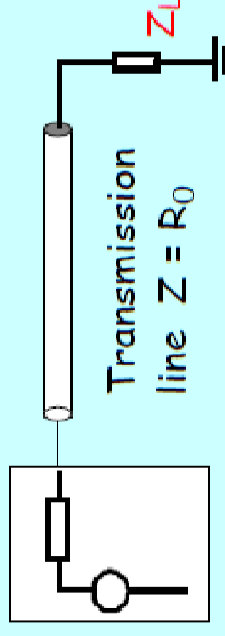
$$V_{ref}/V_{inc} = 0 \quad V_L/V_{inc} = 1 \quad 100\% \text{ transmission to load}$$

- improper termination usually causes unwanted effects

but can sometimes make use of reflection

eg short circuit termination + step pulse = square pulse with width = $2\Delta t$

- why don't we always match terminate?



To match or not? (i)

- Impedance matching is a general question, not only for transmission lines
- Match if
 - to transfer maximum power to load (source must be capable)
 - eg audio speakers
 - minimise reflections from load
 - very important in audio, fast (high frequency) systems, to avoid ringing
 - or multiple pulses (eg in counting systems)
- fast pulses
 - pulse properties can contain important information
 - usually don't want to change
 - sometimes we wish to do this with "too fast" signals - "spoiling"
- Usually match by choosing impedances, adding voltage buffers
- transformer matching is another method if this is impractical

To match or not? (ii)

- Don't match if
 - High impedance source with small current signals - typical of many sensors
 - photodiode, or other sensors must drive high impedance load
 - short cables are required to avoid difficulties
 - Weak voltage source, where drawing power from source would affect result
 - eg bridge circuits
- require to change properties of fast pulse
 - eg pulse widening for ease of detection
- electronics with limited drive capabilities
 - eg logic circuits, many are designed to drive other logic, not long lines
 - CMOS circuits, even with follower, are an example
- If you get this wrong, often end up with new time constants in the system
 - or prevent system from working at all, eg diode with low R load

Coaxial cable limits

- Transmission speed and bandwidth limiting
 - all cables have finite resistance
 - remarkably small - see table for calculated values
 - for long cables, RC time constant per unit length becomes noticeable
 - therefore expect delay, attenuation and finite rise time in fast pulses
- When is a cable a transmission line?
 - not reasonable to assume transmission line behaviour unless length of line is at least
 - $\sim 1/8$ wavelength
 - Other forms of transmission line
 - in high speed circuits, tracks must be laid out carefully using knowledge of the characteristics of the boards to control delays, rise times and signal velocities
 - eg parallel tracks,...
 - often need measurement to define parameters precisely
 - ultra high frequencies need waveguides or alternative

Amplifiers

- inescapable in electronic instruments
 - amplifiers are needed for many instruments
 - even if not used to boost signals, amplifiers are the basis of most important functional blocks
- in many circumstances amplification, in the sense of “boosting” signals, is vital
 - signals to be measured or observed are often small
 - defined by source - or object being observed
 - and sensor - it is not usually easy to get large signals
 - data have to be transferred over long distances without errors
 - safest with “large” signals

Amplifiers in systems

- Amplification
 - Role of preamplifier
 - single gain stage rarely sufficient
 - add gain to avoid external noise eg to transfer signals from detector
 - practical designs depend on detailed requirements
 - constraints on power, space,... cost in large systems
 - e.g. ICs use limited supply voltage which may constrain dynamic range
- Noise will be an important issue in many situations
 - most noise originates at input as first stage of amplifier dominates
 - often refer to Preamplifier = input amplifier
 - may be closest to sensor, subsequently transfer signal further away
- In principle, several possible choices
 - V sensitive (Conventional)
 - I sensitive (Used with low impedance detectors)
 - Q sensitive (Used with semiconductor detectors)

Voltage sensitive amplifier

- As we have seen many sensors produce current signals but some examples produce voltages - thermistor, thermocouple, ...
op-amp voltage amplifier ideal for these especially slowly varying signals - few kHz or less
- For sensors with current signals voltage amplifier usually used for secondary stages of amplification

• Signal $V_{out} = Q_{sig}/C_{tot}$

C_{tot} = total input capacitance

C_{tot} will also include contributions from wiring and amplifier

V_{out} depends on C_{tot}

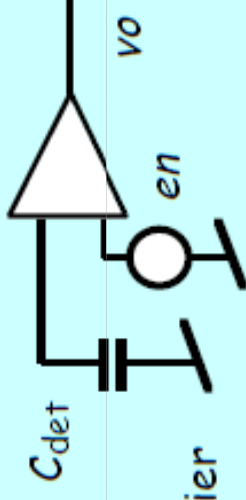
not desirable if C_{det} is likely to vary

eg with time, between similar sensors, or depending on conditions

• Noise to be discussed more later

contribution from amplifier, and possibly sensor

$S/N = Q_{sig}/(C_{tot} \cdot V_{noise})$ can it be optimised?



Current sensitive amplifier

- Common configuration, eg for photodiode signals

$$V_{out} = -A V_{in}$$

$$V_{in} - V_{out} = i_{in} R_f$$

$$V_{out} = -[A/(A+1)] \cdot i_{in} R_f \approx -i_{in} R_f$$

- Input impedance

$$V_{in} = i_{in} R_f / (A+1) \quad Z_{in} = R_f / (A+1)$$

- Effect of C & R_{in} - consider in frequency domain

$$v_0 = i(1/j\omega C || R_{in})$$

$$= i(\omega)R/(1 + j\omega\tau)$$

input signal convoluted with falling exponential

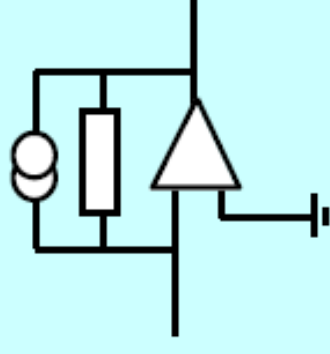
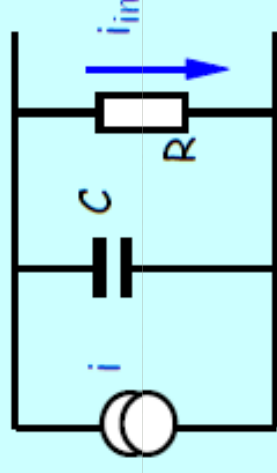
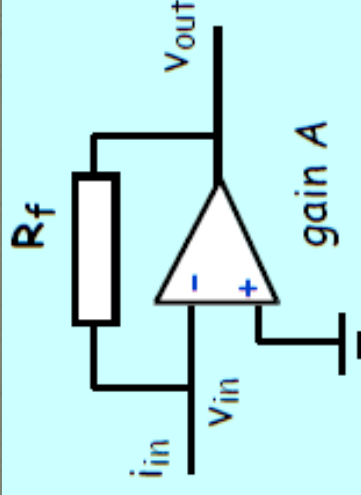
increasing R_f to gain sensitivity will increase τ

fast pulses will follow input with some broadening

- Noise

will later find that feedback resistor is a noise source

contributes current fluctuations at input $\sim 1/R_f$



Charge sensitive amplifier

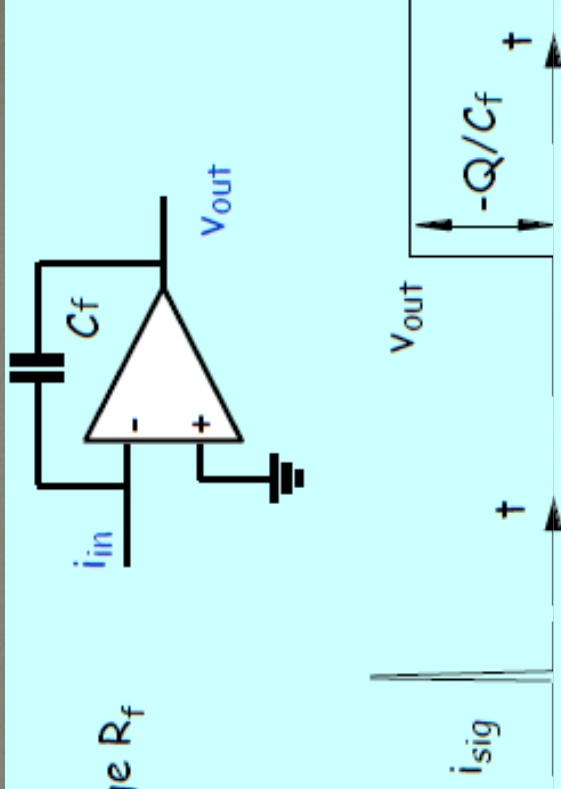
- Ideally, simple integrator with C_f but need means to discharge capacitor - large R_f
- Assume amplifier has Z_{in} very high (usual case)

$$V_{out} = -AV_{in}$$

$$V_{out} - V_{in} = i_{in}/j\omega C_f$$

$$V_{out} = -[A/(A+1)] \cdot i_{in}/j\omega C_f \approx i_{in}/j\omega C_f$$

$$\Rightarrow -Q/C_f$$



- Input impedance

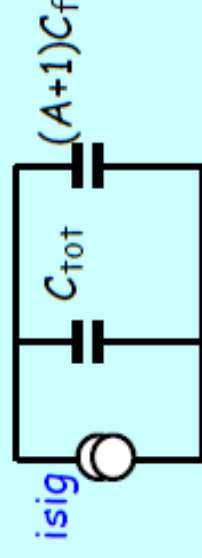
$$V_{in} = i_{in}/(A+1)j\omega C_f \quad C = (A+1)C_f \text{ at low } f$$

so amplifier looks like large capacitor to signal source
low impedance but some charge lost

$$\text{e.g. } A = 10^3 \quad C_f = 1\text{pF}$$

$$Q_A = Q/[1 + C_{tot}/(A+1)C_f] \quad C_{tot} = 10\text{pF} \quad Q_A/Q = 0.99$$

$$C_{tot} = 100\text{pF} \quad Q_A/Q = 0.90$$



Feedback resistance

Feedback resistance

- Must have means to discharge capacitor so add R_f

$$Z_f = R_f || 1/j\omega C_f$$

$$V_{out} = -[A/(A+1)] \cdot i_{in} Z_f$$

$$= i(\omega) R_f / (1 + j\omega\tau_f) \quad \tau_f = R_f C_f$$

step replaced by decay with $\sim \exp(-t/R_f C_f)$ τ is long because R_f is large (noise)
 easiest way to limit pulse pileup - differentiate
 ie add high pass filter

- Pole-zero cancellation

exponential decay + differentiation $\Rightarrow$ unwanted baseline undershoot

introduce canceling network

$$v_0 = 1/(1 + j\omega\tau_f)$$

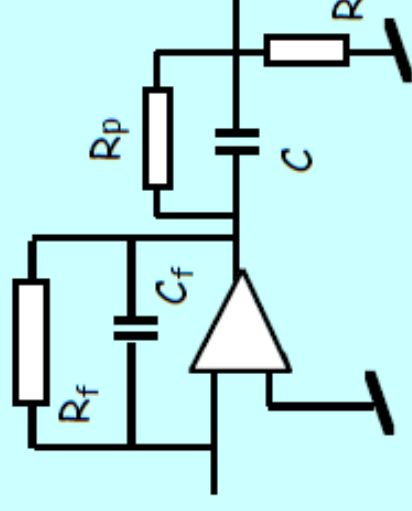
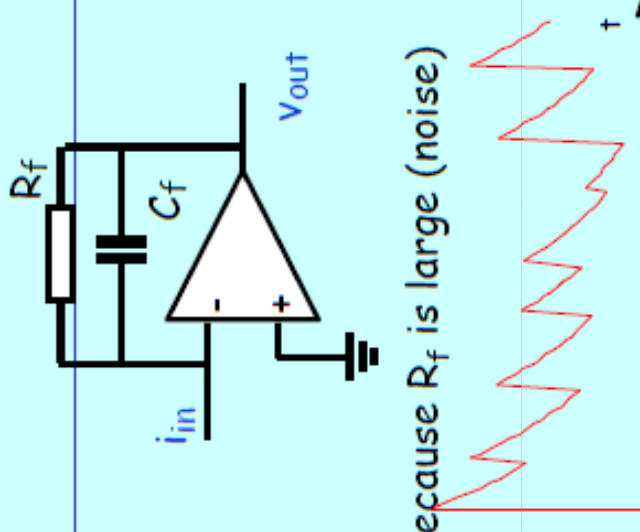
$$v_1 = 1/(1 + j\omega\tau_f)(1 + j\omega\tau_1)$$

$$\tau_1 = RC < \tau_f$$

add resistor R_p so $R_p C = \tau_f$

then

$$v_1' = 1/(1 + j\omega\tau_3) \text{ with } \tau_3 = (R || R_p)C < \tau_f$$



Pulse shaping

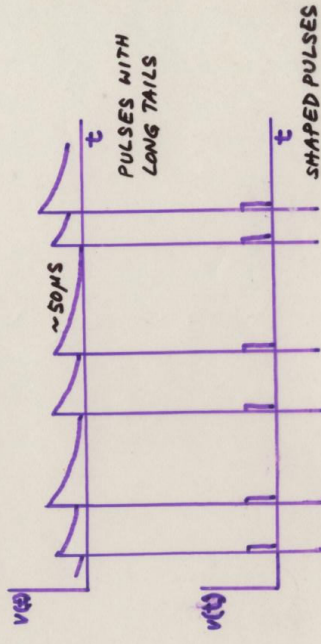
- Amplifiers must preserve the information of interest
 - If timing required: fast response
 - If pulse height required: strict proportionality, limit bandwidth
- Preamplifier pulse
 - Exponential with long tail
 - Pulse pileup: Reduce counting rate or reshape
- Optimization of signal-to-noise ratio
 - For a given noise spectrum, there exists an optimum pulse shape to improve the S/N
 - For ex: Tail pulses in presence of typical noise spectra are not ideal
 - Triangular or Gaussian – symmetric pulse shapes are ideal
- Fast amplifiers: No or very little shaping
- What to do in case you need good timing and pulse height information?

PULSE SHAPING AND FILTERING NETWORKS

- Where do you find these circuits in HEP instrumentation signal chain?

- Why do you need these circuits?

1. To eliminate pulse "pile-up".



2. Optimisation of S/N ratio.

- For a given noise spectrum, there exists an optimum

- Pulse shape in which the signal is least disturbed by noise.

- Look at signal and noise in terms of their Fourier

- Components to study the relation between pulse shape

- and noise.

- ⇒ Filter out those frequencies where noise is maximum.

- Narrowing BW. ⇒ Change of pulse shape

- ⇒ Indication of the filtering scheme.

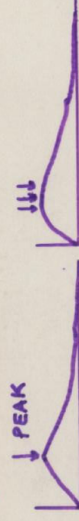
- pulses with long tails not ideal.

- Gaussian or triangular shape preferred.

3. Shaping for DAQ needs.

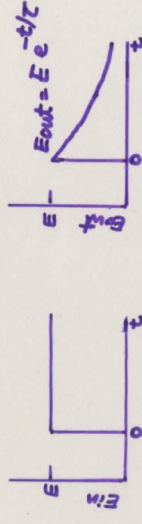
- Signals with sharp peaks vs 'flat' peaks as peak

- Sensing ADC inputs.



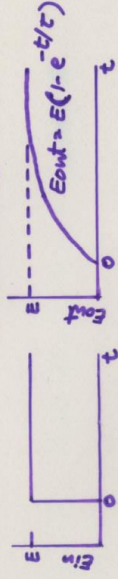
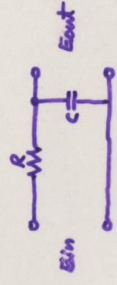
1. CR-RC Shaper circuit:

CR-Differentiator/
High-pass filter



τ should be small compared to input pulse leading or trailing edges.

RC-Integrator/
Low-pass filter



τ should be large compared to time duration of input pulse.

CR-RC shaping most widely used.

Single CR impractical for pulse analysis, high frequency noise components passed through. Low S/N

General Solution of its response of 1K network for step input,

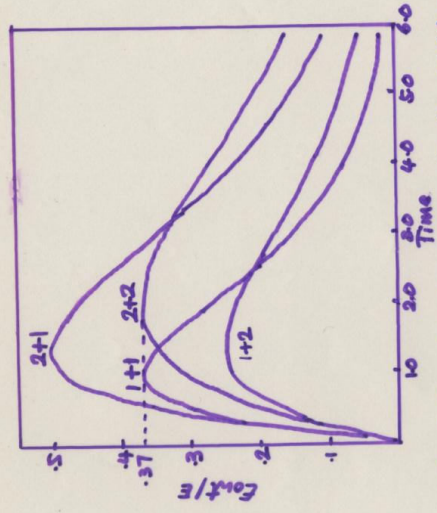
$$E_{out} = \frac{E\tau_1}{\tau_1 - \tau_2} \left(e^{-t/\tau_1} - e^{-t/\tau_2} \right)$$

Particular Solution for $\tau = \tau_1 = \tau_2$,

$$E_{out} = E \frac{t}{\tau} e^{-t/\tau}$$

τ depends on charge collection time in detector. Smaller, its better for reducing "pile-up". But, limit due to ballistic deficit...

Fig. 3

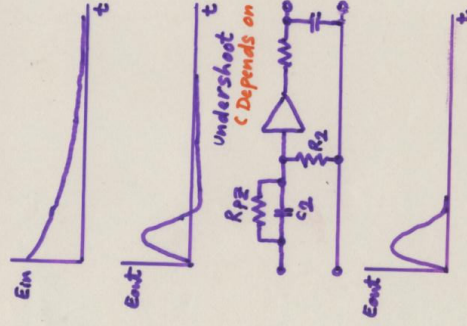


Response of CR-RC for step input, for different pairs of τ_s for CR and RC stages.

- For equal τ_s , Peak at $\sim 1.2\tau$ and return to base line at $\sim 7\tau$.

- studies and observations.

• Pole-Zero Cancellation



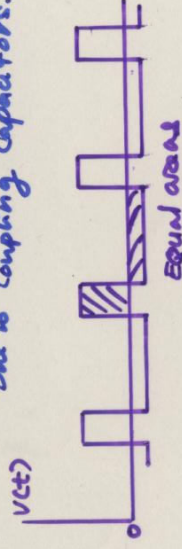
R_2 allows an attenuated replica of the input pulse to pass through to the o/p.

Fig. 4

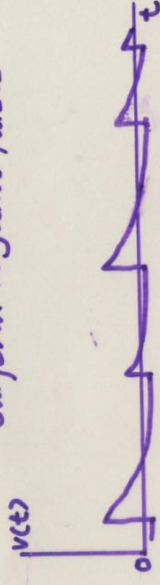
- studies and observations

3. Base-Line Restorer

Relevant when a train of pulses is considered.
Due to coupling capacitors.



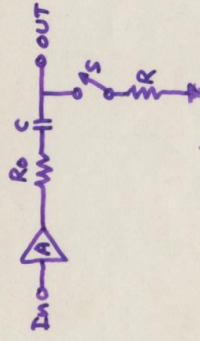
Uniform regular pulses



Random pulses

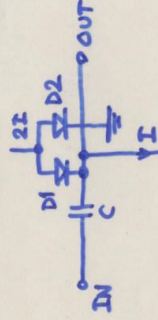
- Average d.c voltage to the right of 'c' in CR circuit is zero.
- If in the input it is not zero, then base line suppression occurs.
- More severe if the input pulse duty cycle is increased.
- Base line shift can be compensated in the first case more severe in the second case.
- One solution is to shape the input pulses in bipolar.
- Another is to d.c couple the elements of signal chain instead of coupling capacitors.
But complications due to amplifier offsets.
- So, the solution is base-line restoration.
To return to true zero of the base line between pulses in as short a time as possible.
- As a bonus, even low-frequency disturbances such as power-line hum and vibrational microphonics are reduced.

Equivalent circuit of Base-Line restorer.



R_0 = O/P impedance of $1k\Omega$
 opamp of gain $A=1$
 R = Equivalent resistance
 of $1k\Omega$ switch (such as diode)
 C = Coupling capacitance
 $\tau = RC$

- Many Complicated circuits used.
- BLS example from Dφ experiment.
- Expt. using L.B. Robinson's (1961) circuit.

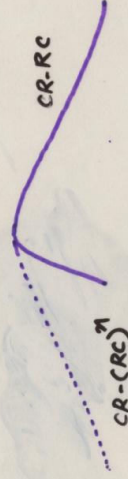


- circuit and observations

Fig.5

4. Semi-Gaussian shaper

- One CR, followed by many RC stages - $CR-(RC)^n$
- $n \approx 4$ would be enough to realise mathematical Gaussian shape.
- Best S/N can be obtained.
- Drawback: wide pulses 'pulse pile-ups'.



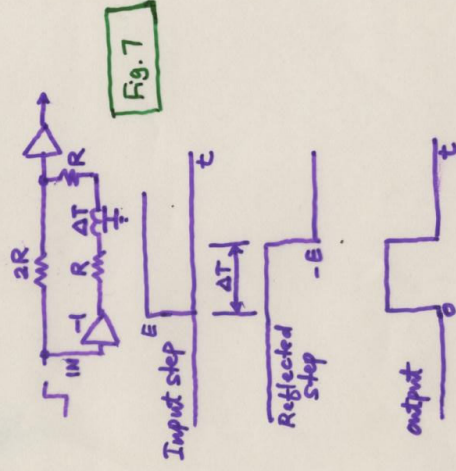
- circuit and observations.

Fig.6

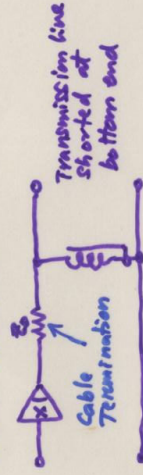
$$V_{out}(s) = \frac{V_0}{\tau^n (s + \tau)^{n+1}}$$

5. Delay-Line shaping

- Alternative to RC shaping
- Uses reflections from delay line
- Rise time of its input pulse unaltered, thus ideal for fast amplifier.



• Another Variation....



- Length of transmission line should be long enough compared to its rise time of its step voltage input, else ballistic deficit.
- Cables with low propagation velocity need to reduce long lengths.
- Often shapers are designed employing both CR-RC and delay-line shaping techniques.

Discriminators

- Frequently need to compare a signal with a reference
eg temperature control, light detection, DVM,...
basis of analogue to digital conversion $\rightarrow$ 1 bit

- Comparator

high gain differential amplifier,

difference between inputs sends output to saturation (+ or -)
could be op-amp - without feedback - or purpose designed IC

Sometimes ICs designed with open-collector output so add pull-up R to supply
also available with latch (memory) function

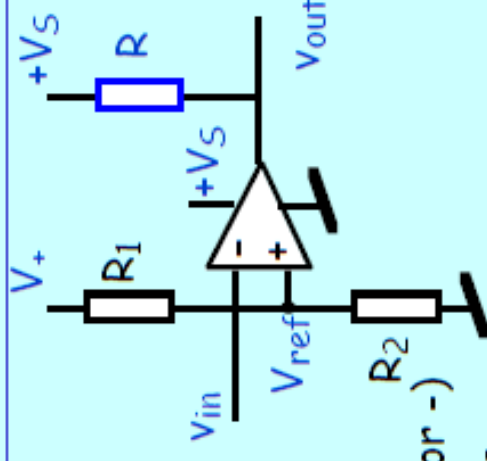
- NB

no negative feedback so $v_- \neq v_+$

saturation voltages may not reach supply voltages - check specs
speed of transition

- Potential problem

multiple transitions as signal changes near threshold



Hysteresis

- Add positive feedback (Schmitt trigger)

V_{ref} changes as $V_{out} \rightarrow +V_S$

ie threshold falls once transition is made preventing immediate fall positive feedback speeds transition

$$V_{out} = A(V_{ref} - V_-)$$

$$V_{ref} > V_- \Rightarrow V_{out} = V_S \quad V_{ref} = V_{high}$$

$$V_{ref} < V_- \Rightarrow V_{out} = 0V \quad V_{ref} = V_{low}$$

here, signal $\Rightarrow$ logical "1": $V_{out} = 0V$

- Output depends on history

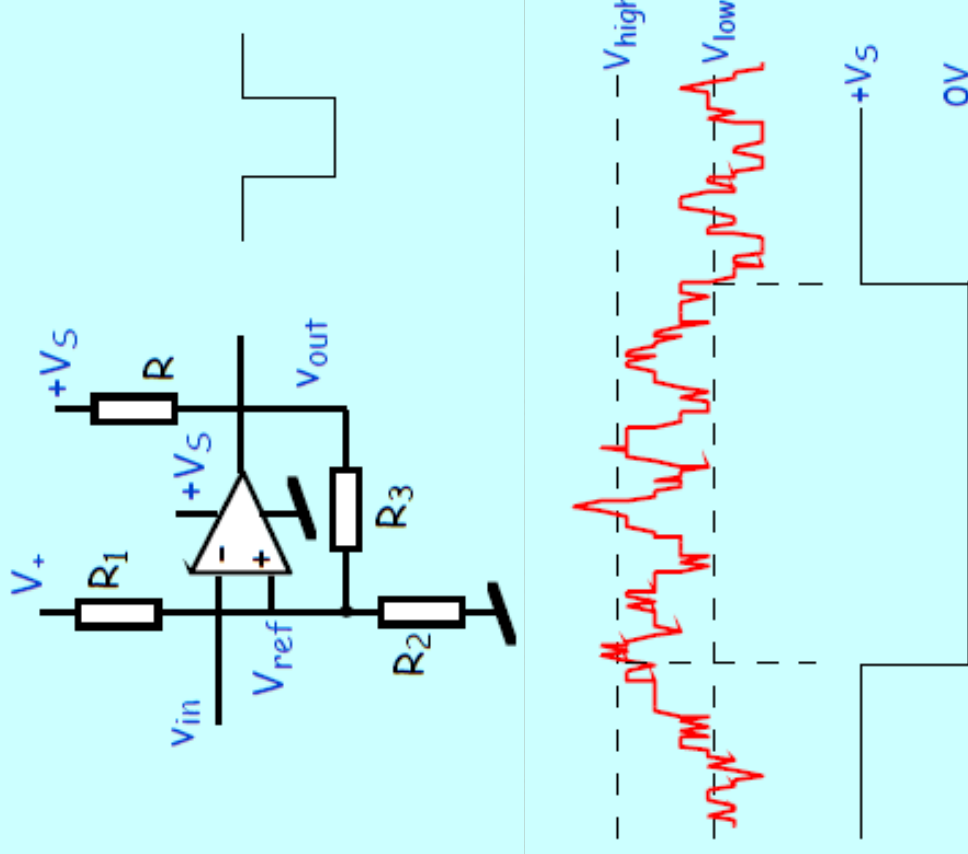
eg $V_+ = 10V$, $V_S = +5V$, $0V$

$$R_1 = 10k\Omega, R_2 = 10k\Omega, R_3 = 100k\Omega$$

$$V_{out} = 0V, V_{ref} = 4.76V$$

$$V_{out} = 5V, V_{ref} = 5V$$

$$\text{hysteresis} = \Delta V_{ref} = 0.24V$$



Considerations for discriminators

- Two common problems
 - Walk
 - Jitter
- Time-Pickoff methods
 - Leading edge triggering
 - Fast zero-crossing triggering
 - Constant fraction triggering
 - Amplitude and risetime compensated triggering

Timewalk and jitter

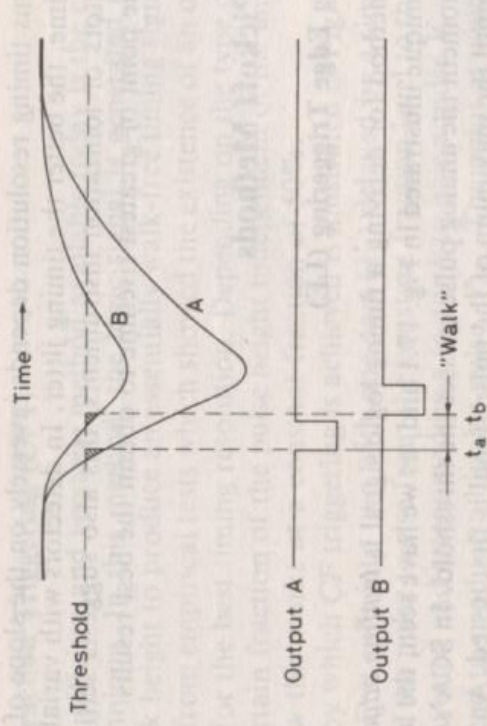
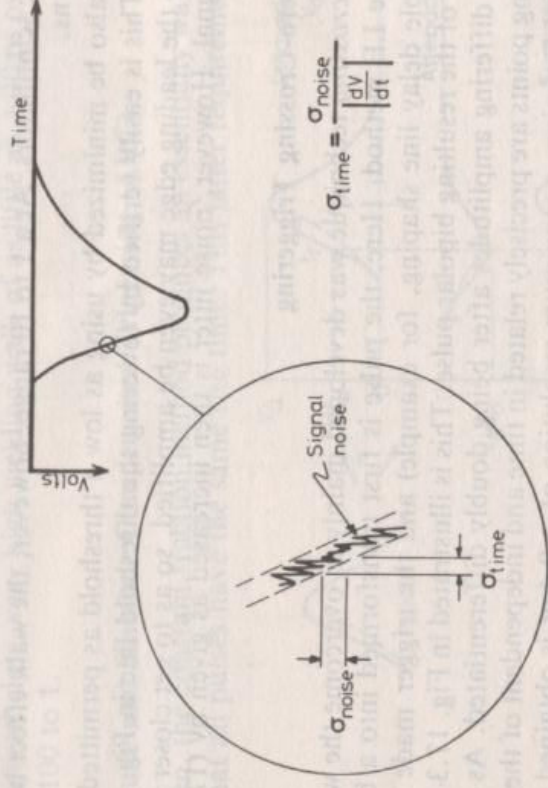


Fig. 17.1. *Walk* in a discriminator or SCA. Coincident signals with different amplitudes cross the threshold at different times. An additional *walk* effect occurs because of the finite charge which must be integrated on a capacitor to trigger the discriminator or SCA



$$\sigma_{\text{time}} = \frac{\sigma_{\text{noise}}}{\left| \frac{dV}{dt} \right|}$$

Zero-crossing and Constant fraction

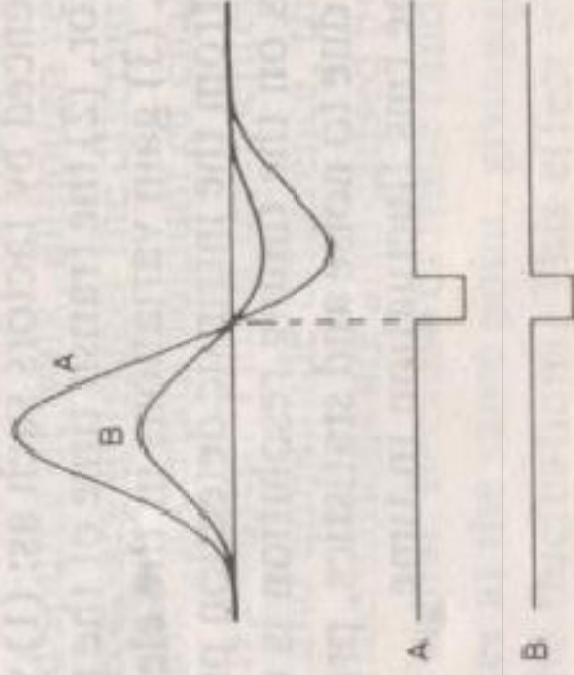


Fig. 17.3. Zero-crossing timing.
Variations in the cross-over point
are known as *zero-crossing walk*

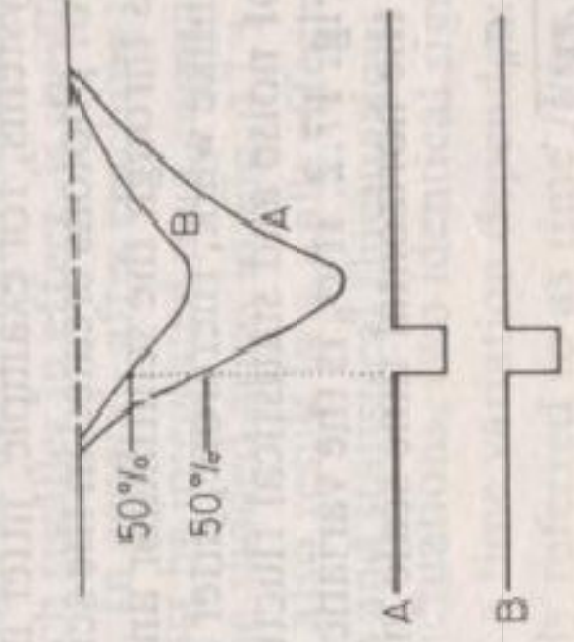


Fig. 17.4. Constant fraction discrimination

CF and ARC triggering

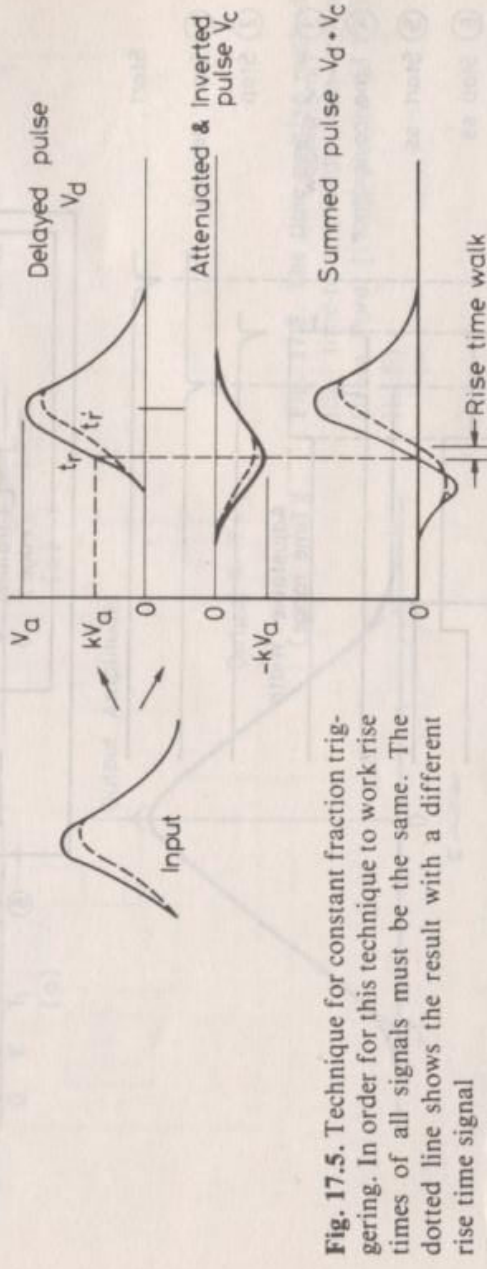


Fig. 17.5. Technique for constant fraction triggering. In order for this technique to work rise times of all signals must be the same. The dotted line shows the result with a different rise time signal

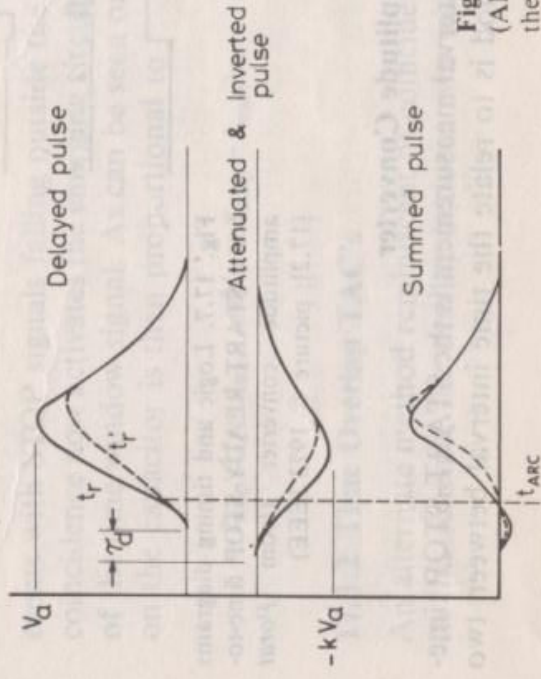
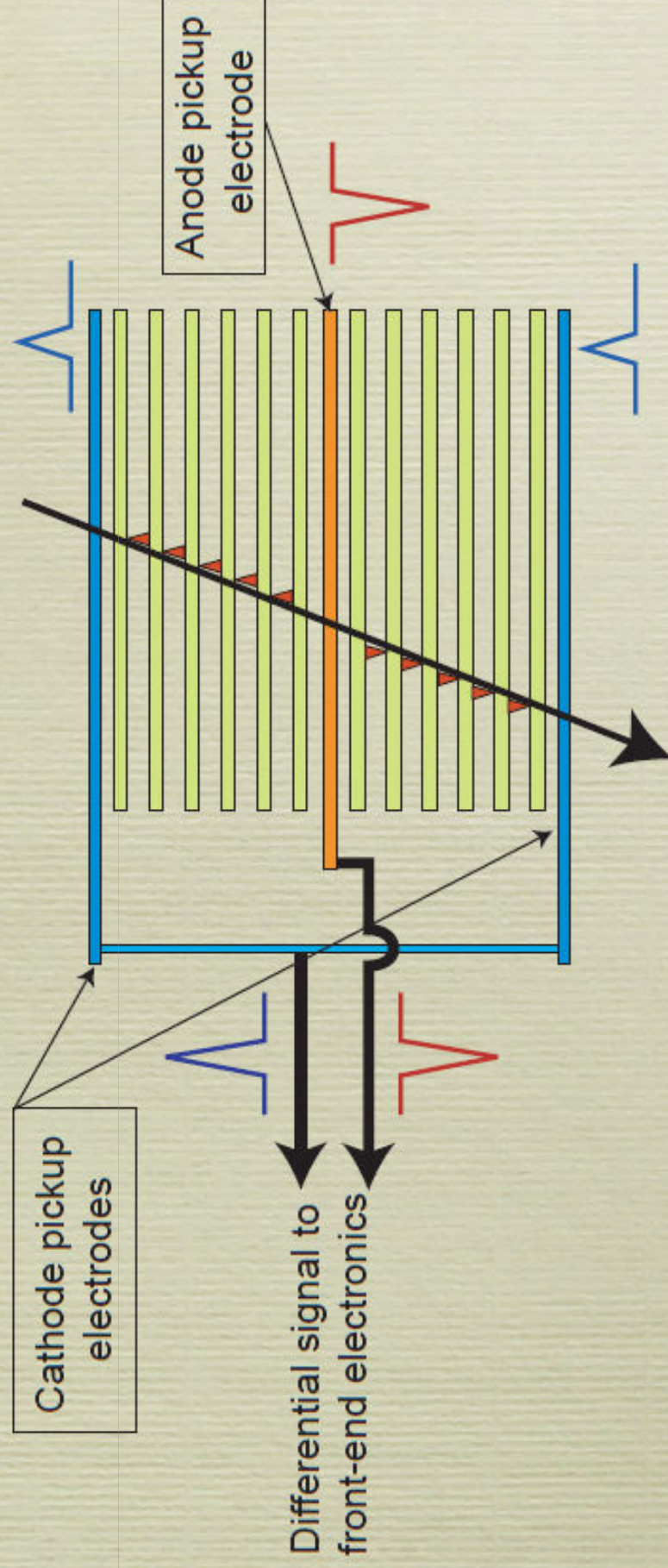


Fig. 17.6. Amplitude and risetime compensation (ARC) triggering. The zero-crossover occurs before the signal peak is reached

ALICE-TOP RPC signal

ALICE-TOP has 10 gas gaps, each of 250 micron width
Built in the form of strips, each with an active area of $120 \times 7 \text{ cm}^2$,
readout by 96 pads (each $2.5 \times 3.5 \text{ cm}^2$)

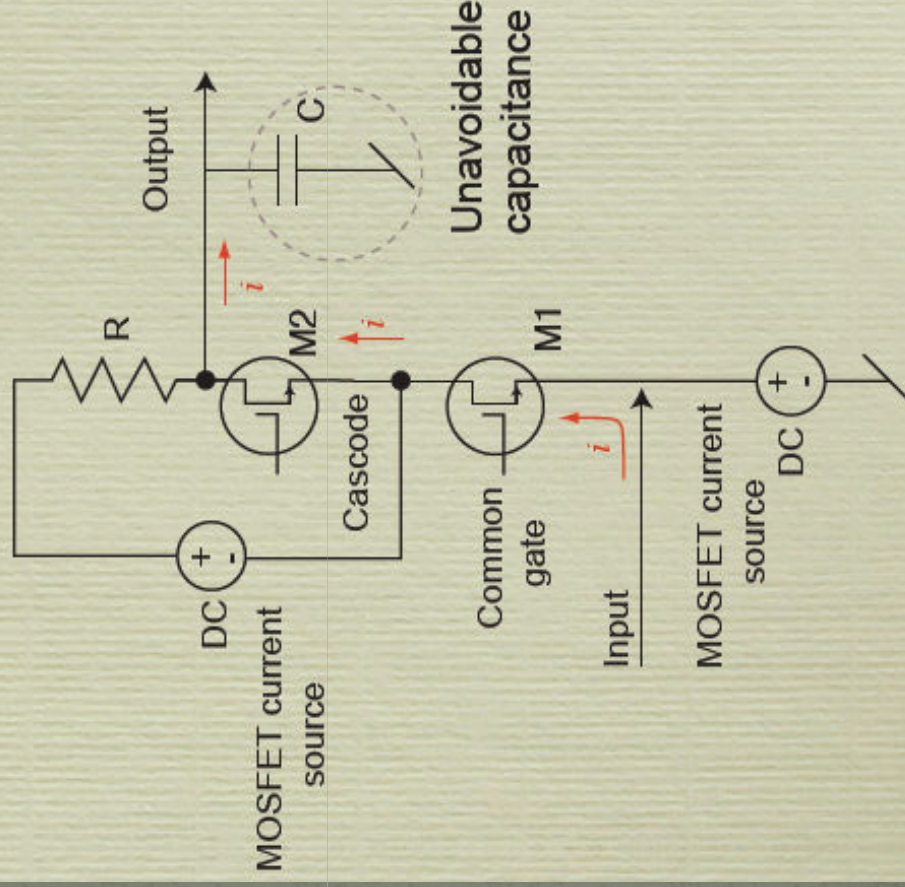


The NINO ASIC

- Time-over-threshold measurement of input charge
- Amplifier+discriminator+time-over-threshold ASIC
- 0.25 μm CMOS technology
- Differential input
- Designed to be coupled to transmission line
- Fast (1 nS peaking time) to minimise jitter
- Differential design throughout to minimise cross-talk
- Low power (less than 50mW/channel was the target)

NINO Input stage

1/2 of input circuit



- o The input current flows through the two transistors and charges the capacitor at the output (need to minimise C for maximum voltage)
- o Trailing-edge of voltage pulse at output has RC time constant
- o The impedance seen at the input is mainly the $1/g_m$ of the input transistor.
- o The advantage of this configuration is the high bandwidth with excellent stability due to the absence of feedback element.

Low frequency feedback to control offset and threshold control

The diagram illustrates a 4-stage high-bandwidth amplifier. It is divided into three main functional blocks: an input stage, a 4-stage high-bandwidth amplifier, and an LVDS output driver.

Input stage: This block includes an input differential pair (M1, M2) with a tail current source (M5). The inputs are labeled $in+$ and $in-$. Biasing is provided by $BiasN1$, $BiasN2$, and $BiasN3$. The output of the input stage is connected to the first stage of the main amplifier.

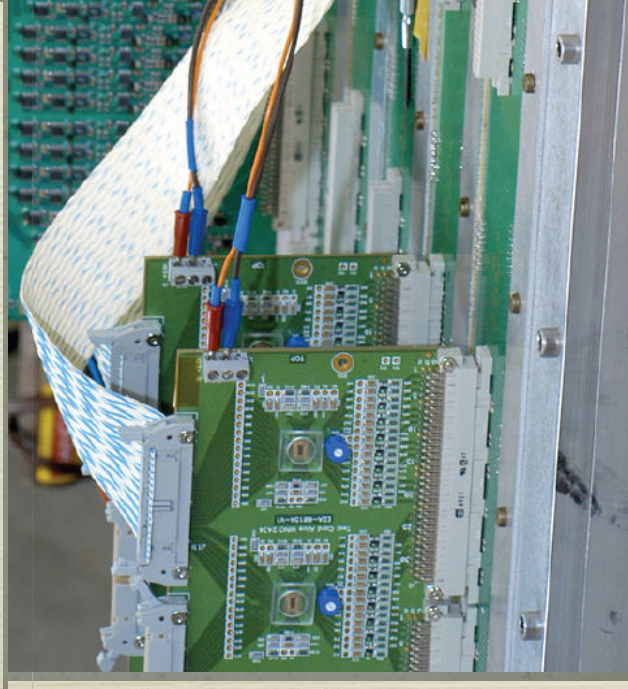
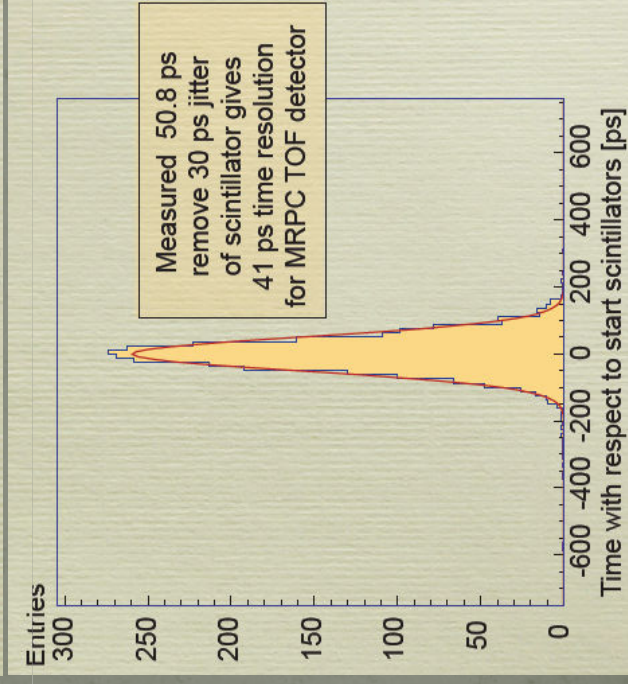
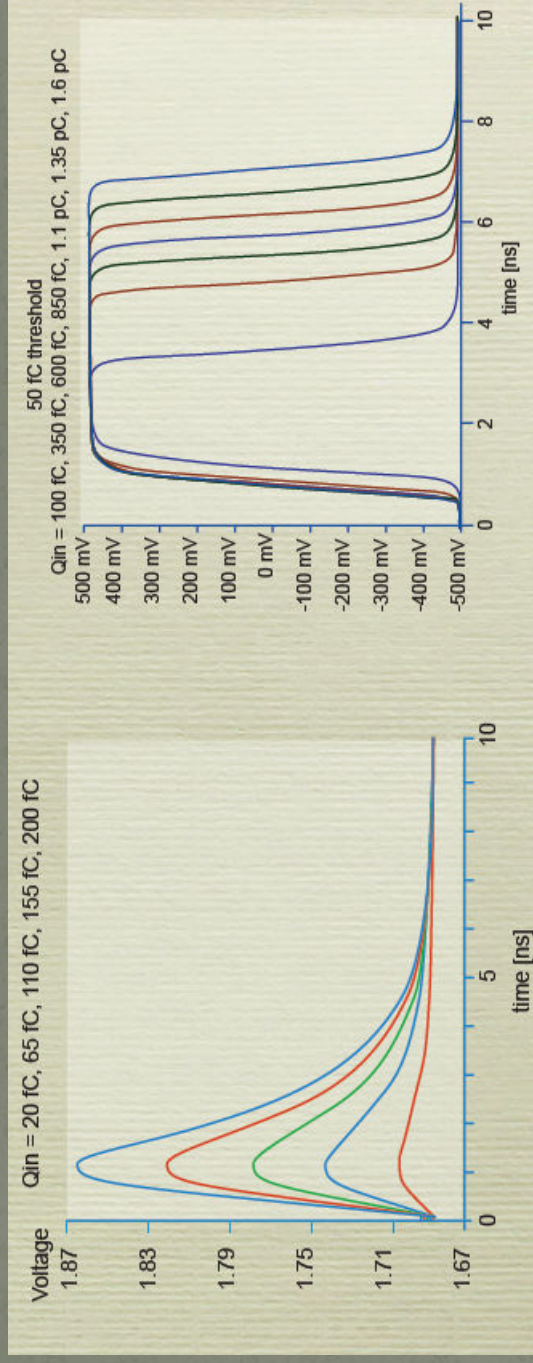
4 stage high-bandwidth amplifier: This block consists of four identical stages. Each stage is a differential pair (M7, M8) with a tail current source (M5) and a load resistor (R3). The stages are biased by $BiasN4$, $BiasN5$, and $BiasN6$. The output of the fourth stage is connected to the LVDS output driver.

LVDS output driver: This block includes a differential pair (M23, M24) with a tail current source (M25) and a load resistor (R13). The output is connected to the LVDS output driver, which is labeled "LVDS output driver".

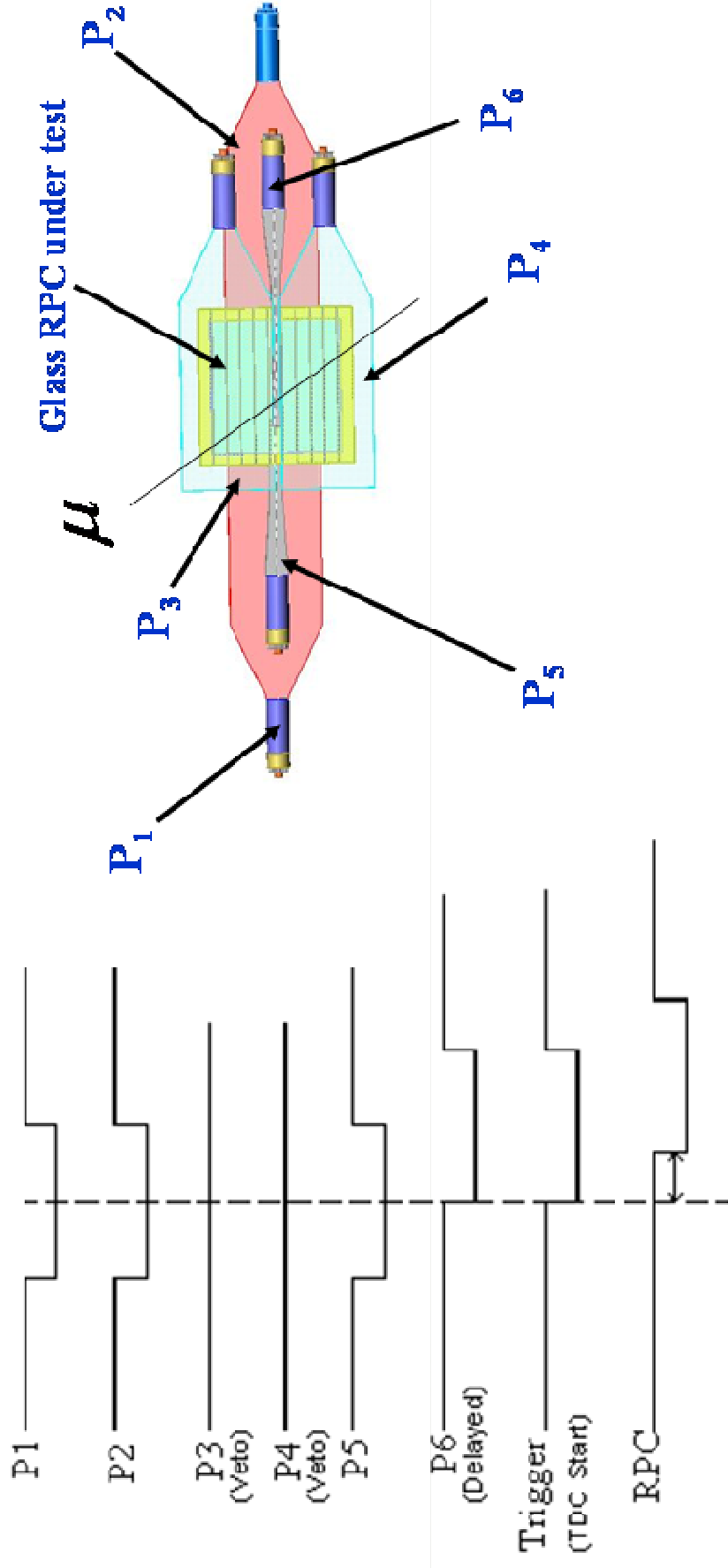
Hysteresis: A hysteresis circuit is shown, consisting of a differential pair (M21, M22) with a tail current source (M23) and a load resistor (R13). The output is connected to the input of the input stage.

Other components: The circuit includes various biasing points (BiasP1, BiasP2, BiasN1, BiasN2, BiasN3, BiasN4, BiasN5, BiasN6), threshold points (Th+, Th-), and a low-frequency feedback path (C1a, C1b) to control offset and threshold control.

Performance of NINO

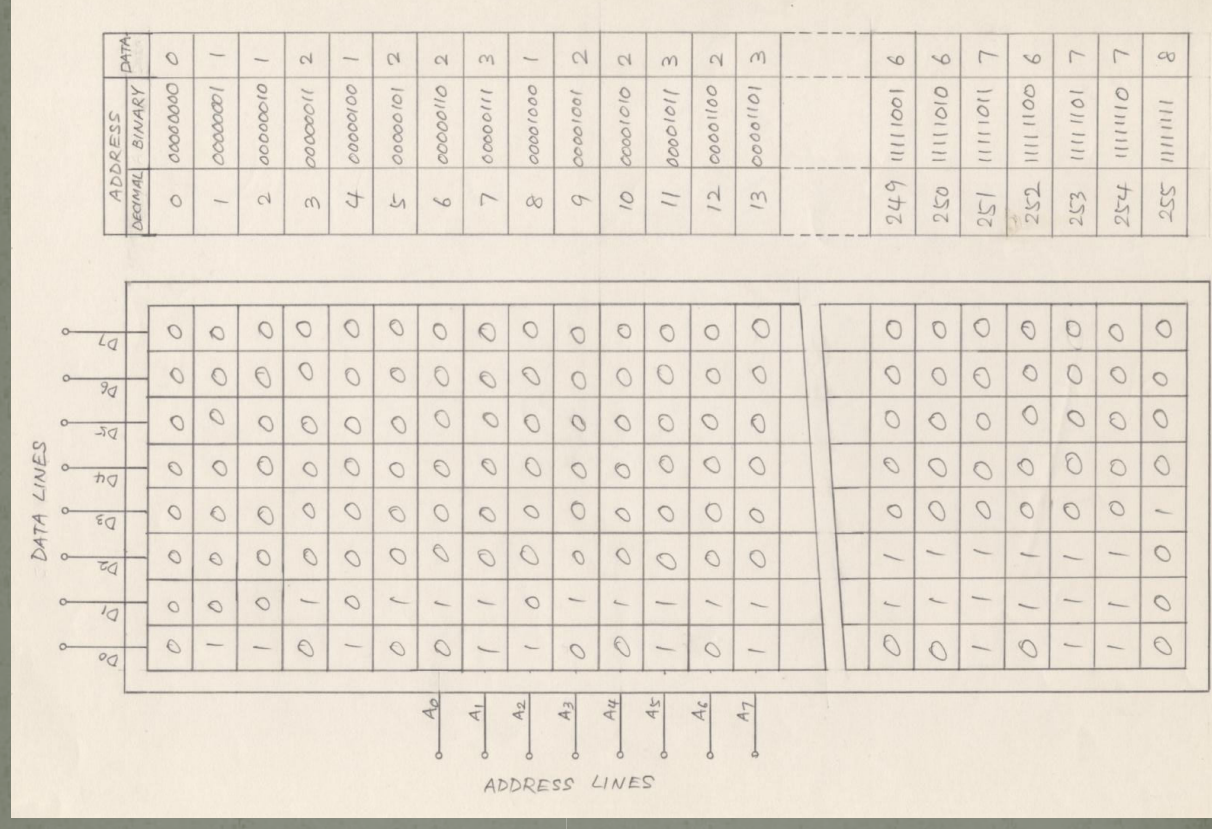


Coincidence scheme for cosmic telescope



$$\text{Muon Trigger} = P_1 \bullet P_2 \bullet \overline{P_3} \bullet \overline{P_4} \bullet P_5 \bullet P_6$$

Memory-lookup table



Part-III

Friday, February 20, 2009

Acknowledgements & References: G.Hall, W.R.Leo, Jörgen Christiansen, GRAPES collaboration , Ortec, P.Horowitz & W.Hill, C.F.G.Delaney

Analogue to Digital Conversion

- Turns electrical input (voltage/current) into numeric value
- Parameters and requirements
 - Resolution
 - the granularity of the digital values
 - Integral Non-Linearity
 - proportionality of output to input
 - Differential Non-Linearity
 - uniformity of digitisation increments
- Conversion time
 - how much time to convert signal to digital value
- Count-rate performance
 - how quickly a new conversion can begin after a previous event
- Stability
 - how much values change with time

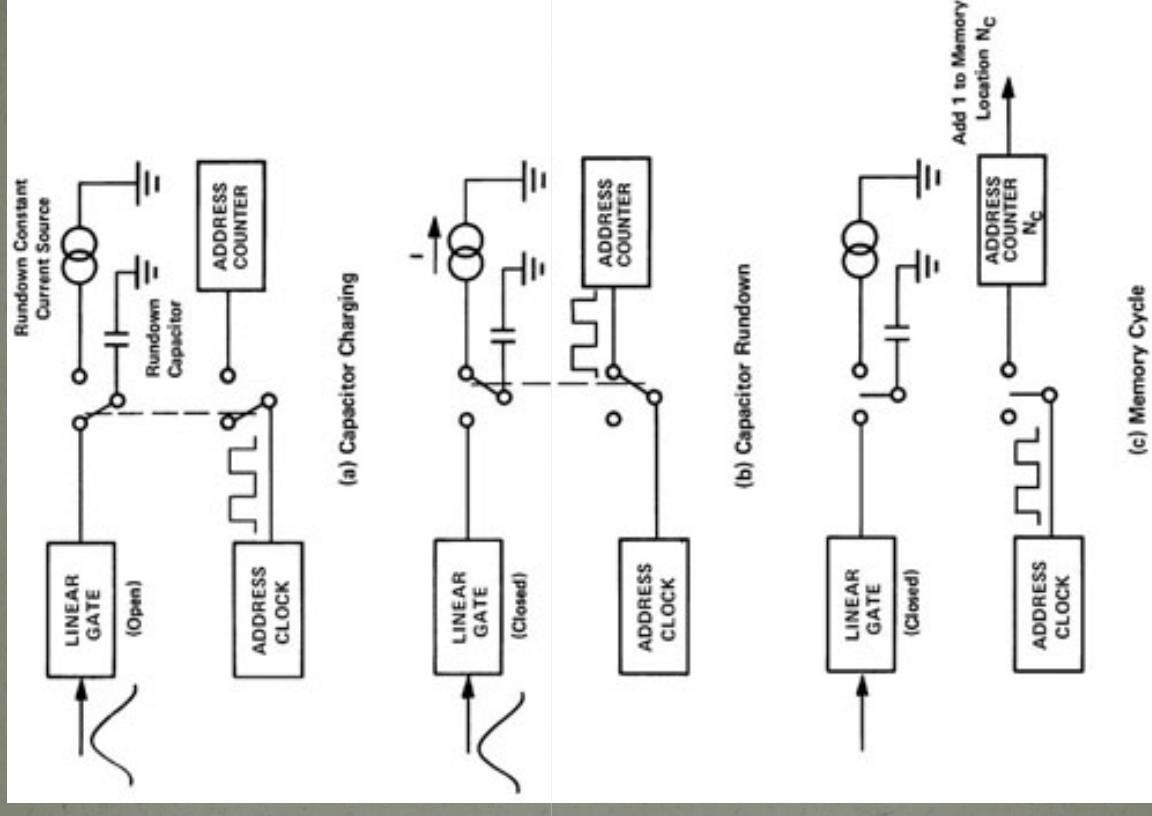
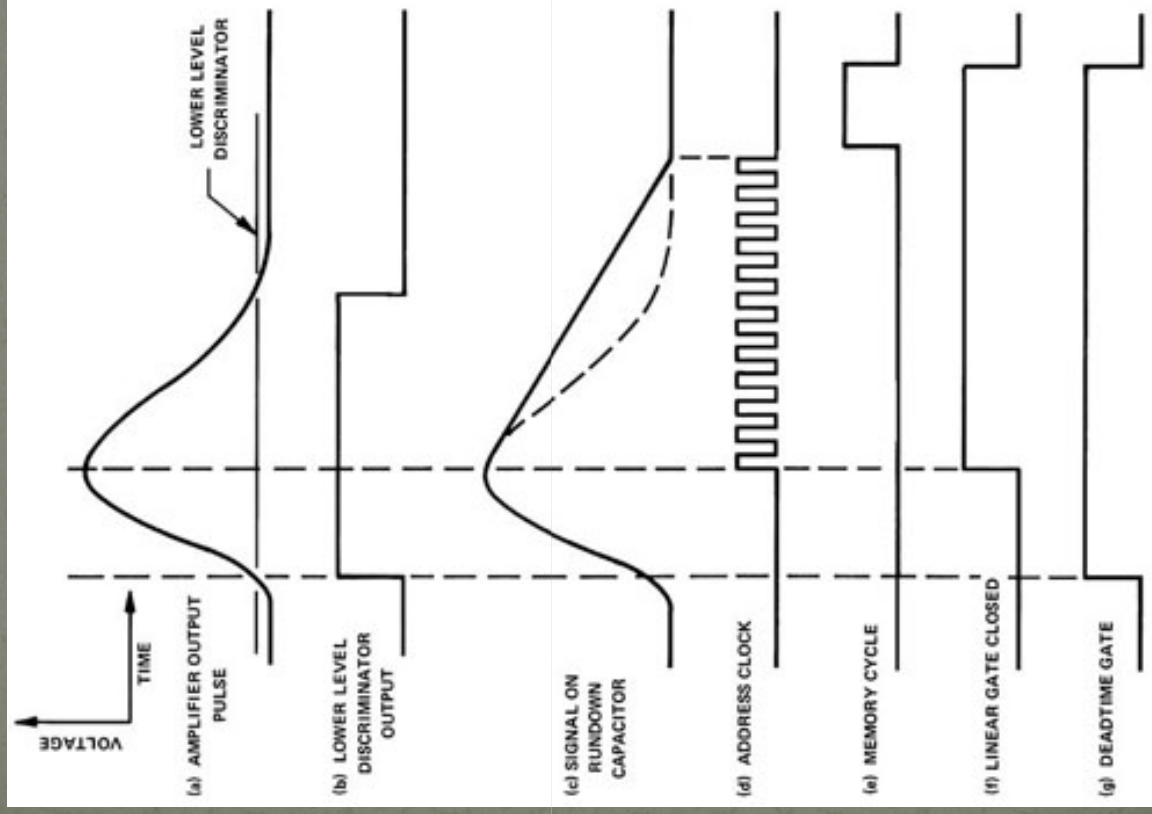
Analog-to-Digital Converters (ADCs)

- Peak-sensing
 - Maximum of the voltage signal is digitised
 - Ex: Signal of the PMT in voltage mode (slow signals, already integrated)
- Charge sensitive
 - Total integrated current digitised
 - Ex: Signal of the PMT in the current mode (fast signals)
- Time of integration or the time period over which the ADC seeks a maximum is determined by the width of the gate signal

Types of ADCs

- Ramp or Wilkinson
- Successive approximation
- Flash or parallel
- Sigma-delta ADC
- Hybrid (Wilkinson + successive approximation)
- Tracking ADC
- Parallel ripple ADC
- Variable threshold flash ADC
- ...

Ramp or Wilkinson ADC



Successive approximation ADC

- analogous to binary search

generate $V_{\text{ref}} = \Delta V \times (2^{N-1}, 2^{N-2}, \dots, 2^0)$ in N steps

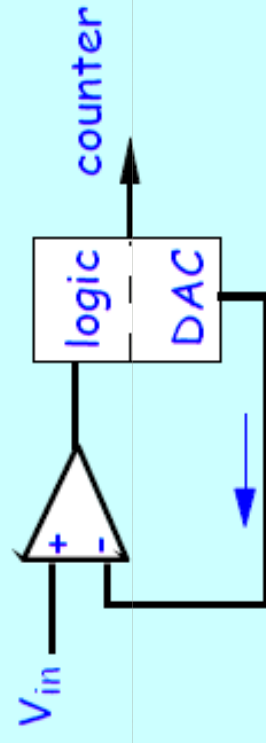
set bit = 1
if $V_{\text{in}} > V_{\text{ref}}$
leave
else bit = 0

- Pros

speed $\sim \mu\text{sec}$
high resolution

- Cons

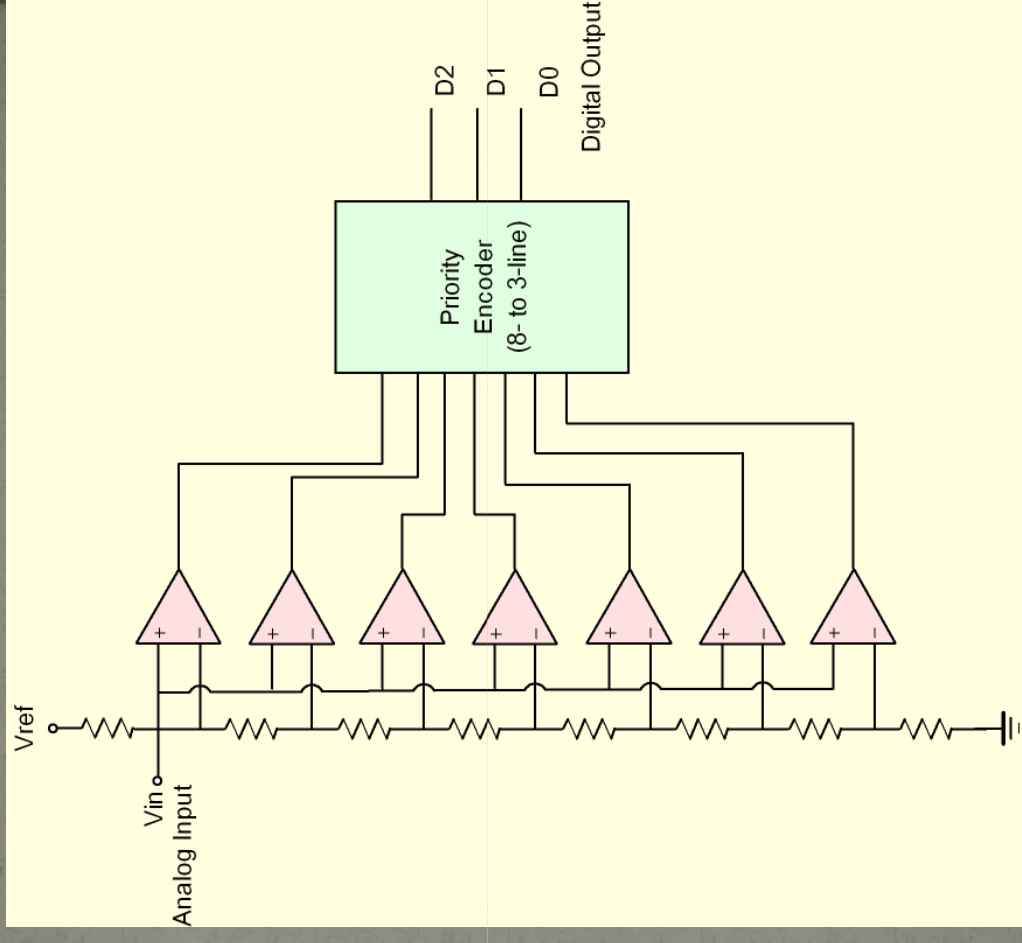
DNL 10-20%
very precise resistors required with DAC for V_{ref}



DAC = digital to
analogue converter
ie number $\rightarrow$ voltage

Flash or parallel ADC

- Flash ADC is the fastest ADC type available. The digital equivalent of the analog signal will be available right away at its output – hence the name “flash”.
- The number of required comparators is 2^{n-1} , where n is the number of output bits.
- Since Flash ADC comparisons are set by a set of resistors, one could set different values for the resistors in order to obtain a non-linear output, i.e. one value would represent a different voltage step from the other values.



Sigma-delta ADC

- Digitise the signal with 1-bit resolution at a high sampling rate (MHz).
useful for high resolution conversion of low-frequency signals, to 20bits
low-distortion conversion of audio signals
good linearity and high accuracy.

• Operation - At $t = 0$, assume $V_{ref} = 0$

V_{out} high

integrator charges -ve

at rate $\sim V_{in}$

comparator flips

counter goes low

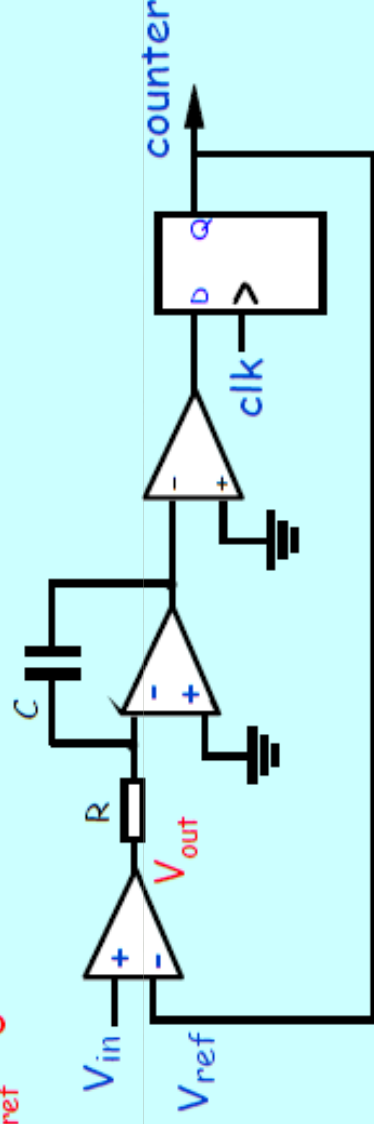
clock increments... etc,...

$V_{in} = 0 \Rightarrow \text{output} = 000000...$

$V_{in} = (1/2)V_{in}(\text{max}) \Rightarrow \text{output} = 101010...$

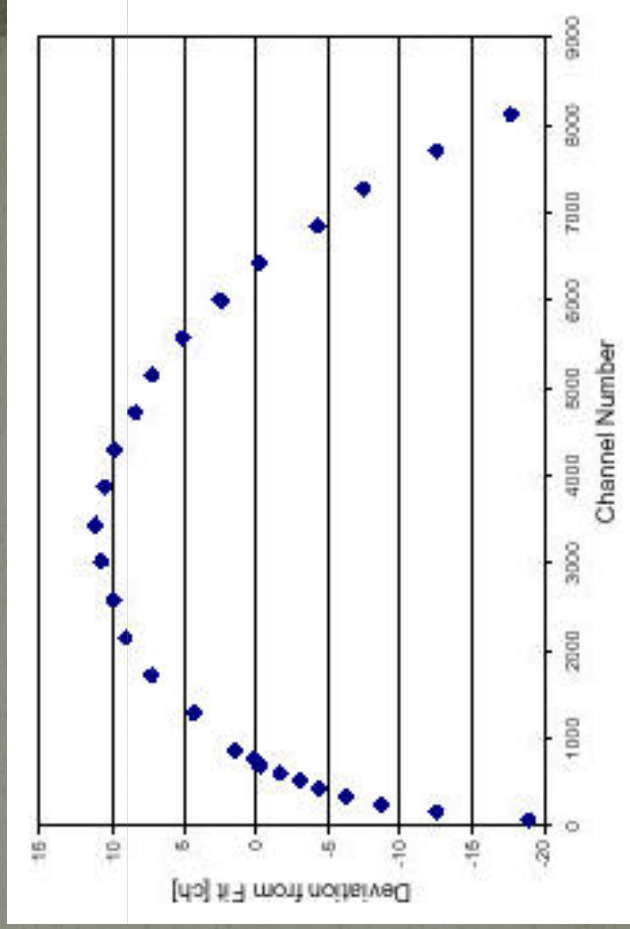
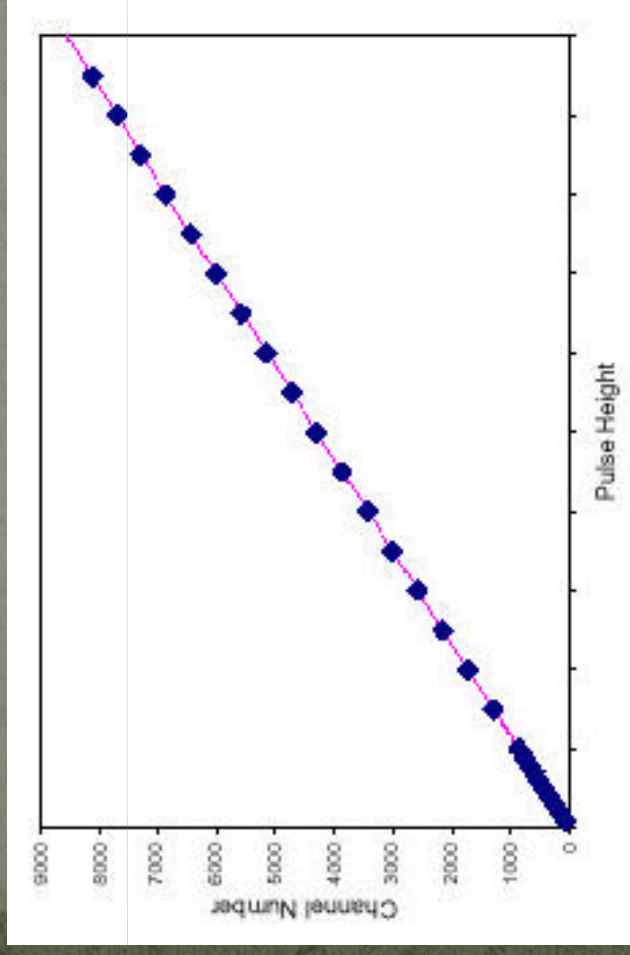
$V_{in} = V_{in}(\text{max}) \Rightarrow \text{output} = 111111...$

the higher the input voltage, the more 1's at the serial digital output.



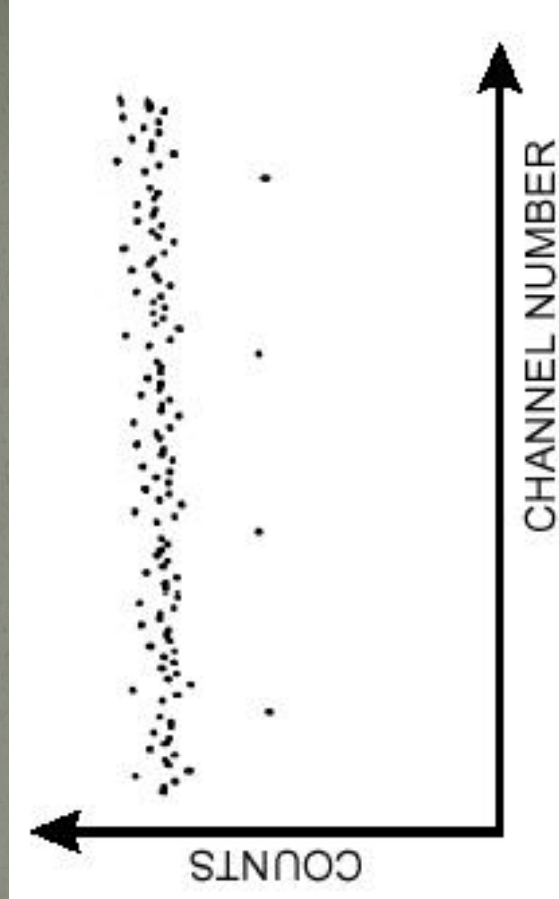
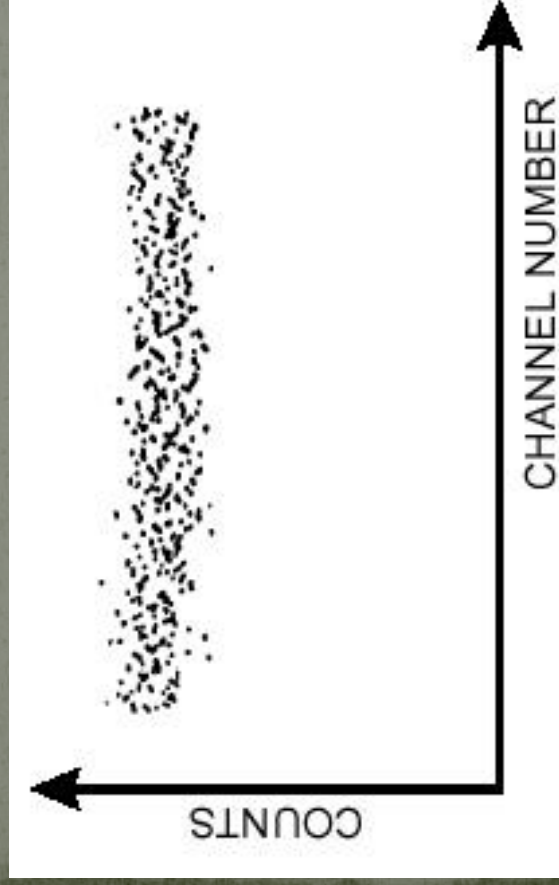
Integral non-linearity

- Output value D should be linearly proportional to V
- Check with plot
- For more precise evaluation of INL fit to line and plot deviations
- Plot $D_i - D_{\text{fit}}$ vs n_{chan}



Differential non-linearity

- Measures non-uniformity in channel profiles over range
$$\text{DNL} = \text{DV}_i / \langle \text{DV} \rangle - 1$$
$$\text{DV}_i = \text{width of channel } i$$
$$\langle \text{DV} \rangle = \text{average width}$$
- RMS or worst case values may be quoted
$$\text{DNL} \sim 1\% \text{ typical but } 10^{-3} \text{ can be achieved}$$
can show up systematic effects, as well as random

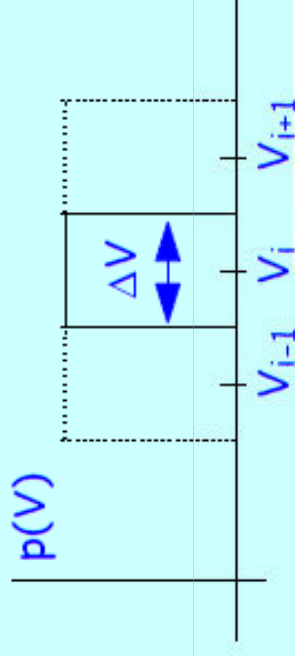


Resolution

- To convert an analogue value, eg voltage, to digital two parameters are required
range and number of bits

quantum = $\Delta V = (V_{\max} - V_{\min}) * 2^{-N}$ referred to as 1LSB (least significant bit)

- eg 10 bits = $2^{10} = 1024$, $V_{\max} - V_{\min} = 1V \Rightarrow \Delta V = 1V/1024 \approx 1mV$

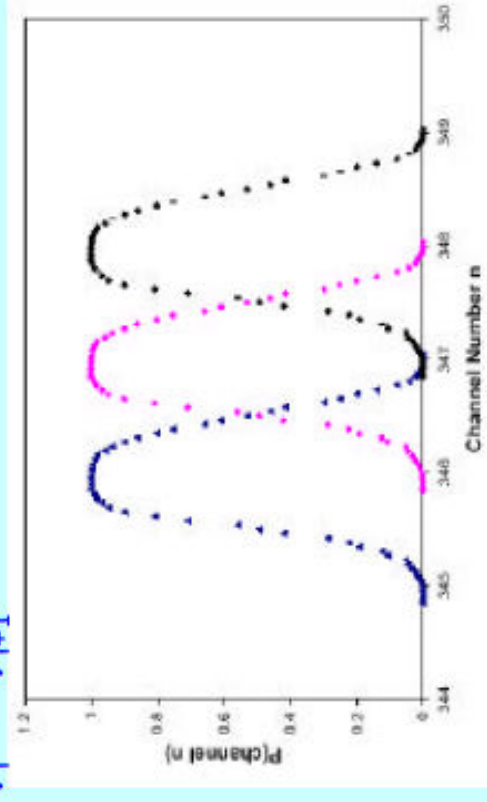


- Ideal ADC behaviour
probability vs amplitude

- Real ADC behaviour

noise in digitisation process
smears resolution

$$\sigma_{\text{noise}} < \Delta V/4$$



Other variables

- Conversion time
 - finite time is required for conversion and storage of values
 - may depend on signal amplitude
 - gives rise to dead time in system
 - i.e. system cannot handle another event during dead time
 - may need accounting for, or risk bias in results
- Rate effects
 - results may depend on rate of arrival of signals
 - typically lead to spectral broadening
- Stability
 - temperature effects are a typical cause of variations
- A partial solution to most of these problems is regular calibration, preferably under real operating conditions, as well as control of variables

Non-linear ADC

- A integrating system for measuring x-ray photons for crystallography, measuring spots. The most intense spots contain up to $\sim 10^9$ photons, the weakest just a few.

Measure N in spot

aim: achieve 1% resolution
using a 10-bit ADC (cost)

assume 1V range

1V = largest signal, defines G_1

$N < 10^4$ $\sigma(N)/N > 1\%$

defines smallest signals

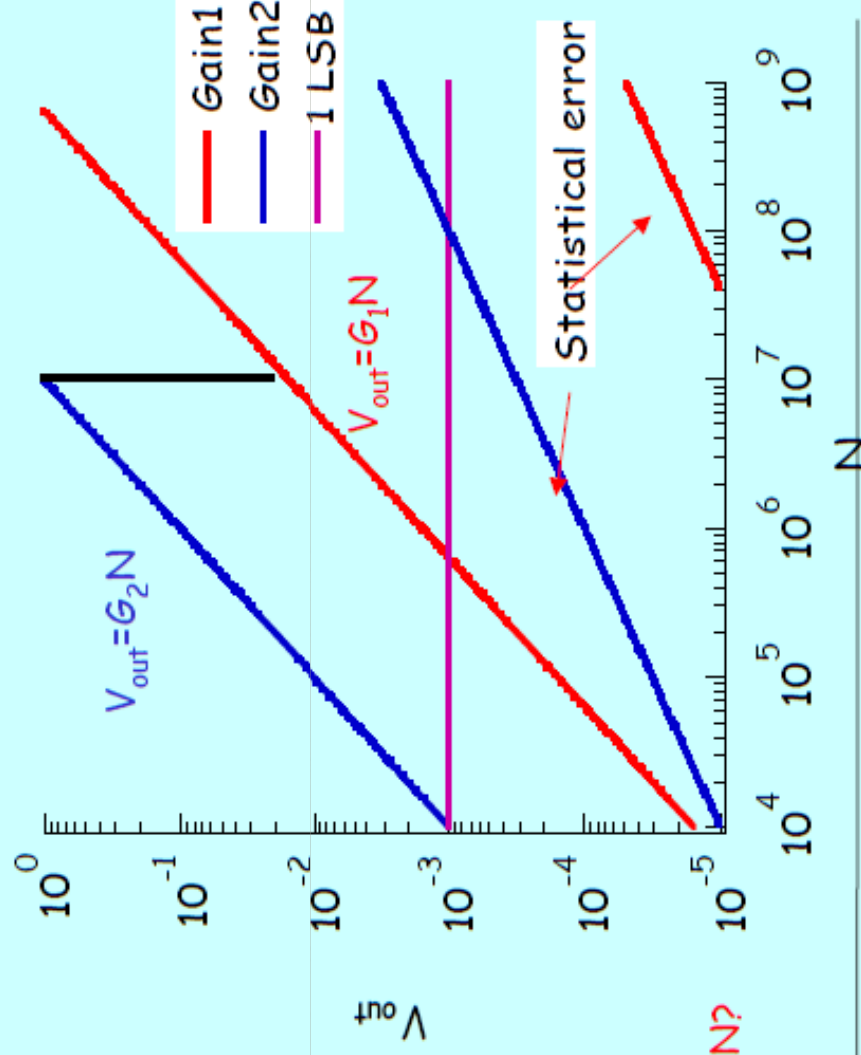
but ADC LSB $>$ signal

Increase small signal gain G_2

Select output in ADC range

• Is 1% resolution achieved for all N ?

If not... ?



Why TDCs?

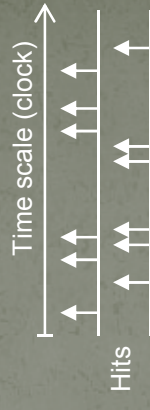
TDCs are used to measure time or intervals

- Start – Stop measurement
 - Measurement of time interval between two events:
Start signal – Stop signal
 - Used to measure relatively short time intervals with high precision
 - Like a stop watch used to measure sport competitions



• Time tagging

- Measure time of occurrence of events with a given time reference:
Time reference (Clock)
Events to be measured (Hits)
- Used to measure relative occurrence of many events on a defined time scale:
Such a time scale will have limited range; like 12/24 hour time scale on your watch when having no date and year



Where TDCs?

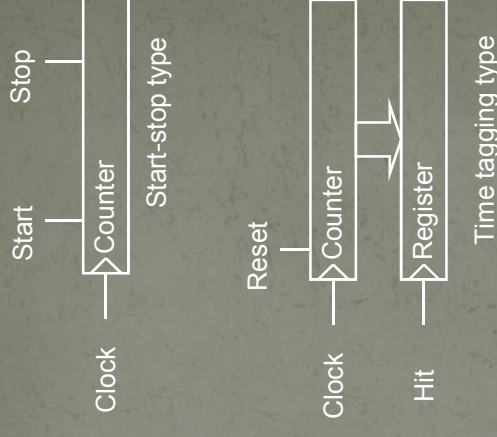
- Special needs for High Energy Physics
 - Many thousands of channels needed
 - Rate of measurements can be very high
 - Very high timing resolution
 - A mechanism to store measurements during a given interval and extract only those related to an interesting event, signaled by a trigger, must be integrated with TDC function
- Other applications
 - Laser/radar ranging to measure distance between cars
 - Time delay reflection to measure location of broken fiber
 - Most other applications only needs one or a few channels

How to compare TDCs?

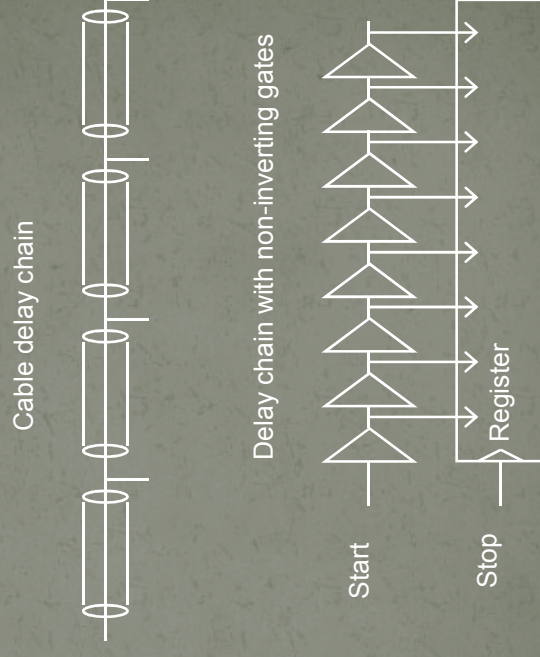
- Merits
 - Resolution
 - Bin size and effective resolution (RMS, INL, DNL)
 - Dynamic range
 - Stability
 - Use of external reference
 - Drift (e.g. temperature)
 - Jitter and Noise
 - Integration issues
 - Digital / analog
 - Noise / power supply sensitivity
 - Sensitivity to matching of active elements
 - Required IC area
 - Common timing block per channel
 - Time critical block must be implemented on chip together with noisy digital logic
- Use in final system
 - Can one actually use effectively very high time resolution in large systems (detectors)
 - Calibration - stability
 - Distribution of timing reference (start signal or reference clock)
 - Other features: data buffering, triggering, readout, test, radiation, etc.

Basic TDC types - I

- Counter type
- Advantages
 - Simple; but still useful!
 - Digital
 - large dynamic range possible
 - Easy to integrate many channels per chip
- Disadvantages
 - Limited time resolution (ins using modern CMOS technology)
 - Meta stability (use of Gray code counter)



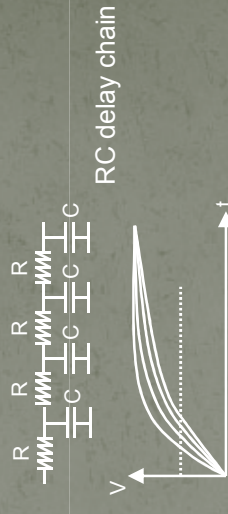
- Single Delay chain type
- Cable delay chain (distributed L-C)
 - Very good resolution (5ps mm)
 - Not easy to integrate on integrated circuits
- Simple delay chain using active *gates*
 - Good resolution (~100ps using modern tech)
 - Limited dynamic range (long delay chain and register)
 - Only start-stop type
 - Large delay variations between chips and with temperature and supply voltage



Counter-type TDC

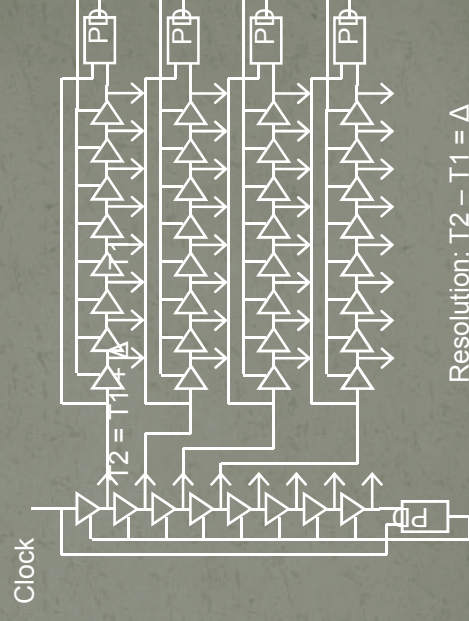
Basic TDC types - II

- Single Delay chain type (Contd ...)
 - Delay locked loop
 - Self calibrating using external frequency reference (clock)
 - Allows combination with counter
 - Delicate feedback loop design (jitter)
 - R-C delay chain
 - Very good resolution
 - Signal slew rate deteriorates
 - Delay chain with losses; so only short delay chain possible
 - Large sensitivity to process parameters (and temperature)



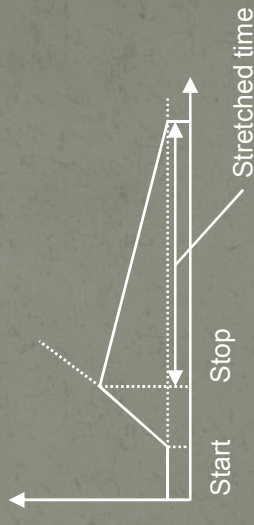
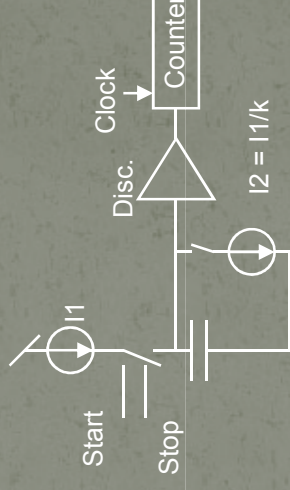
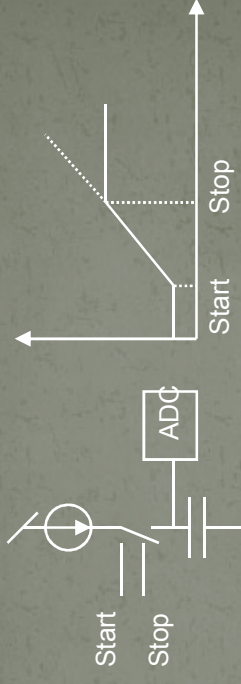
Basic TDC types - III

- Multiple delay chain type
 - Vernier delay chain types
 - Resolution determined by delay difference between two chains. Delay difference can be made very small and very high resolution can be obtained.
 - Small dynamic range (long chains)
 - Delay chains can not be directly calibrated using DLL
 - Matching between delay cells becomes critical
- Coupled delay locked loops
 - Sub-delay cell resolution ($\frac{1}{4}$)
 - All DLLs use common time reference (clock)
 - Common timing generator for multiple channels
 - Jitter analysis not trivial

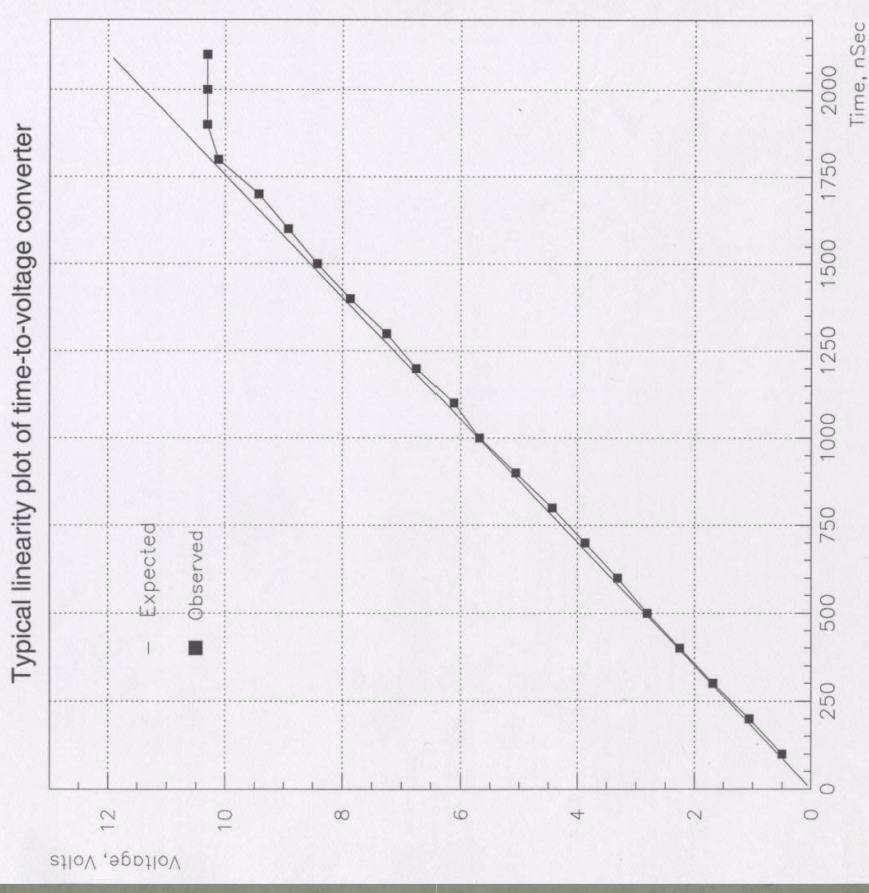
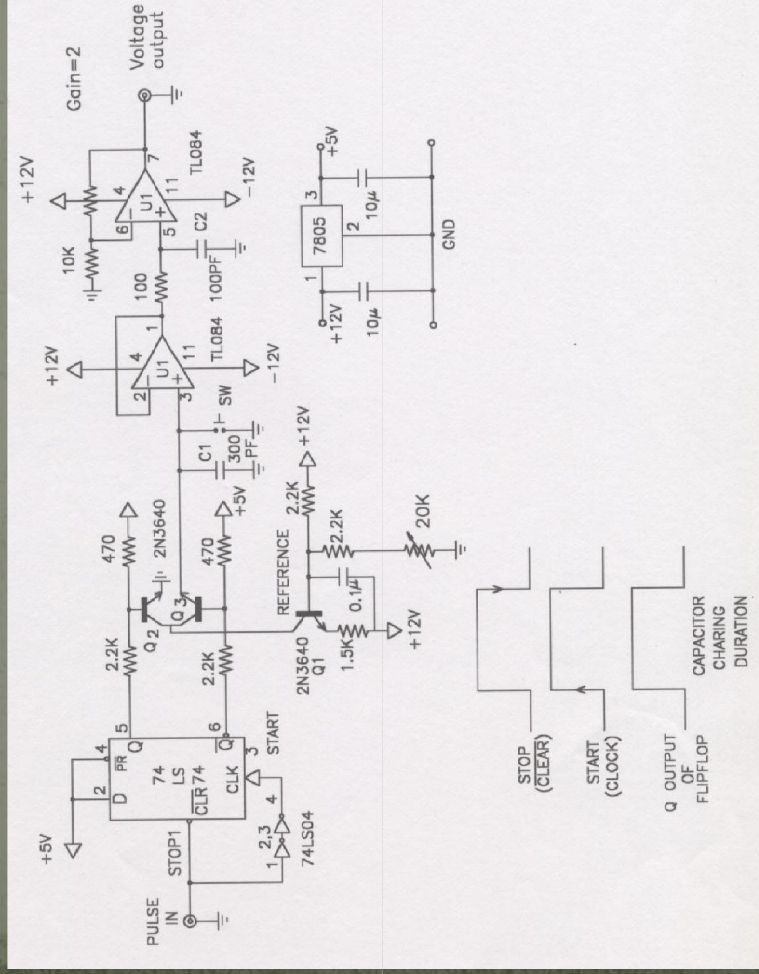


Basic TDC types - IV

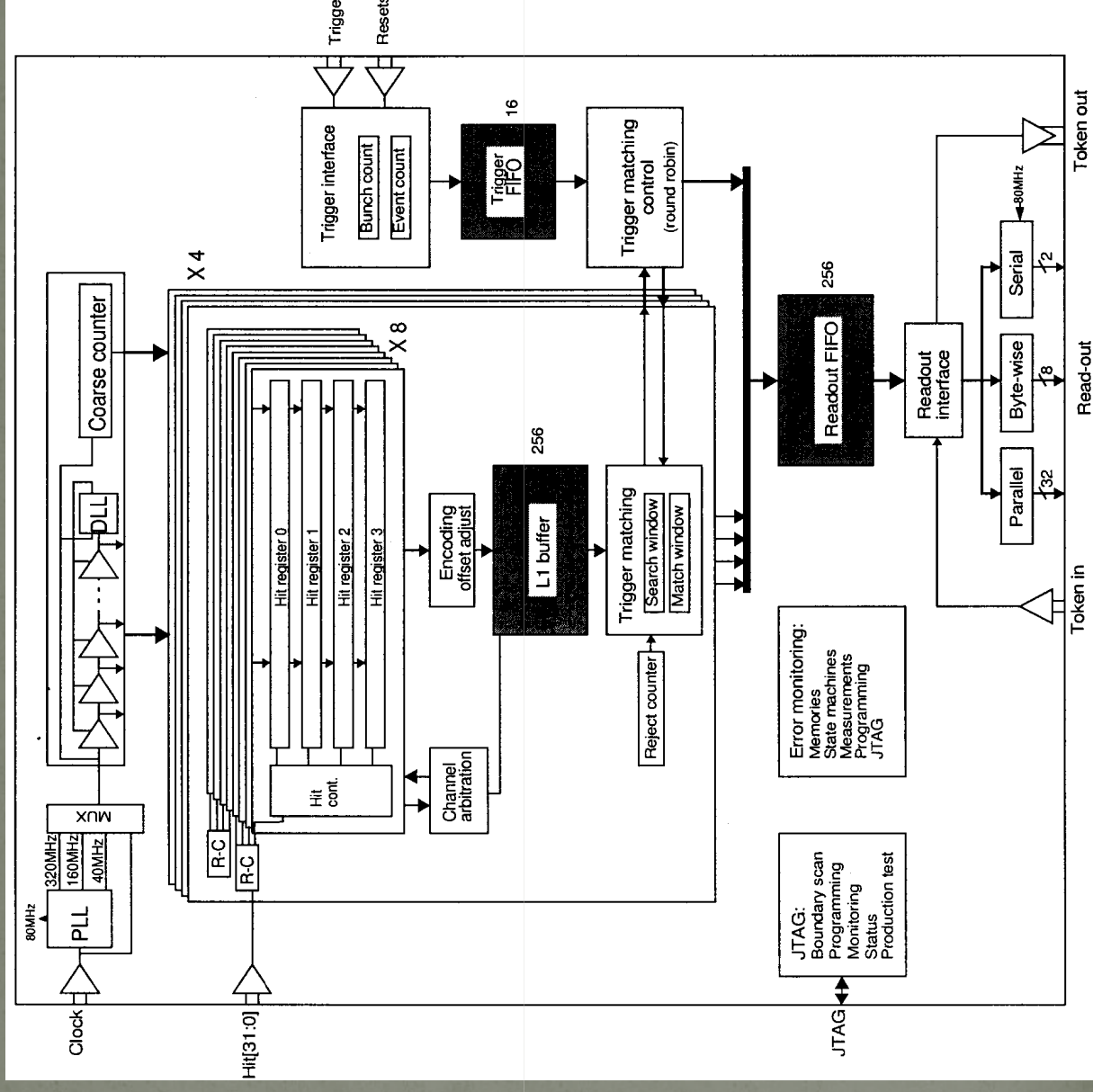
- Charge integration
 - Using ADC (TAC)
 - High resolution
 - Low dynamic range
 - Sensitive analog design
 - Low hit rate
 - Requires ADC
 - Using double slope (time stretcher)
 - No need for ADC (substituted with a counter)
- Multiple *exotic* architectures
 - Heavily coupled phase locked loops
 - Beating between two PLLs
 - Re-circulating delay loops
 - Summing of signals with different slew rates



Time-to-Amplitude Converter(TAC)

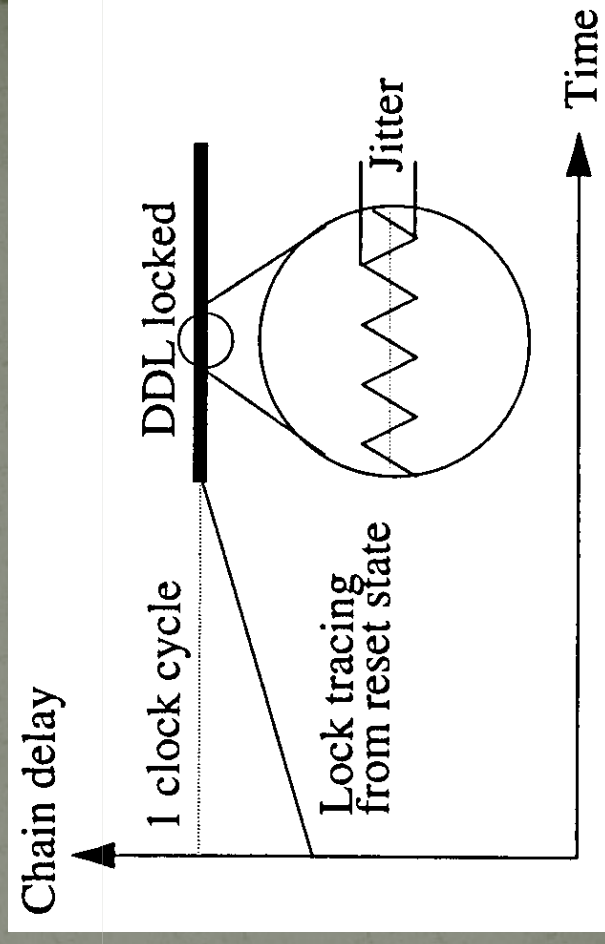
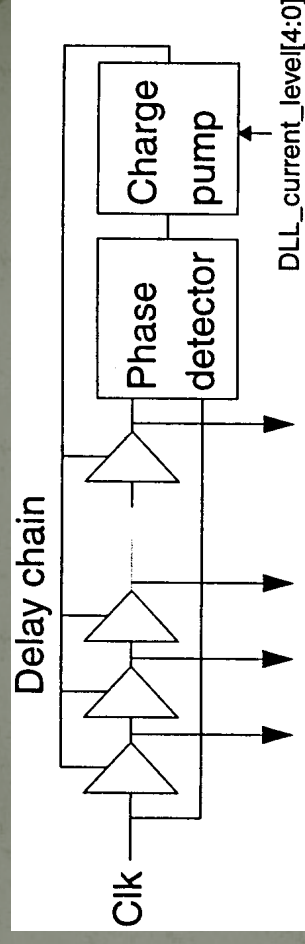


Architecture of HPTDC (ALICE TOF)



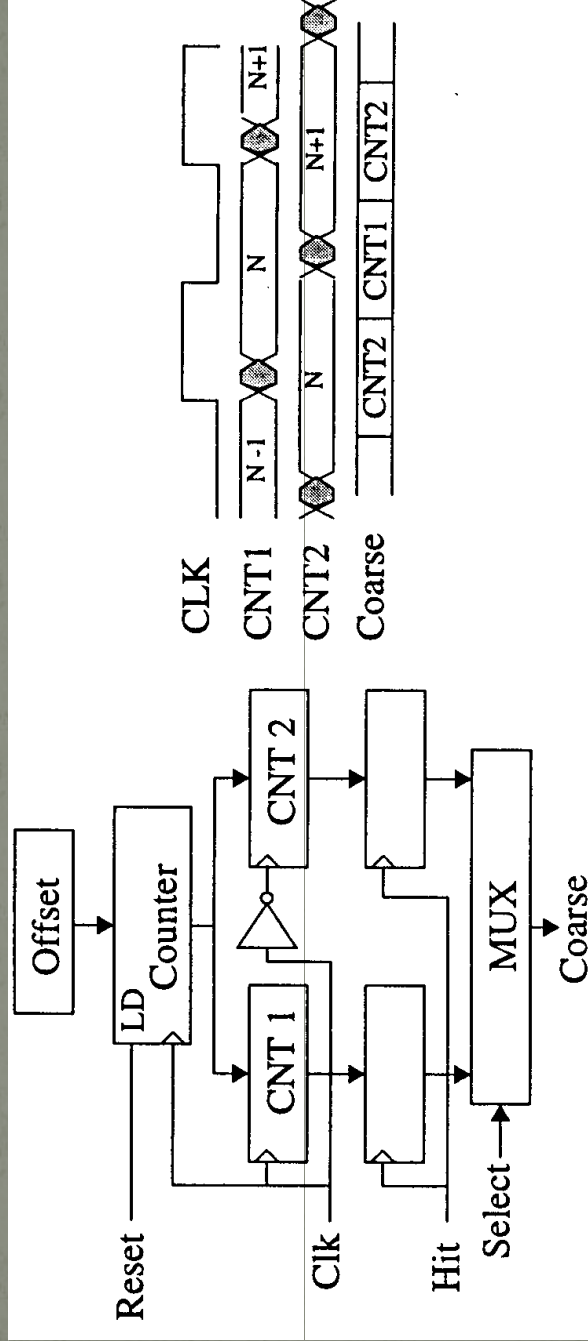
Delay Locked Loop (DLL)

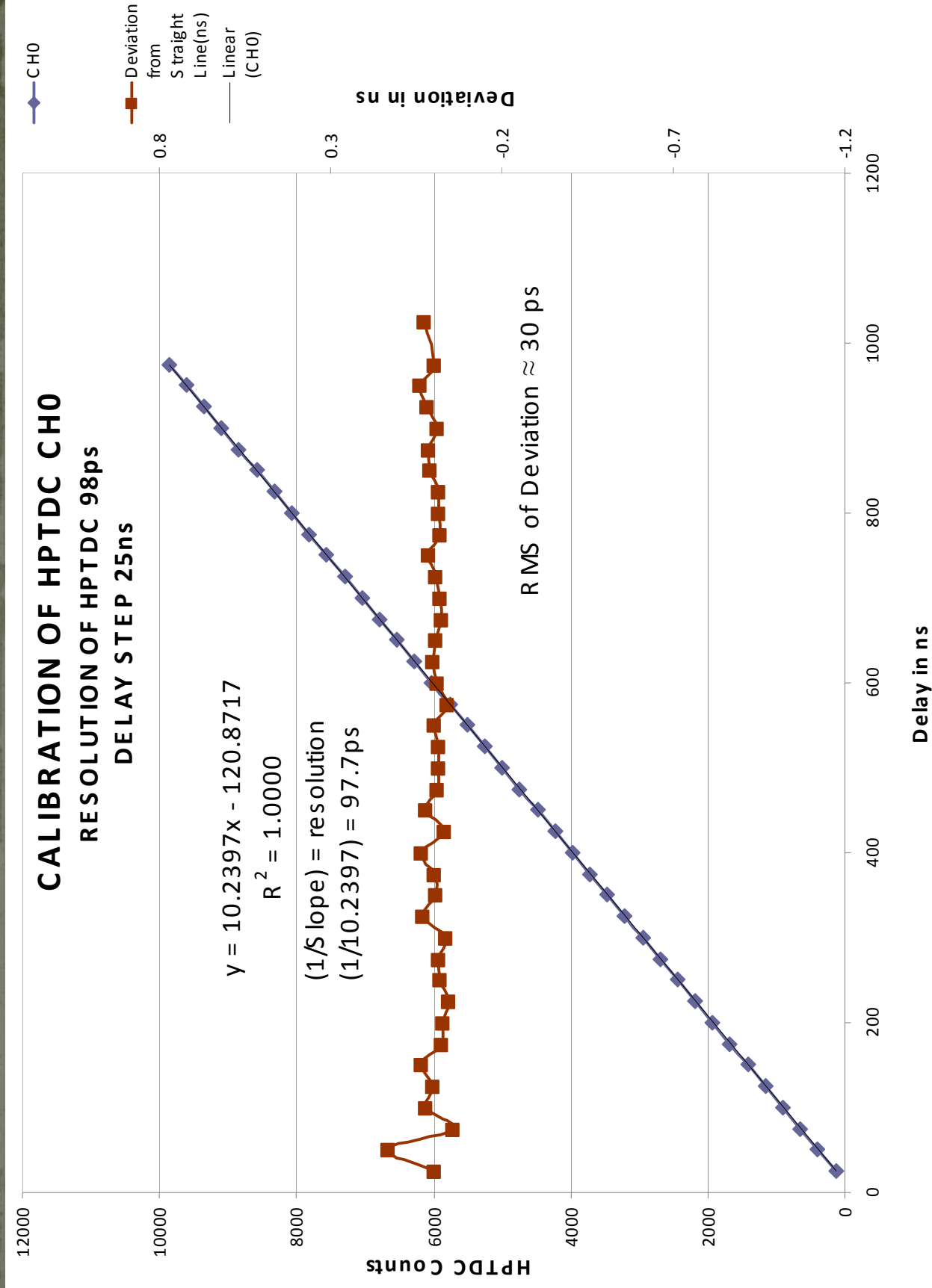
- Three major components:
 - Chain of 32 delay elements; adjustable delay
 - Phase detector between clock and delayed signal
 - Charge pump & level shifter generating control voltage to the delay elements
- Jitter in the delay chain
- Lock monitoring
- Dynamics of the control loop
- Programmable charge pump current level



Coarse time count

- Dynamic range of the fine time measurement, extracted from the state of DLL is expanded, by
- Storing the state of a clock synchronous counter
- Hit signal is synchronous to the clocking, so
- Two count values, $\frac{1}{2}$ a clock cycle out of phase stored
- At reset, coarse time counter loaded with time offset

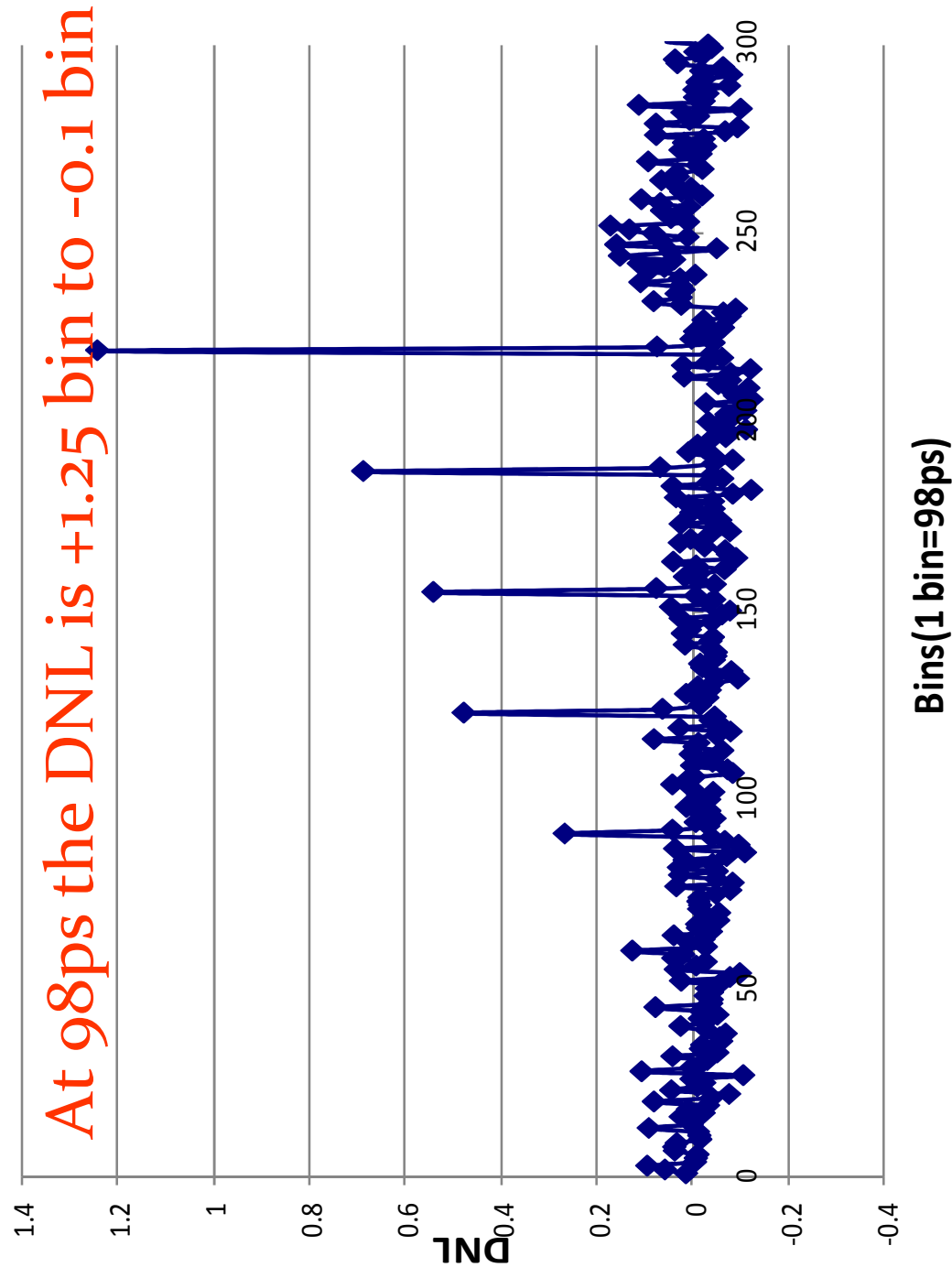




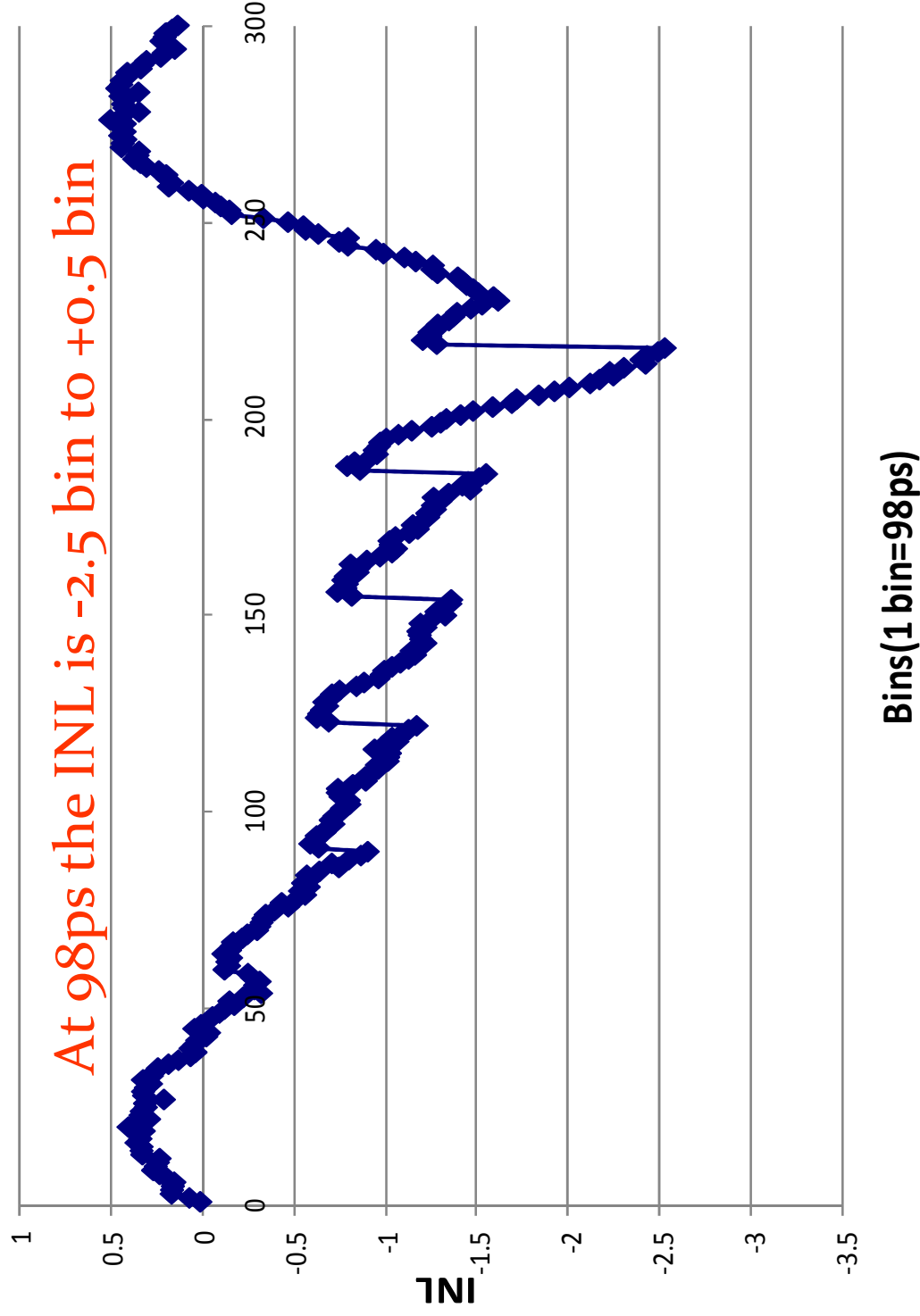
HPTDC's DNL and INL

- Differential Non-Linearity(DNL) is defined as the variation of any code from an ideal 1 LSB step.
- $DNL(n) = (Actual(n)/Expected(n)) - 1$.
- Integral Non-Linearity (INL) is the deviation of the transfer function from a reference line measured in fractions of 1 LSB using a best straight line. INL is simply the integral of the DNL.
- So if we can get the DNL then we can compute the INL.
- In HPTDC the base clock is 40 MHz i.e. 25ns so the DNL pattern repeats every 25ns.

HPTDC's DNL test result



HPTDC's INL test result



HP'TDC's DNL/INL data correction

- The fixed pattern in the INL is caused by 40 MHz cross talk from the logic part of the chip to the time measurement part .
- As this crosstalk comes from the 40MHz clock, which is also the time reference of the TDC, the integral non linearity have a stable shape between chips and can therefore be compensated for using the LSB bits of the measurements.

Test Condition	Effective resolution (RMS)
98ps resolution	64ps
98ps resolution after INL correction	34ps
24ps resolution	58ps
24ps resolution after INL correction	17ps

Thank you

For your attention.

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SERCEHEP07, IIT Bombay, Powai