Signal Processing Electronics

B.Satyanarayana
Department of High Energy Physics
Tata Institute of Fundamental Research, Mumbai
E: bsn@tifr.res.in ▪ **T**: 09987537702 ▪ **W**: http://www.tifr.res.in/~bsn

Plan of the course

- Lecture – I (Monday, January 28, 2013, 11:45-1:00)
  - Introduction
  - Some basic concepts
  - Signal types and characteristics
  - Signal transmission
- Lecture – II (Tuesday, January 29, 2013, 10:00-11:15)
  - Preamplifiers
  - Shaping amplifiers
  - Comparators/discriminators
  - Coincidence circuits
- Lecture – III (Tuesday, January 30, 2013, 2:30-3:45)
  - Analog-to-Digital Converters
  - Spectroscopy systems
  - Time-to-Digital Converters
  - Waveform digitisers
- Lecture – IV (Wednesday, January 30, 2013, 5:15-6:30)
  - Digital circuits and systems
  - CPLDs, FPGAs and ASICs
  - Instrumentation and interface standards
  - Data acquisition systems

Lecture - I

Monday, January 28, 2013

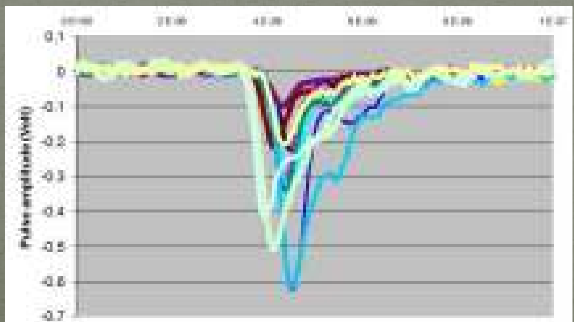
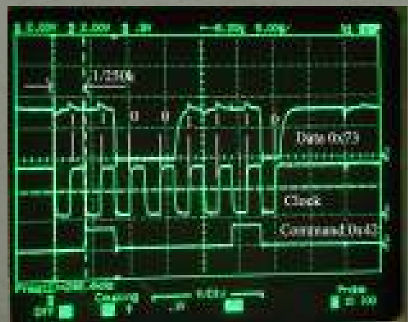
- ✓ Introduction
- ✓ Some basic concepts
- ✓ Signal types and characteristics
- ✓ Signal transmission

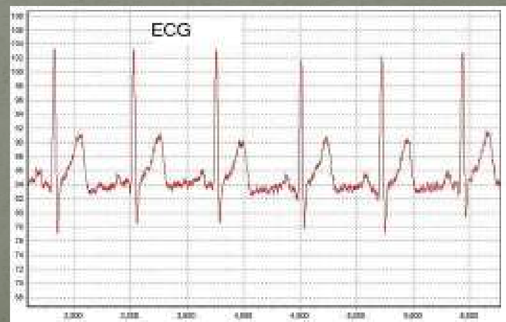
Motivation

- Detection of radiation using particle detectors in the end nearly always comes down to detecting some small electrical signal.
- Dealing with such small signals is one of the main challenges in designing detectors and instrumentation for nuclear physics and particle physics experiments.
- Electronic processing of signals is done in some fashion to extract some useful information from them, usually leading to a physics measurement.

Signals

- Generalised name for inputs into the instrumentation system
- Might seem logical to consider signals even before the sensors, though they can not be seen or recorded
- Wide range of signal types are possible:
  - Depends on sensors or detectors
  - Depends on any further transformation – for ex. light to electrical
- Most common types of signals:
  - Short, random pulses usually of current. Pulse shape, amplitude, rise time, area etc. carry useful information - typical of radiation sensors
  - Trains of pulses, often current, usually binary - typical of communication systems
  - Continuous, usually of slowly varying quantity – for ex. current or voltage



Signal characteristics

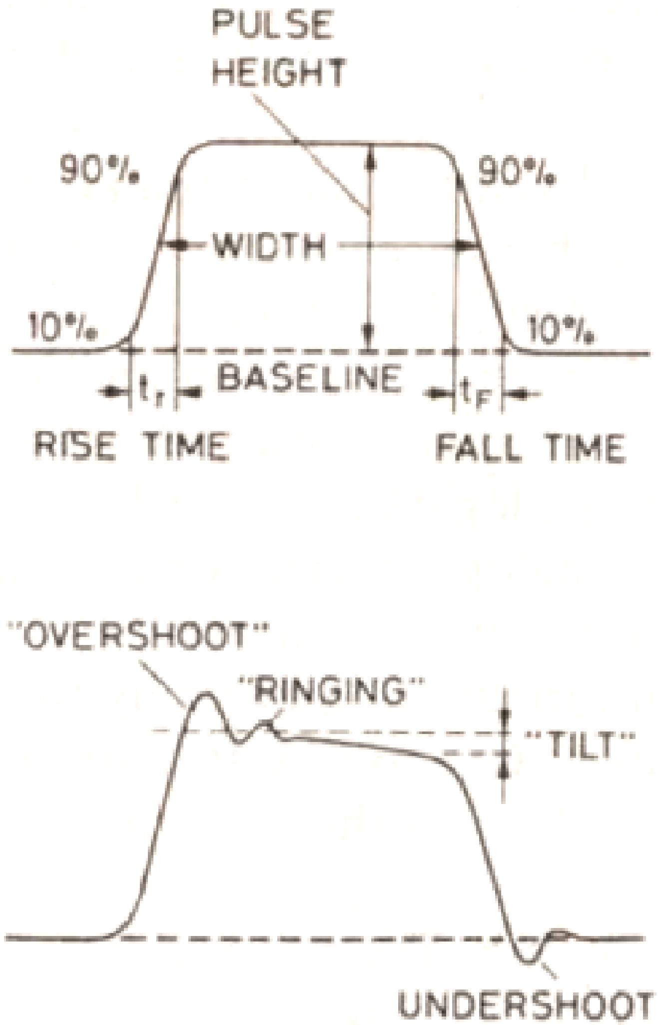
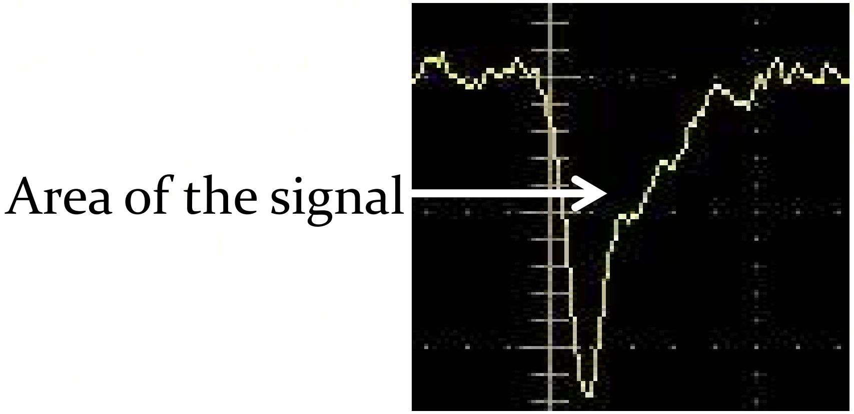


Fig. 11.1. Pulse signal terminology



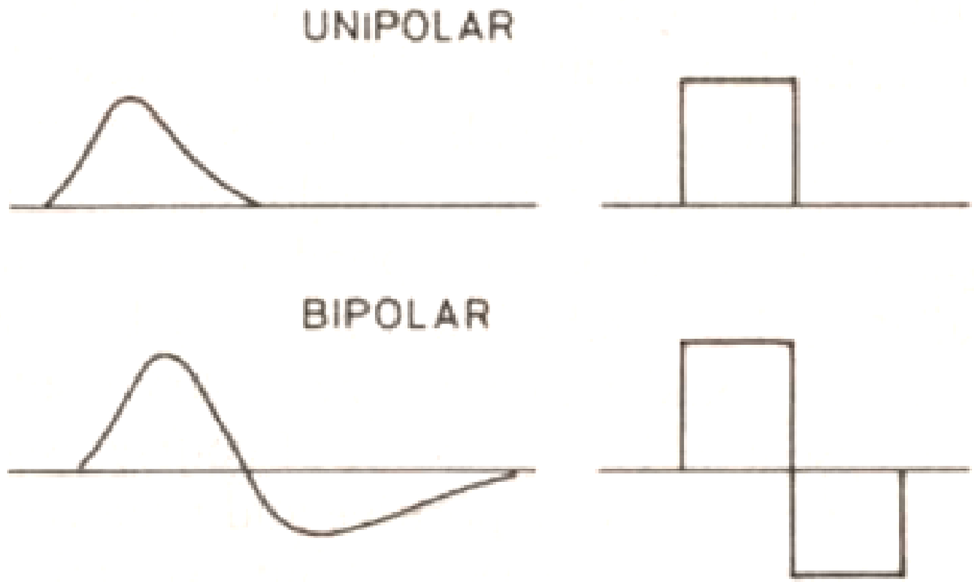
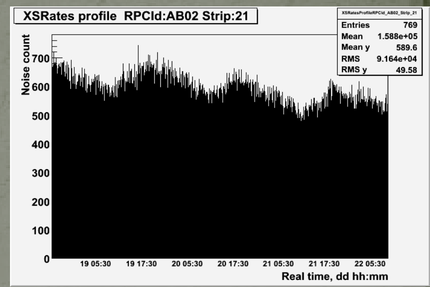


Fig. 11.2. Unipolar and bipolar pulses

Issues on signal production

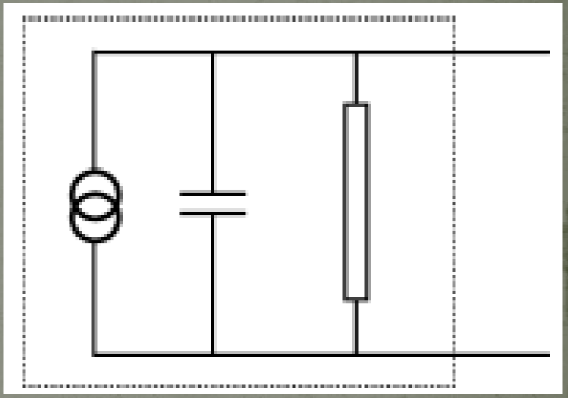
- Issues in practical applications
  - Duration
    - Radiation: depends on transit time through sensor and details of charge induction process in external circuit
  - Linearity
    - Most radiation sensors are characterised or chosen for linearity
    - Commercial components can expect non-linearity, offset and possible saturation
  - Reproducibility
    - Many signals are temperature dependent in magnitude - mobility of charges, other effects easily possible as well



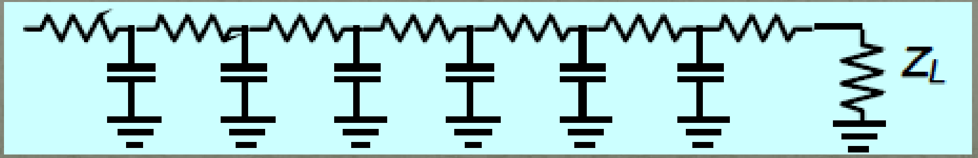
  - Ageing
    - Sensor signals can changed with time for many reasons
    - Natural degradation of sensor, variation in operating conditions, radiation damage, etc.
- All these issues mean that one should always be checking or calibrating measurements intended for accuracy, as best one can

Sensor equivalent circuits

- Many of the sensors can be modelled as current source associated with large internal resistance and a small capacitance.
- Capacitance of detectors vary considerably:
  - 100fF for semiconductor pixel
  - 10-20pF for gas or Si microstrip, PMT anode
  - 100pF for large area diode
  - µF for wire chamber



- Usually there is some resistance associated with the sensor, for ex. leads or metallisation but this has little effect on signal formation or amplification
- Notable exceptions: microstrips - gas or silicon
  - The capacitance is distributed, along with the strip resistance
  - Forms a dissipative transmission line:



Typical signals

- Some examples

Signal source	Duration
Inorganic scintillator	$e^{-t/\tau}$ $\tau \sim$ few μs
Organic scintillator	$e^{-t/\tau}$ $\tau \sim$ few ns
Cerenkov	~ns
Gaseous	few ns - μs
Semiconductor	~10ns
Thermistors	continuous
Thermocouple	continuous
Laser	pulse train ~ps rise time or short pulses ~fs

- However, we will find later that speed of signal is not always sufficient to build fast responding systems

Dynamic range of signals

- In most systems, there will be a smallest measurable signal
  - If there is noise present, it is most likely to be related to the smallest signal distinguishable from noise
  - In the absence of any ionising radiation there is a small current, which is called the dark current or leakage current
- and a largest measurable signal
  - most likely set by apparatus or instrument, eg. saturation
- Dynamic range = ratio of largest to smallest signal often expressed in dB or bits
  - For ex. 8 bits = dynamic range is 256_{10} = 48dB (if signal is voltage)
- Decibels (dB)
  - Signal magnitudes cover wide range, so frequently logarithmic scale is preferred.
  - Number of dB = $10\log_{10}(P_2/P_1)$
  - Often measuring voltages in system: dB =$20\log_{10}(V_2/V_1)$

Precision of signal measurement

- Many measurements involve detection of particle or radiation quantum (photon)
  - Simple presence or absence sometimes sufficient = binary (0 or 1)
  - Other measurements are of energy, timing etc.
- Why do we need such observations?
  - Primary measurement may be energy
    - Ex. medical imaging using gammas or high energy x-rays, astro-particle physics
  - Extra information to improve data quality
    - Removes experimental background, for ex. Compton scattered photons mistaken for real signal
  - Optical communications - pressure to increase "bandwidth" – eg. number of telephone calls carried per optical fibre
    - Wavelength division multiplexing - several "colours" or wavelengths in same fibre simultaneously

Types of detectors

Non-electronic detectors (Bubble chamber)

Electronic detectors (MWPC)

Electronic requirements for detectors

Detector	Physics	Technical
Tracking	High spatial precision Large channel count Limited energy precision Limited dynamic range	Low power ~mW/channel High radiation levels ~10Mrad
Calorimeter (EM & Hadron)	High energy resolution Large energy range Excellent linearity Very stable over time	Intermediate radiation levels ~0.5Mrad Power constraints
Muon	Very large area Moderate spatial resolution Accurate alignment & stability	Low radiation levels
Time of Flight	Discriminates between a lighter and a heavier particle of the same momentum	Time of flight between two detector planes
Neutrinos	Detected through inferred momentum conservation.	Good spatial and time resolutions
Dark matter	Principle of nuclear recoil by candidate particles	Low counting and high precision experiment

Measurements & measuring elements

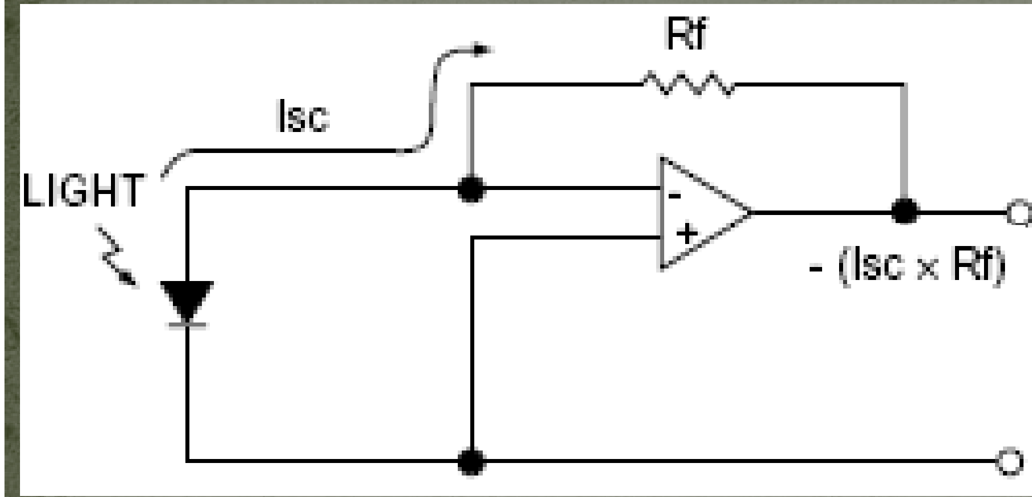
- Some primary and some derived
- Light
- Energy
- Charge/Current
- Pulse shape
- Pulse height/Voltage
- Relative timing
- Position/Particle track

- Amplifiers and Comparators
- Analog to Digital Converters
- Charge to Digital Converters
- Time to Digital Converters
- Waveform digitisers
- Latches and Registers
- Memories
- Logic/trigger systems
- Hybrids

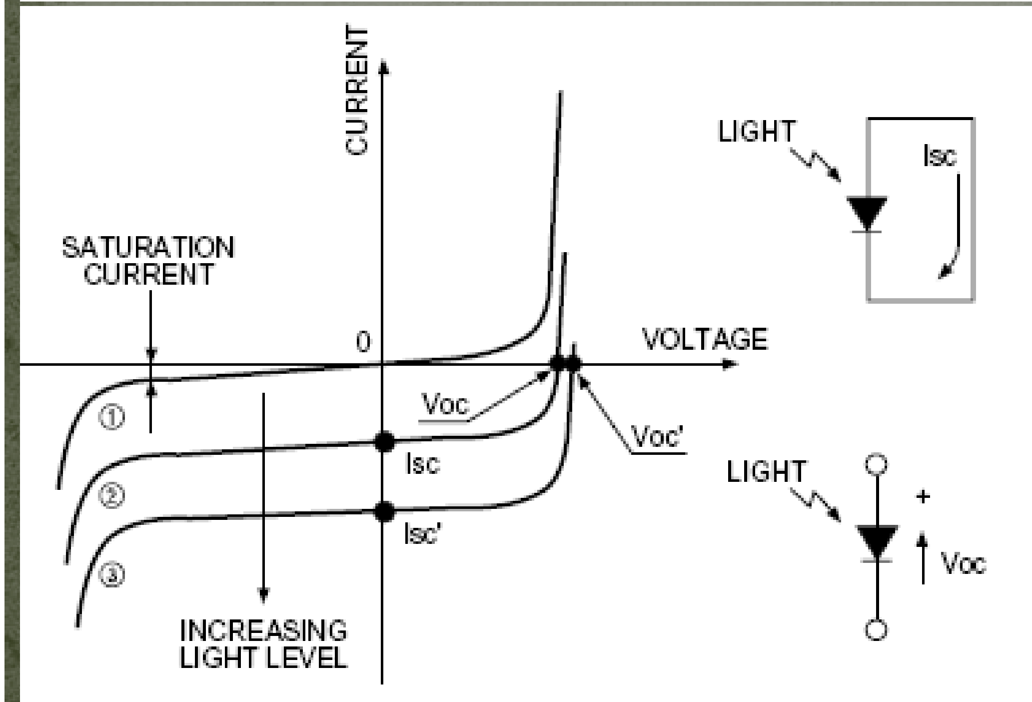
Modes for measuring detector signals

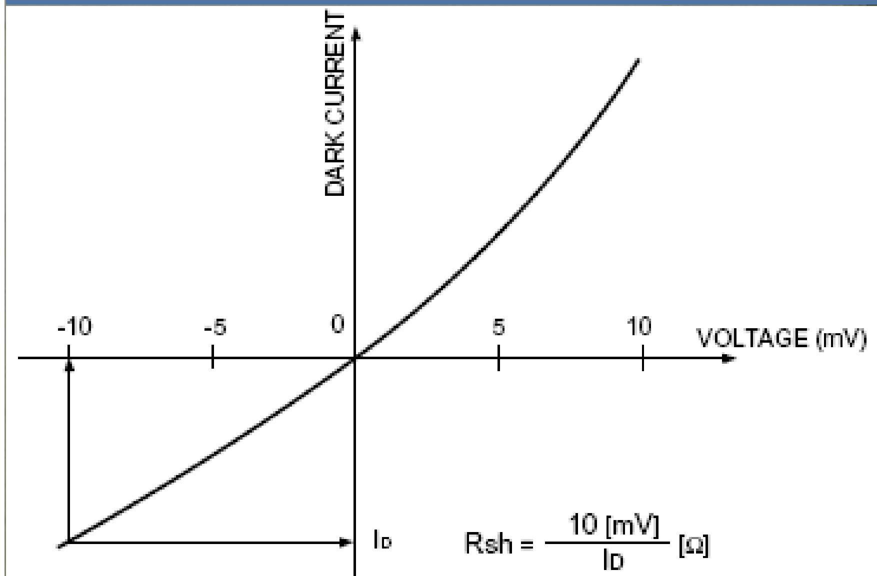
- Current mode
  - Measures the total current of the detector and ignores the pulse nature of the signal.
  - Does not allow advantage to be taken of the timing and amplitude information present in the signal.
- Pulse mode
  - Observes and counts the individual pulses generated by the particles.
  - Gives superior performance but cannot be used if the rate is too large.

Current mode

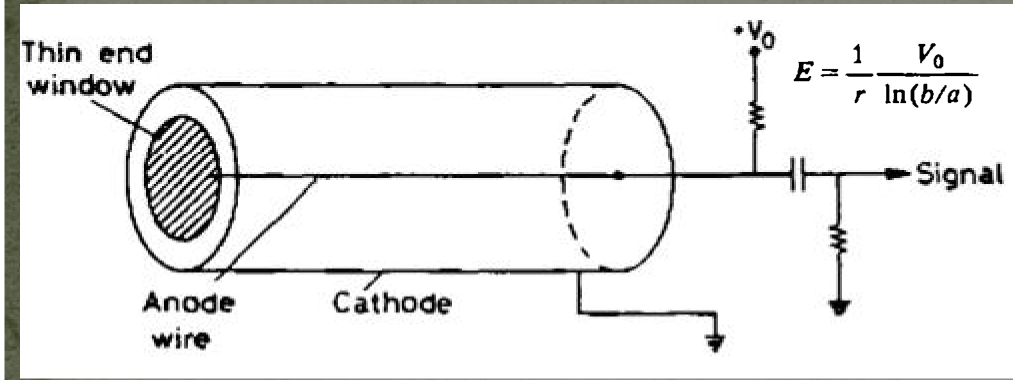


If we set the open loop gain of the operational amplifier as A, the characteristics of the feedback circuit allows the equivalent input resistance to be which is several orders of magnitude smaller than R_f. Thus this circuit enables ideal I_{sc} measurement over a wide range.

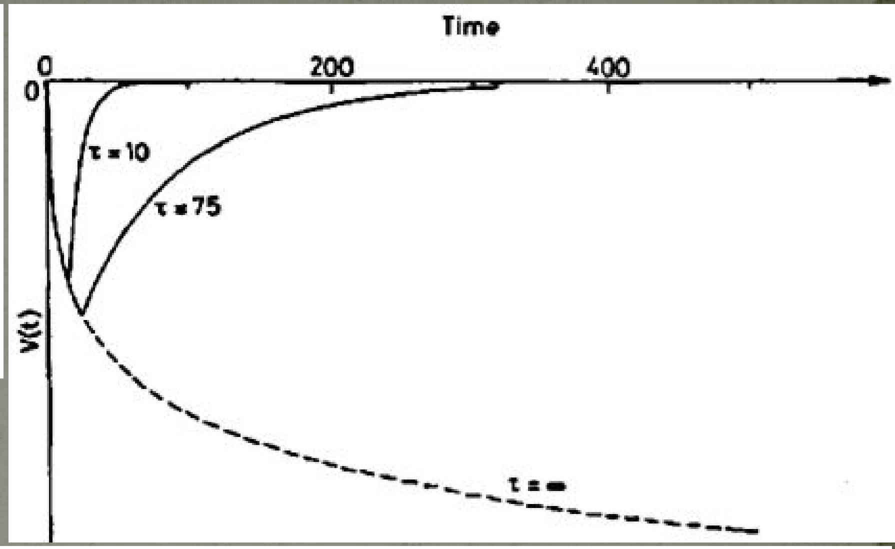




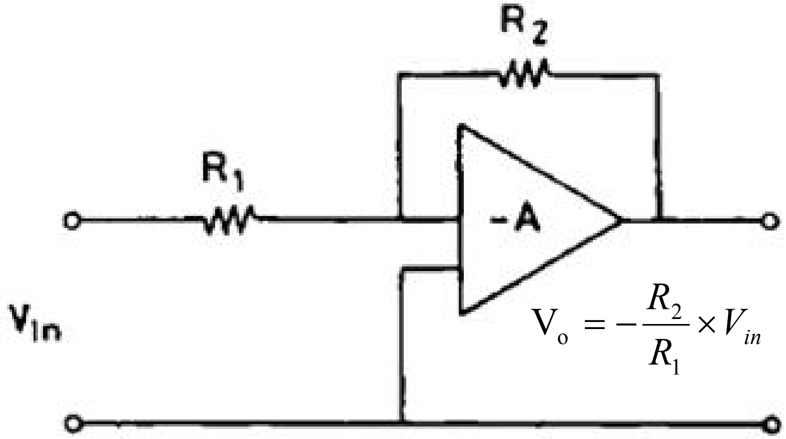
An example of pulse mode



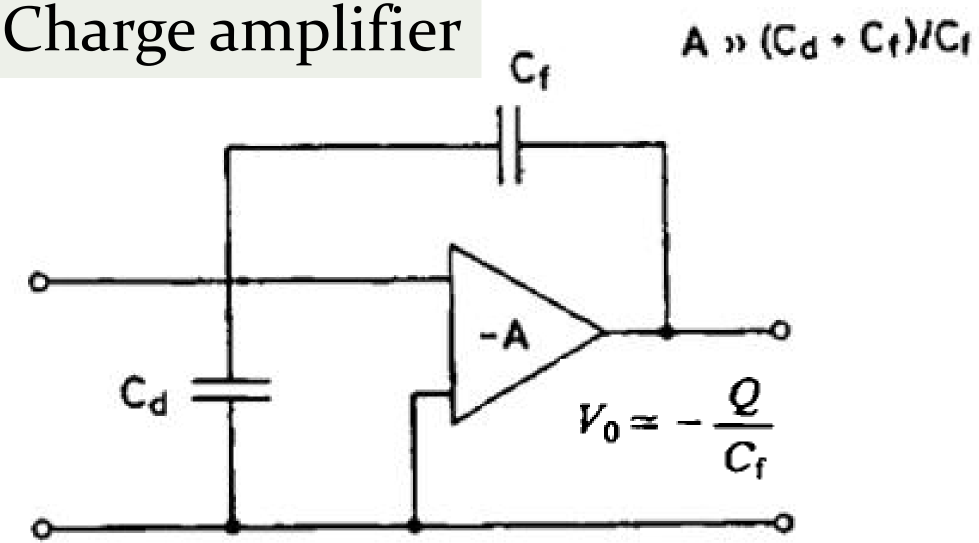
Basic ionisation chamber



Voltage amplifier



Charge amplifier

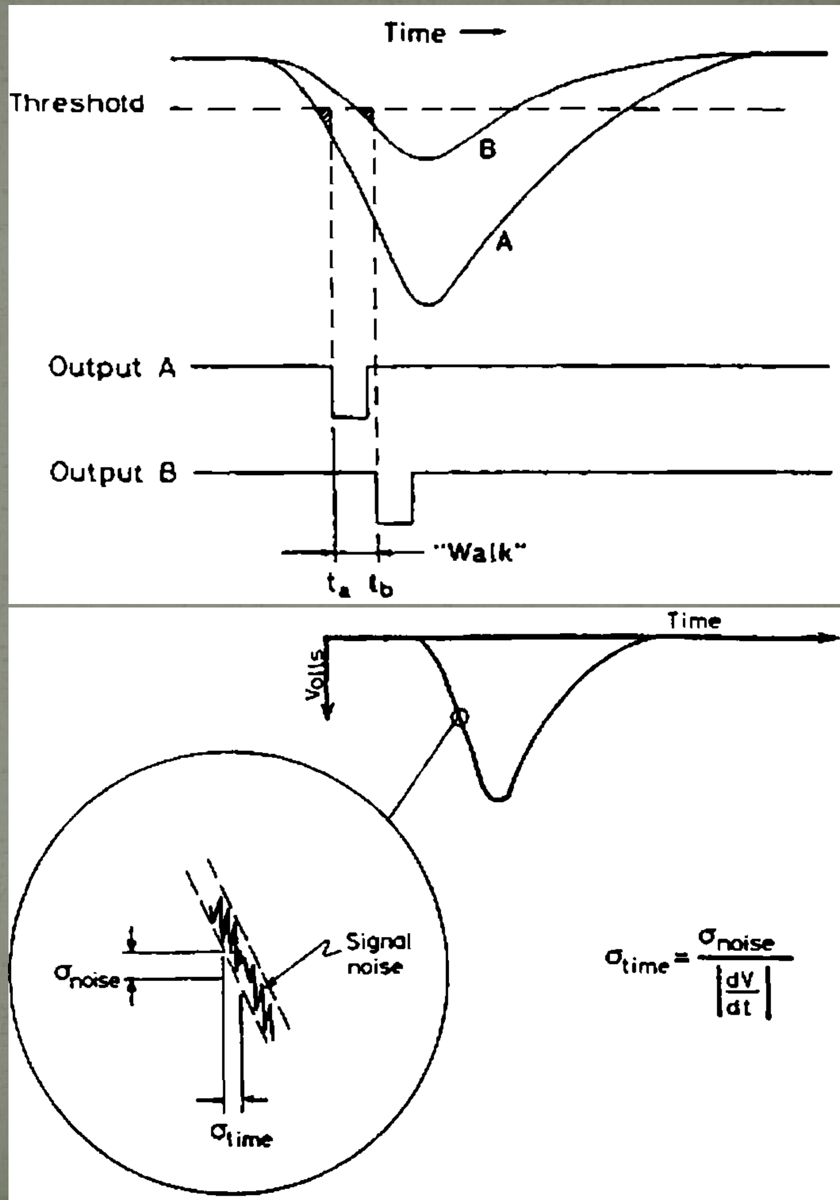


Pulse mode

- Amplitude of the pulses is proportional to the initial charge signal and the arrival time of the pulse is some fixed time after the physical event.
- By using appropriate thresholds, one can select and count only those pulses that one wants to count.
- Often the 'good events' are characterised by
  - some specific signal amplitude
  - simultaneous presence of two (or more) signals in different detectors.
  - absence of some other signal.
- In the pulse mode, one can register a pulse height spectrum and such a spectrum contains a large amount of useful information.

Two common problems

- Walk (due to variations in the amplitude and rise time, finite amount of charge required to trigger the discriminator)
- Jitter (due to intrinsic detection process – variations in the number of charges generated, their transit times and multiplication factor etc.)



Transmission of data

- •Real systems are often distributed
  - Data source is remote from signal processing
  - Instruments in hazardous or very remote environment
    - Eg. satellites, HEP, nuclear reactors,..,
  - But also applies to much shorter distances - like nearby labs or instruments in the same room
  - Need to transfer signal/data from source to receiver
  - And usually send messages (ex. control signals) back
- Need to understand
  - Practical ways of doing this
  - Issues: power, speed, noise,... other physical constraints
- Methods - a mixture
  - Electrical, but increasing use of optical fibres,
  - Radio for satellites and space, mobile telephones,...

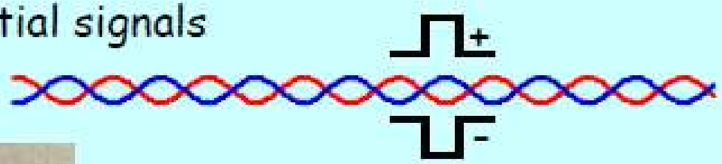
Cables

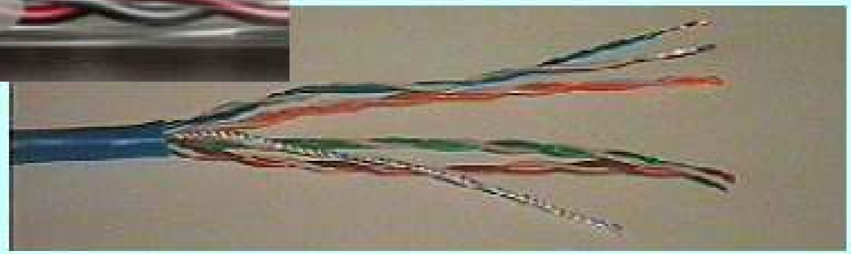
- Any wire has inductance, capacitance and resistance

  so when is it a transmission line?

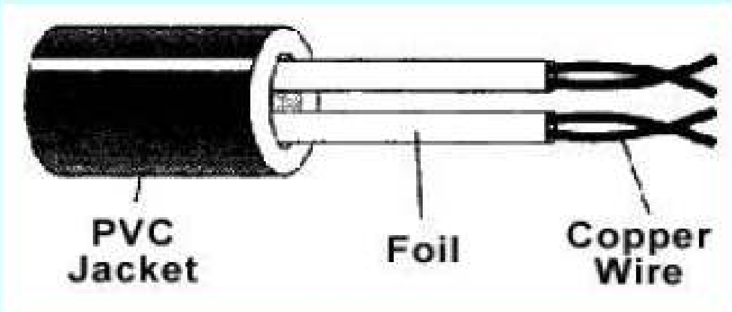
- Twisted pair

  simple pair of wires, mainly intended for differential signals

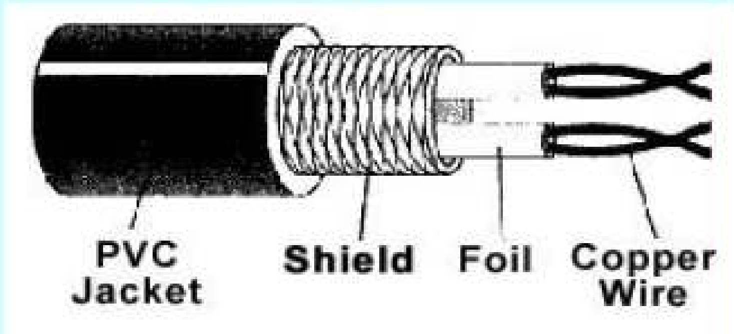




Can also be unshielded…



or shielded



Coaxial cable

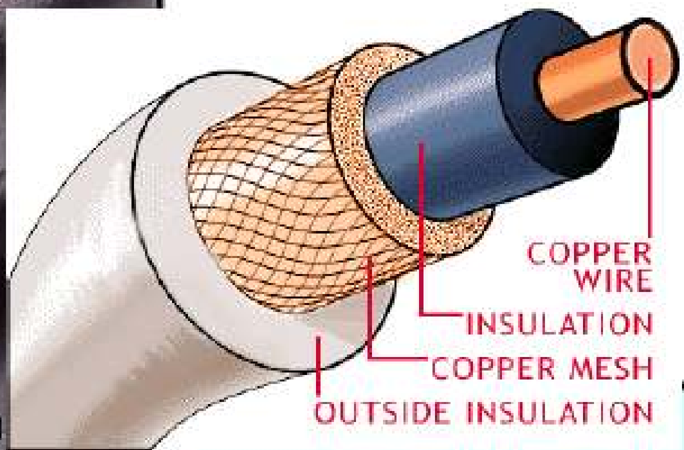
central copper core radius r_1, with plastic dielectric, braided metal shield in cylindrical geometry radius r_2

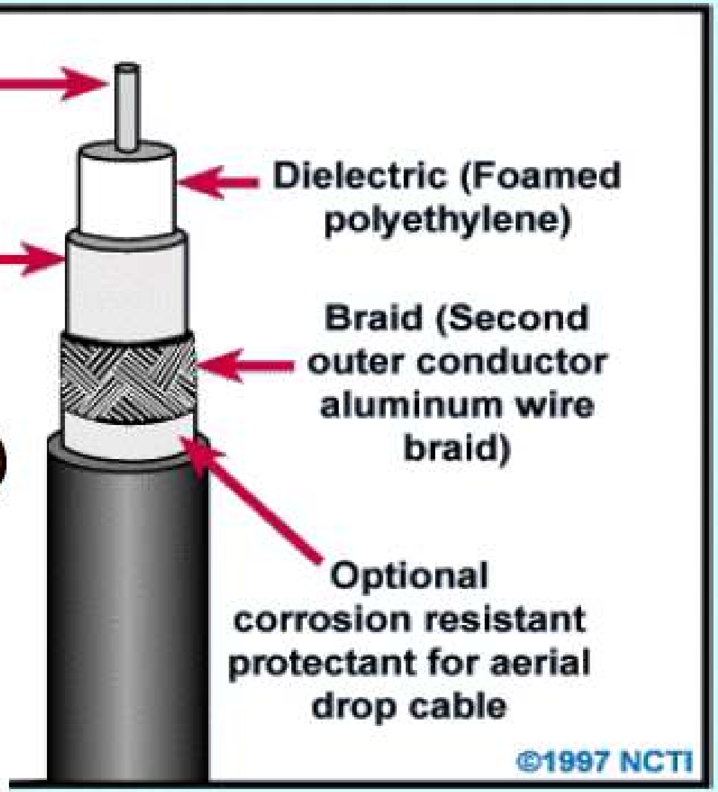
$C_0 = 2\pi\varepsilon/\ln(r_2/r_1)$ $L_0 = (\mu_0/2\pi).\ln(r_2/r_1)$ *see lecture 1 notes*

- Design

  Cu braid connected to ground provides electrical shield

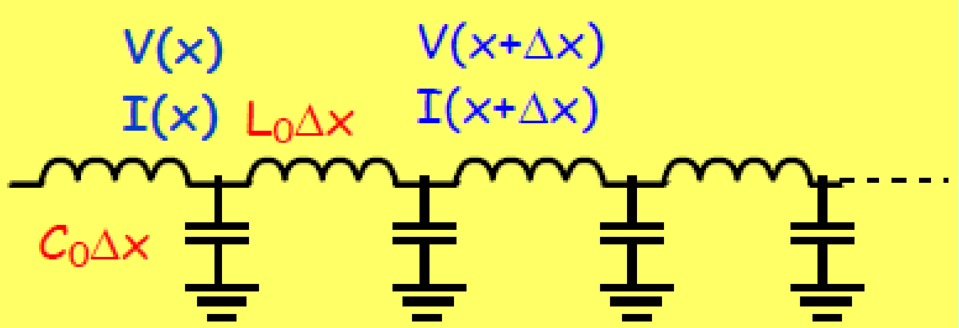
  use special connectors





Electrical transmission lines

• Line with characteristic inductance and capacitance per unit length



An important assumption
R negligible

• Voltage and current satisfy 2nd order differential equation

$d^2V/dx^2 = -\omega^2 L_0 C_0 V = -k^2 V$ ie $k = \omega(L_0C_0)^{1/2}$

• Solution

$V = Ae^{jkx} + Be^{-jkx}$

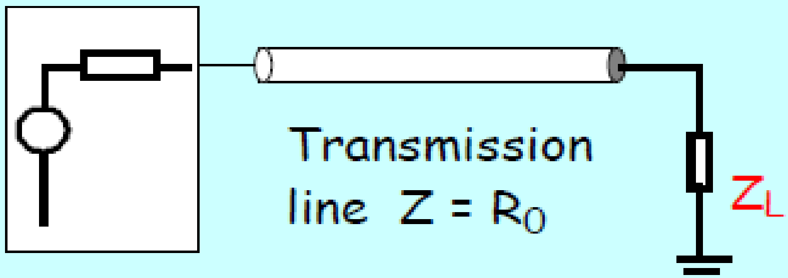
Inject signal $\sim e^{j\omega t}$ $V = Ae^{j(kx+\omega t)} + Be^{-j(kx-\omega t)}$ *two opposite direction waves*

• Speed $v = \omega/k = 1/(L_0C_0)^{1/2}$

• Impedance $Z_0 = (L_0/C_0)^{1/2}$

NB real, ie resistive, but defined by L and C

Termination and Matching



- boundary conditions at termination

  $I_{inc} + I_{ref} = I_L$ & $V_{inc} + V_{ref} = V_L$

  apply them (NB $V_{ref} = -I_{ref}Z_0$)

  $V_{ref}/V_{inc} = (Z_L - Z_0)/(Z_L + Z_0)$

  $V_L/V_{inc} = 2Z_L/(Z_L + Z_0)$

- open circuit termination $Z_L = \infty$

  $V_{ref}/V_{inc} = +1$ $V_L/V_{inc} = 2$ reflected signal = incident signal

- short circuit termination $Z_L = 0$

  $V_{ref}/V_{inc} = -1$ $V_L/V_{inc} = 0$ inverted fully reflected signal

- matched termination $Z_L = Z_0$

  $V_{ref}/V_{inc} = 0$ $V_L/V_{inc} = 1$ 100% transmission to load

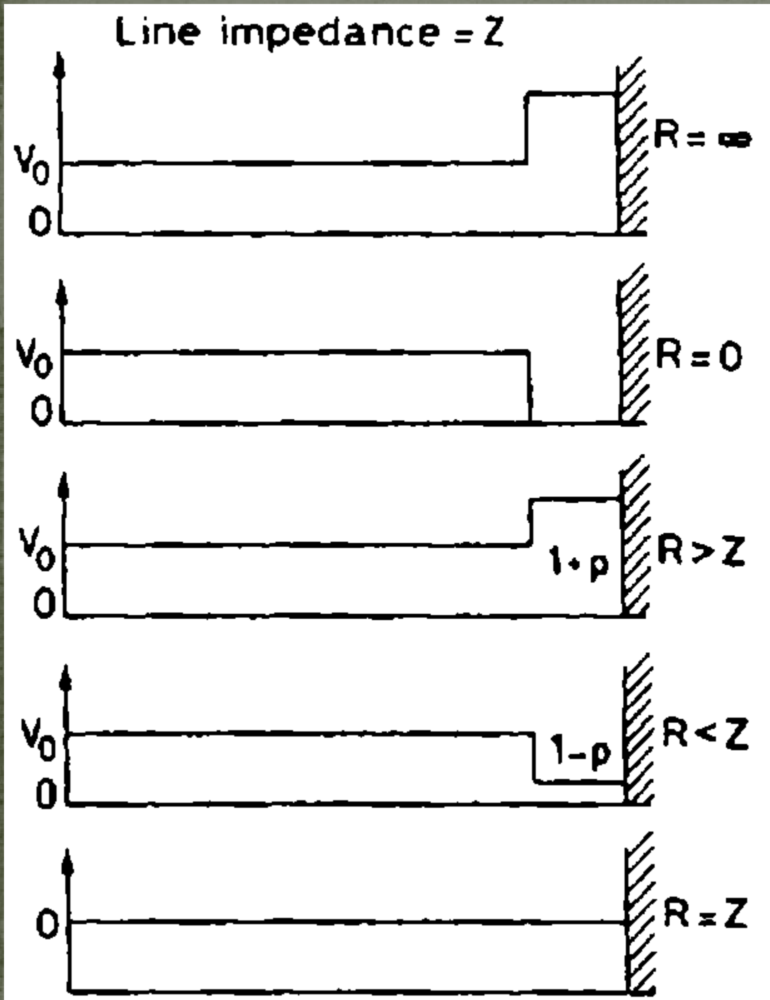
- improper termination usually causes unwanted effects

  but can sometimes make make use of reflection

  eg short circuit termination + step pulse = square pulse with width = $2\Delta t$

- why don't we always match terminate?

Reflections & terminations



$$\rho = \frac{V_r}{V_0} = \frac{-I_r}{I_0} = \frac{R-Z}{R+Z},$$

Cable impedance = Z_c

Source		*Load*	*Termination scheme*
$Z_s = Z_c$	Z_c	$Z_L = Z_c$	No termination necessary
$Z_s = Z_c$	Z_c	$Z_L > Z_c$	Receiving end; parallel $R = Z_c/(1 - Z_c/Z_L)$
$Z_s = Z_c$	Z_c	$Z_L < Z_c$	Receiving end; series $R = Z_c - Z_L$
$Z_s < Z_c$	Z_c	$Z_L = Z_c$	Sending end; series $R = Z_c - Z_s$
$Z_s > Z_c$	Z_c	$Z_L = Z_c$	Sending end; parallel $R = Z_c/(1 - Z_c/Z_s)$

Combinations of the above situations may also arise in which case an appropriate combination of termination schemes may be used, e.g.,

$Z_s < Z_c$	Z_c	$Z_L > Z_c$	Receiving end; parallel $R = Z_c/(1 - Z_c/Z_L)$ with sending end; series $R = Z_c - Z_s$

Match if…

- Impedance matching is a general question, not only for transmission lines
- Match if
  - to transfer maximum power to load (source must be capable)
    - ex. audio speakers
  - minimise reflections from load
    - very important in audio, fast (high frequency) systems, to avoid ringing
    - or multiple pulses (eg in counting systems)
  - fast pulses
    - pulse properties can contain important information
    - we usually don't want to change the pulse shape
    - sometimes we wish to do this with "too fast" signals - "spoiling"
- Usually match by choosing impedances, adding voltage buffers
  - transformer matching is another method if this is impractical

Don’t match if…

- Don't match if
  - High impedance source with small current signals - typical of many sensors
    - photodiode, or other sensors must drive high impedance load
    - short cables are required to avoid difficulties
  - Weak voltage source, where drawing power from source would affect result
    - ex. bridge circuits
  - require to change properties of fast pulse
    - ex. pulse widening for ease of detection
  - electronics with limited drive capabilities
    - ex. logic circuits, many are designed to drive other logic, not long lines
    - CMOS circuits, even with follower, are an example
  - If you get this wrong, often end up with new time constants in the system
    - or prevent system from working at all, ex. diode with low R_{load}

Coaxial cable limits

- Transmission speed and bandwidth limiting
  - all cables have finite resistance (though remarkably small)
  - for long cables, RC time constant per unit length becomes noticeable
  - therefore expect delay, attenuation and finite rise time in fast pulses
- When is a cable a transmission line?
  - not reasonable to assume transmission line behaviour unless length of line is at least ~ 1/8 wavelength
- Other forms of transmission line
  - in high speed circuits, tracks must be laid out carefully using knowledge of the characteristics of the boards to control delays, rise times and signal velocities
  - ex. parallel tracks,…
  - often need measurement to define parameters precisely
  - ultra high frequencies need waveguides or alternative

Pulse distortions in cables

- Signal losses in a transmission line arise from resistance in the conductors and leakage through the dielectric. In addition, some loss may also result from electromagnetic radiation; however, this effect is small, especially in coaxial cables with their inherent shielding, and can be neglected for most purposes.
- As frequency of the signal increases, the current in the conductors confines itself to thinner and thinner layers near the conductor surface. The effective cross-sectional area of the conductor is thus reduced and its resistance increased. For a coaxial cable, this results in a resistance per unit length which varies approximately as the square root of the frequency and inversely as the inner and outer radii.

Pulse distortions in cables

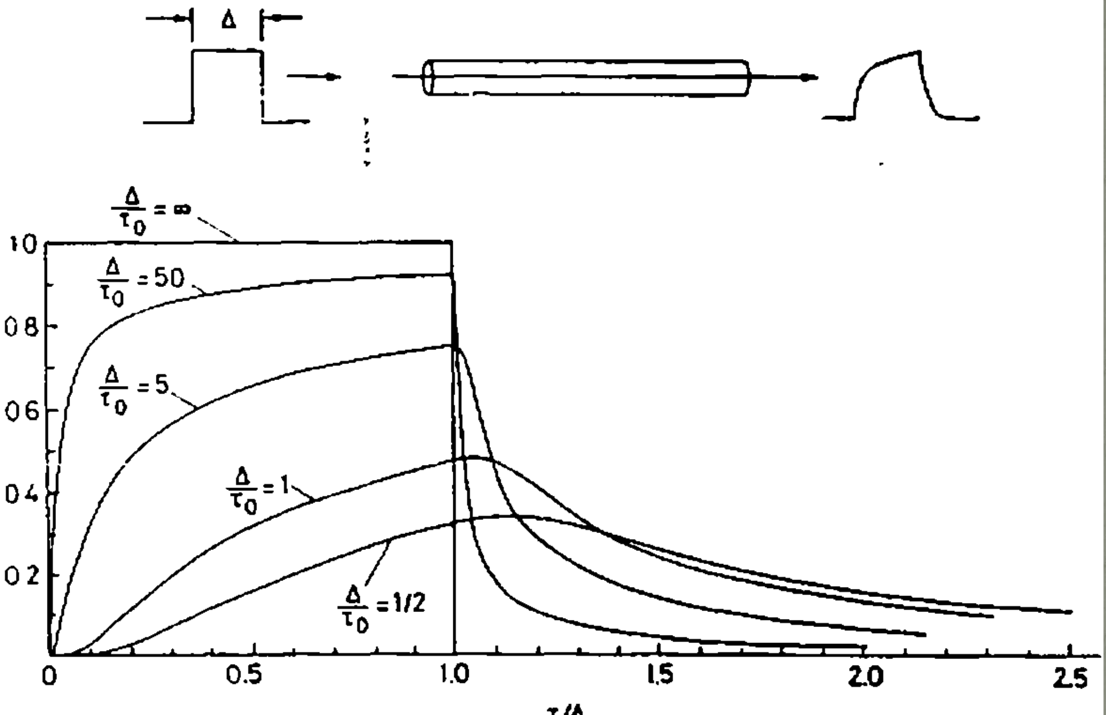


Fig. 13.10

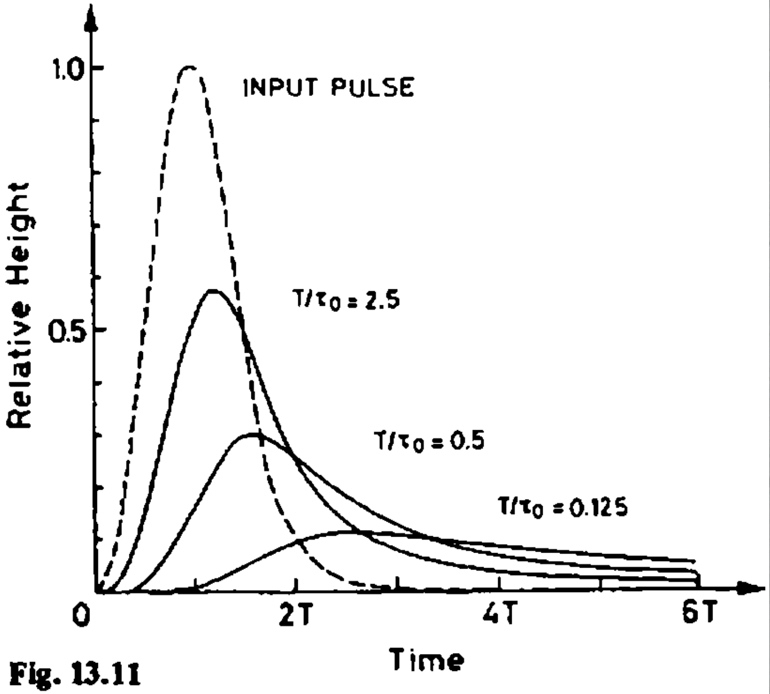


Fig. 13.11

Lecture - II

Tuesday, January 29, 2013

- ✓ Preamplifiers
- ✓ Shaping amplifiers
- ✓ Comparators/discriminators
- ✓ Coincidence circuits

Amplifiers

- Inescapable in electronic instruments
  - amplifiers are needed for most if the detectors
  - even if not used to boost signals, amplifiers are the basis of most important functional blocks
- In many circumstances amplification, in the sense of "boosting" signals, is vital
  - signals to be measured or observed are often small
  - defined by source - or object being observed
  - and sensor - it is not usually easy to get large signals
  - data have to be transferred over long distances without errors
  - safest with "large" signals

Amplifiers in systems

- Amplification
  - role of a preamplifier
  - single gain stage rarely sufficient
  - add gain to avoid external noise , for ex. to transfer signals from detector
  - practical designs depend on detailed requirements
  - constraints on power, space,… cost in large systems
  - ex. ICs use limited supply voltage which may constrain dynamic range
- Noise will be an important issue in many situations
  - most noise originates at input as first stage of amplifier dominates
  - often refer to Preamplifier = input amplifier
  - may be closest to sensor, subsequently transfer signal further away
- In principle, several possible choices
  - I sensitive (Used with low impedance detectors)
  - V sensitive (Conventional, most common)
  - Q sensitive (Used with semiconductor detectors)

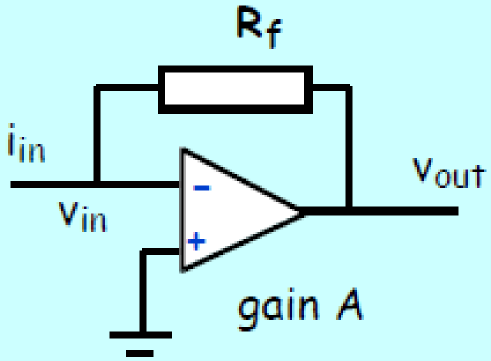
Current sensitive amplifier

- Common configuration, eg for photodiode signals

  $v_{out} = -Av_{in}$

  $v_{in} - v_{out} = i_{in}R_f$

  $v_{out} = -[A/(A+1)].i_{in}R_f \approx -i_{in}R_f$



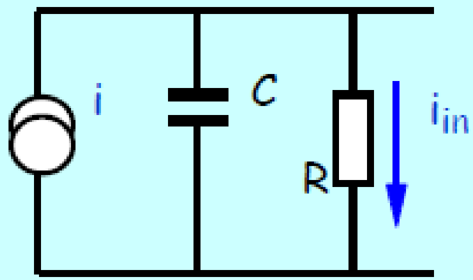
- Input impedance

  $v_{in} = i_{in}R_f/(A+1)$ $Z_{in} = R_f/(A+1)$

- Effect of C & R_{in} - consider in frequency domain

  $v_0 = i(1/j\omega C||R_{in})$

  $= i(\omega)R/(1 + j\omega\tau)$



  input signal convoluted with falling exponential

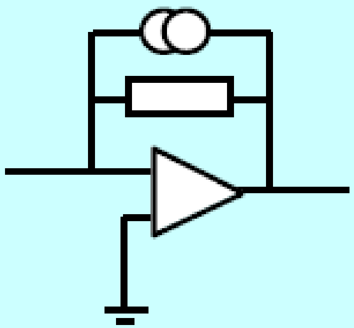
  increasing R_f to gain sensitivity will increase τ

  fast pulses will follow input with some broadening

- Noise

  will later find that feedback resistor is a noise source

  contributes current fluctuations at input ~ $1/R_f$



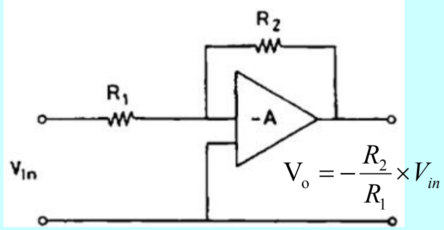
Voltage sensitive amplifier

- Most commonly used, simple to implement
- Many times, input signal is first manipulated, followed by a voltage amplifier

- As we have seen many sensors produce current signals but some examples produce voltages - thermistor, thermocouple,...

  op-amp voltage amplifier ideal for these

  especially slowly varying signals - few kHz or less



- For sensors with current signals voltage amplifier usually used for secondary stages of amplification

- Signal $V_{out} = Q_{sig}/C_{tot}$

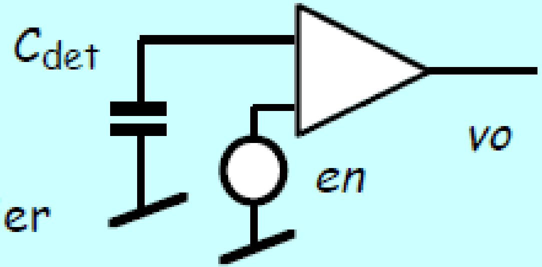
  C_{tot} = *total input capacitance*

  C_{tot} will also include contributions from wiring and amplifier

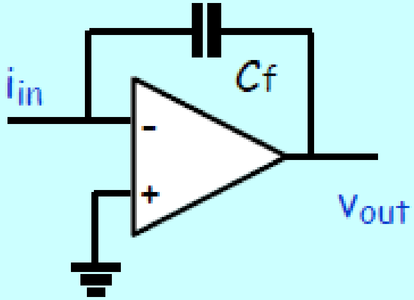
  V_{out} depends on C_{tot}

  not desirable if C_{det} is likely to vary

  eg with time, between similar sensors, or depending on conditions



Charge sensitive amplifier



- Ideally, simple integrator with C_f

  but need means to discharge capacitor - large R_f

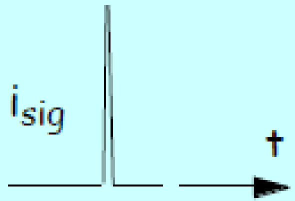
- Assume amplifier has Z_{in} very high (usual case)

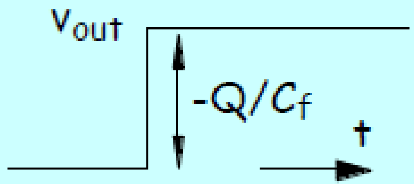
  $v_{out} = -Av_{in}$

  $v_{out} - v_{in} = i_{in}/j\omega C_f$

  $v_{out} = -[A/(A+1)].i_{in}/j\omega C_f \approx i_{in}/j\omega C_f$

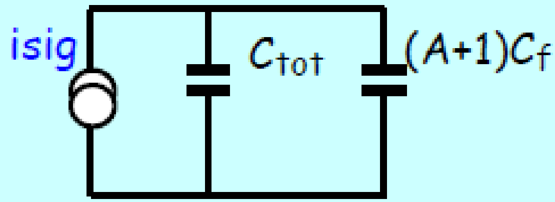
  $\Rightarrow -Q/C_f$





- Input impedance

  $v_{in} = i_{in}/(A+1)j\omega C_f$ $\quad C=(A+1)C_f$ at low f



so amplifier looks like large capacitor to signal source

low impedance but some charge lost

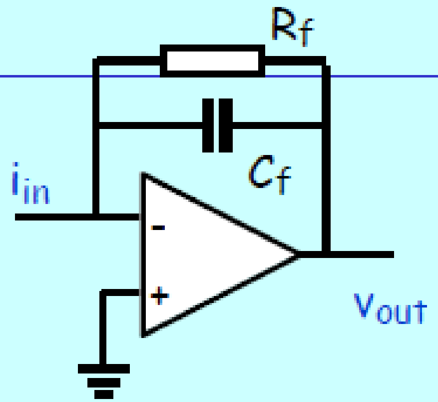
e.g. $A = 10^3$ $\quad C_f = 1pF$

$Q_A = Q/[1 + C_{tot}/(A+1)C_f]$

$C_{tot} = 10pF$ $\quad Q_A/Q = 0.99$

$C_{tot} = 100pF$ $\quad Q_A/Q = 0.90$

Feedback resistance



- Must have means to discharge capacitor so add R_f

  $Z_f = R_f || 1/j\omega C_f$

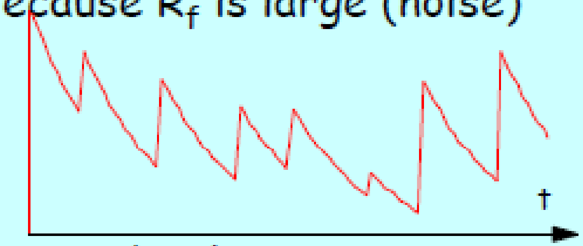
  $v_{out} = -[A/(A+1)].i_{in} Z_f$

  $= i(\omega) R_f/(1 + j\omega\tau_f) \qquad \tau_f = R_f C_f$

  step replaced by decay with ~ $\exp(-t/R_f C_f)$ τ is long because R_f is large (noise)

  easiest way to limit pulse pileup - differentiate

  ie add high pass filter



- Pole-zero cancellation

  exponential decay + differentiation => unwanted baseline undershoot

  introduce canceling network

  $v_0 = 1/(1 + j\omega\tau_f)$

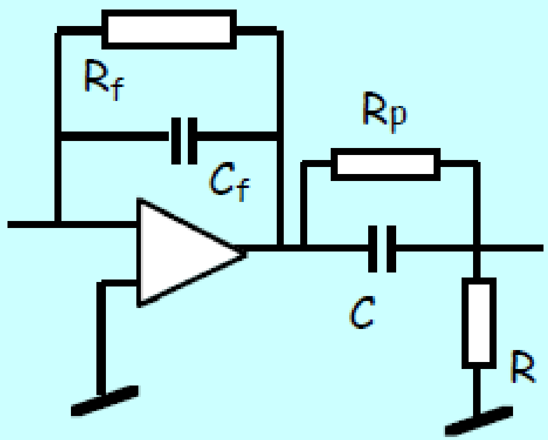
  $v_1 = 1/(1 + j\omega\tau_f)(1 + j\omega\tau_1)$

  $\tau_1 = RC < \tau_f$

  add resistor R_p so $R_p C = \tau_f$

  then

  $v_1' = 1/(1 + j\omega\tau_3)$ with $\tau_3 = (R||R_p)C < \tau_f$



Need for pulse shaping

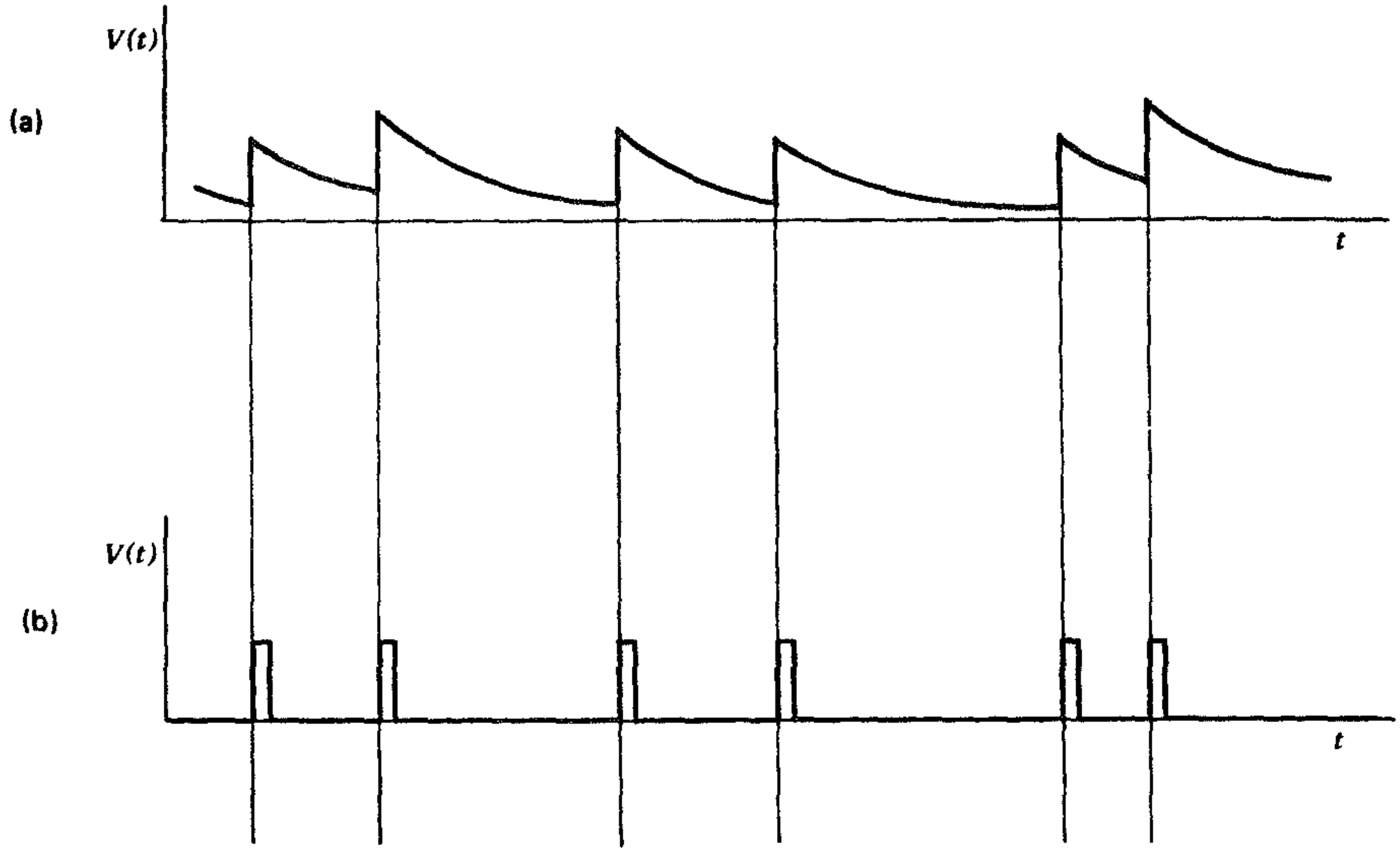
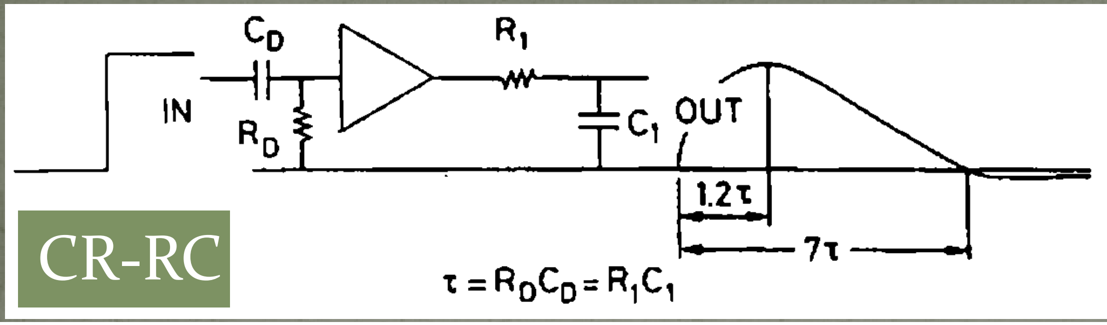


Figure 16.8 The pulses with long tails shown in part (*a*) illustrate the apparent variation in amplitude due to pulse pile-up. These effects can greatly be reduced by shaping the pulses as in part (*b*).

Pulse shaping

- Amplifiers must preserve the information of interest
  - If timing required: fast response
  - If pulse height required: strict proportionality, limit bandwidth
- Preamplifier pulse
  - Exponential with long tail
  - Pulse pileup: Reduce counting rate or reshape
- Optimization of signal-to-noise ratio
  - For a given noise spectrum, there exists an optimum pulse shape to improve the S/N
  - For ex: Tail pulses in presence of typical noise spectra are not ideal
  - Triangular or Gaussian – symmetric pulse shapes are ideal
- Fast amplifiers: No or very little shaping
- What to do in case you need good timing and pulse height information?

CR-RC pulse shapers



Pole-Zero Cancellation

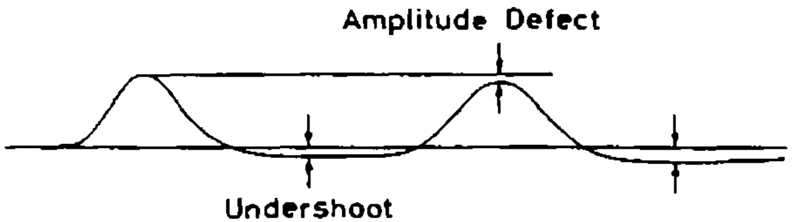


Fig. 14.6. Amplitude defect arising from undershoot in CR-RC pulse shaping

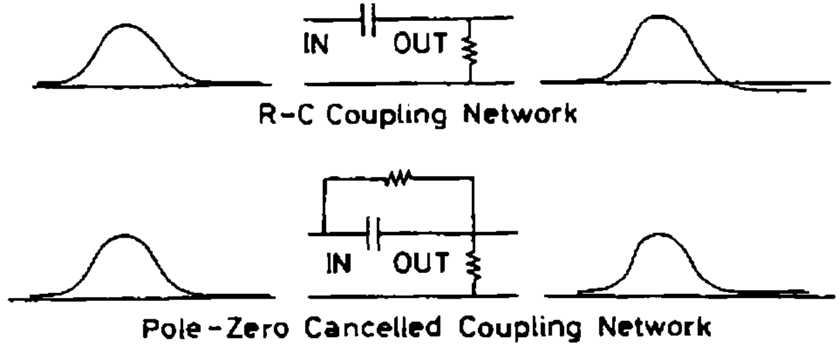
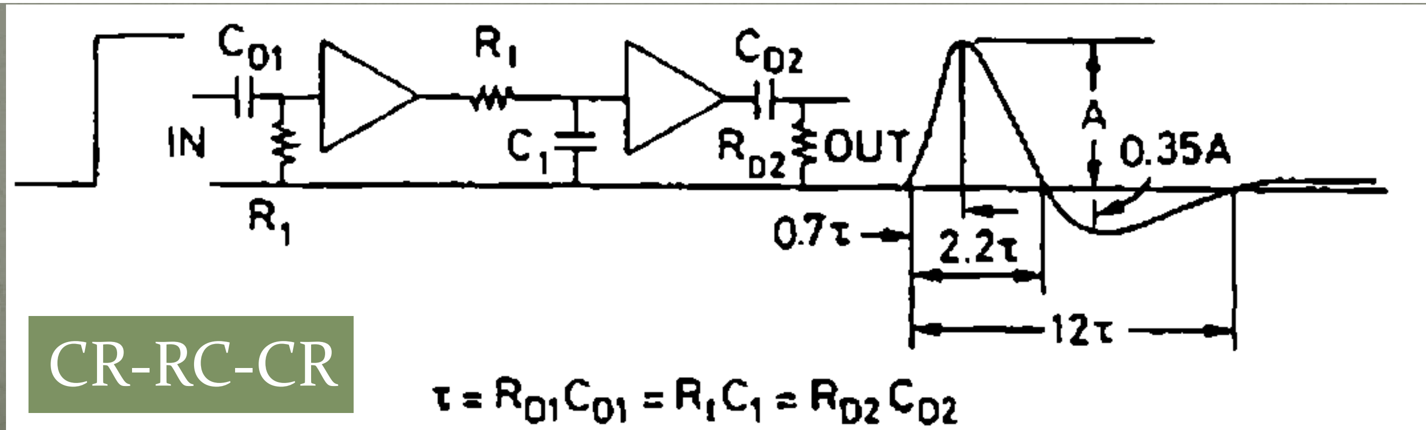


Fig. 14.7. Pole-zero cancellation circuit (from *Ortec* catalog [14.1])



Response of CR-RC shaper

$$E_{out} = \frac{E\tau_1}{\tau_1 - \tau_2}\left(e^{-t/\tau_1} - e^{-t/\tau_2}\right) \tag{16.22}$$

where τ_1 and τ_2 are time constants of the differentiating and integrating networks, respectively. Plots of this response for several different combinations of τ_1 and τ_2 are shown in Fig. 16.12.

In nuclear pulse amplifiers, *CR-RC* shaping is most often carried out using equal differentiation and integration time constants. In that event, Eq. (16.22) becomes indeterminant, and a particular solution for this case is

$$E_{out} = E\frac{t}{\tau}e^{-t/\tau} \tag{16.23}$$

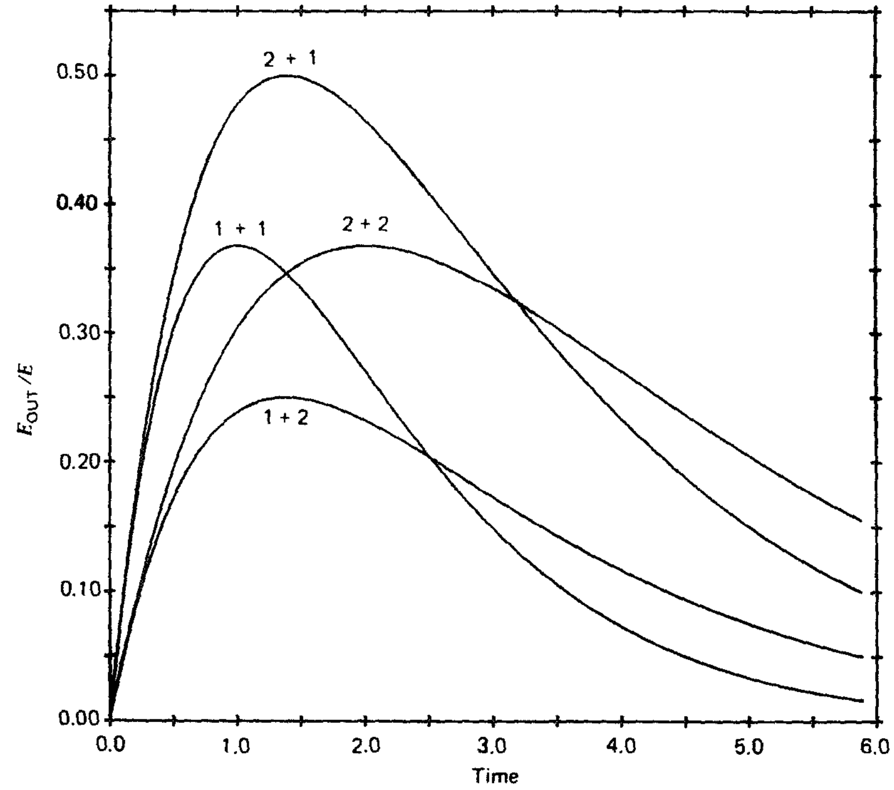


Figure 16.12 The response of a *CR-RC* network to a step voltage input of amplitude E at time zero. Curves are shown for four pairs of differentiator + integrator time constants. Units of the time constants and time scale are identical.

Pole-zero cancellation

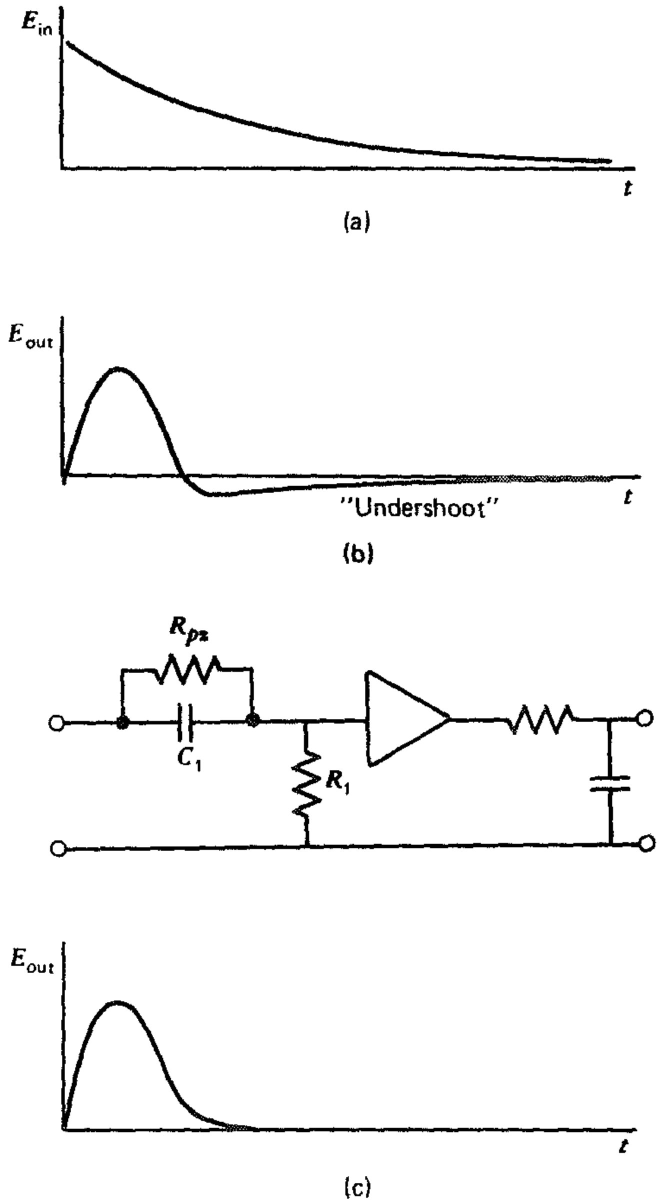
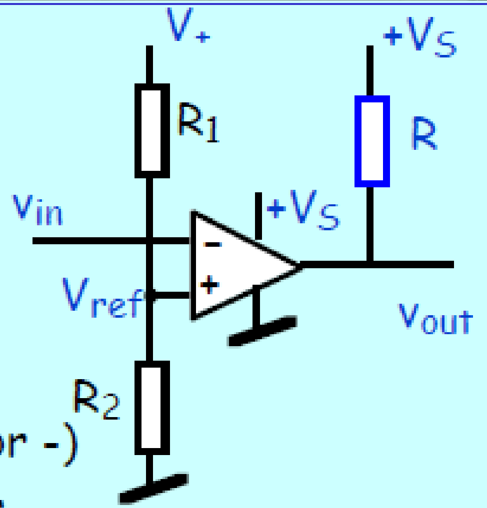


Figure 16.15 Application of pole-zero cancellation to eliminate the undershoot (*b*) normally generated by a *CR*-*RC* shaping network for an input step with finite decay time. By adding an appropriate resistance R_{pz} to the differentiator stage, a waveform without undershoot (*c*) can be obtained.

Discriminators

- Frequently need to compare a signal with a reference
  - eg temperature control, light detection, DVM,...
  - basis of analogue to digital conversion -> 1 bit
- Comparator
  - high gain differential amplifier,
    - difference between inputs sends output to saturation (+ or -)
  - could be op-amp - without feedback - or purpose designed IC
  - Sometimes ICs designed with open-collector output so add pull-up R to supply
    - also available with latch (memory) function



- NB
  - no negative feedback so $v_- \neq v_+$
  - saturation voltages may not reach supply voltages - check specs
  - speed of transition
- Potential problem
  - multiple transitions as signal changes near threshold

Hysteresis

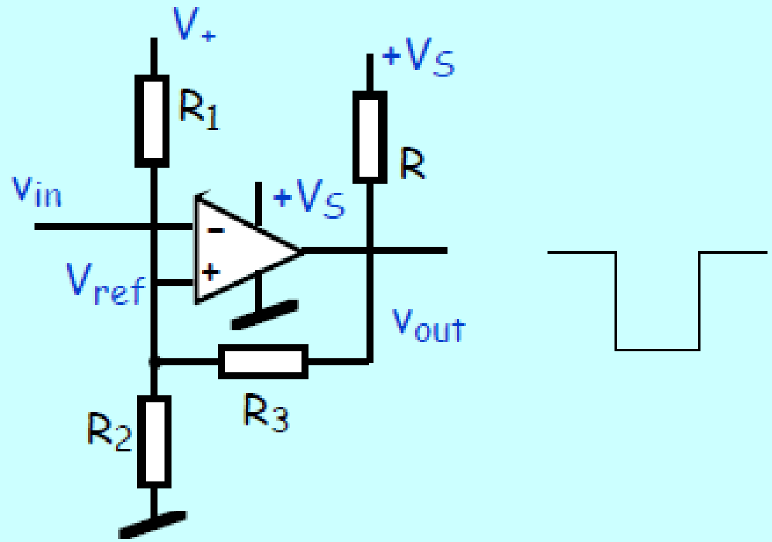
- Add positive feedback (Schmitt trigger)
  - V_{ref} changes as v_{out} -> $+V_S$
  - ie threshold falls once transition is made
  - preventing immediate fall
  - positive feedback speeds transition

$$v_{out} = A(V_{ref} - v_-)$$

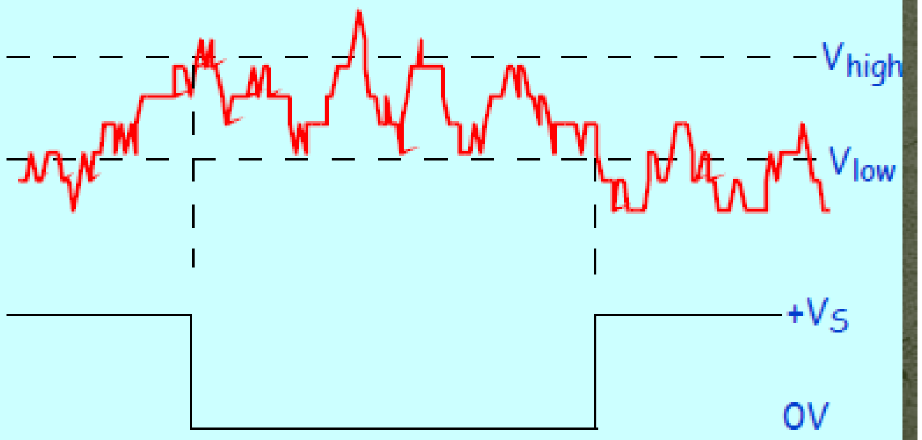
$V_{ref} > v_-$ => $v_{out} = V_s$ $V_{ref} = V_{high}$

$V_{ref} < v_-$ => $v_{out} = 0V$ $V_{ref} = V_{low}$

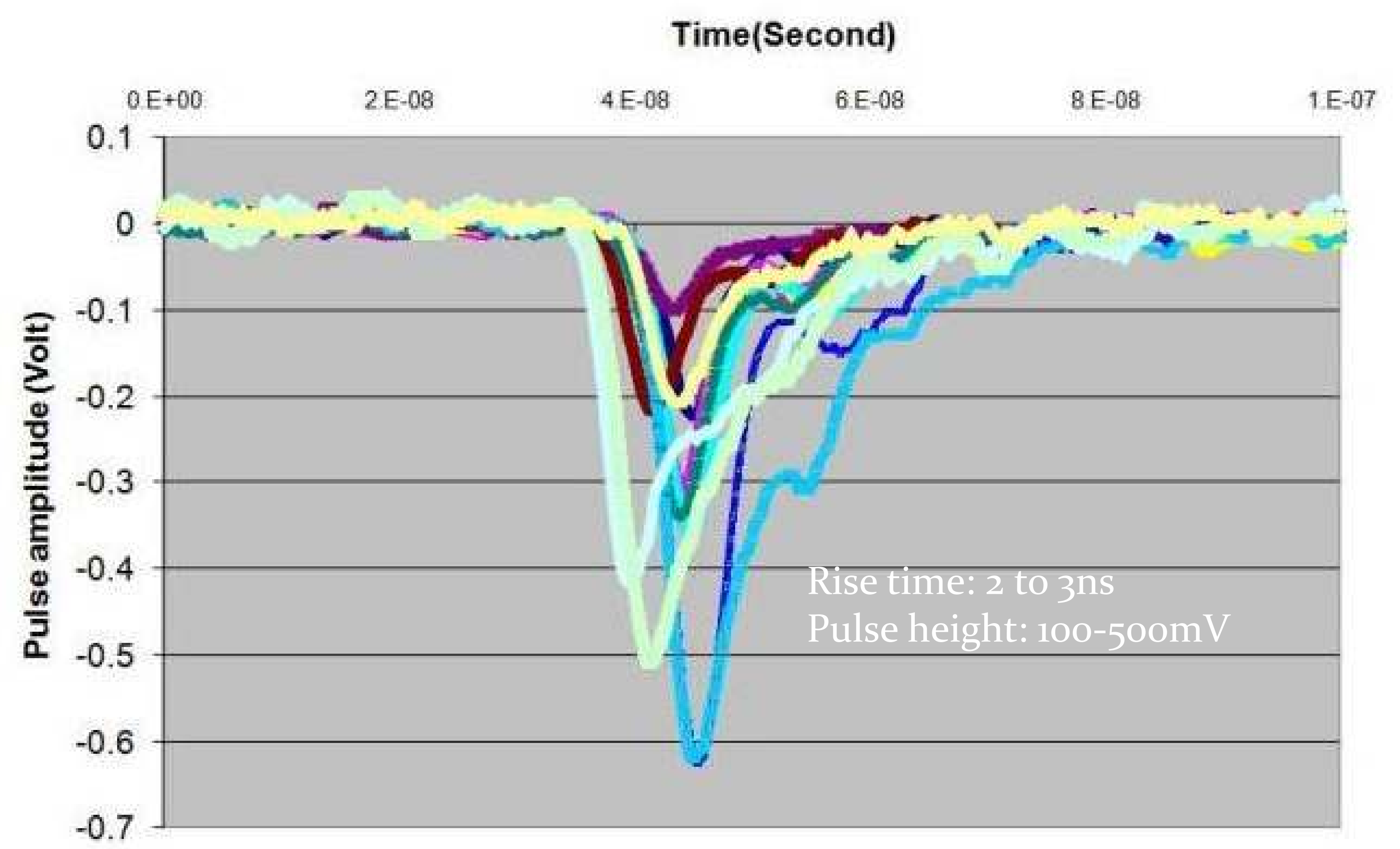
  - here, signal => logical "1": $v_{out} = 0V$



- Output depends on history
  - eg $V_+ = 10V$, $V_S = +5V$, 0V
  - $R_1 = 10k\Omega$, $R_2 = 10k\Omega$, $R_3 = 100k\Omega$
  - $V_{out} = 0V$, $V_{ref} = 4.76V$
  - $V_{out} = 5V$, $V_{ref} = 5V$
  - hysteresis = $\Delta V_{ref} = 0.24V$

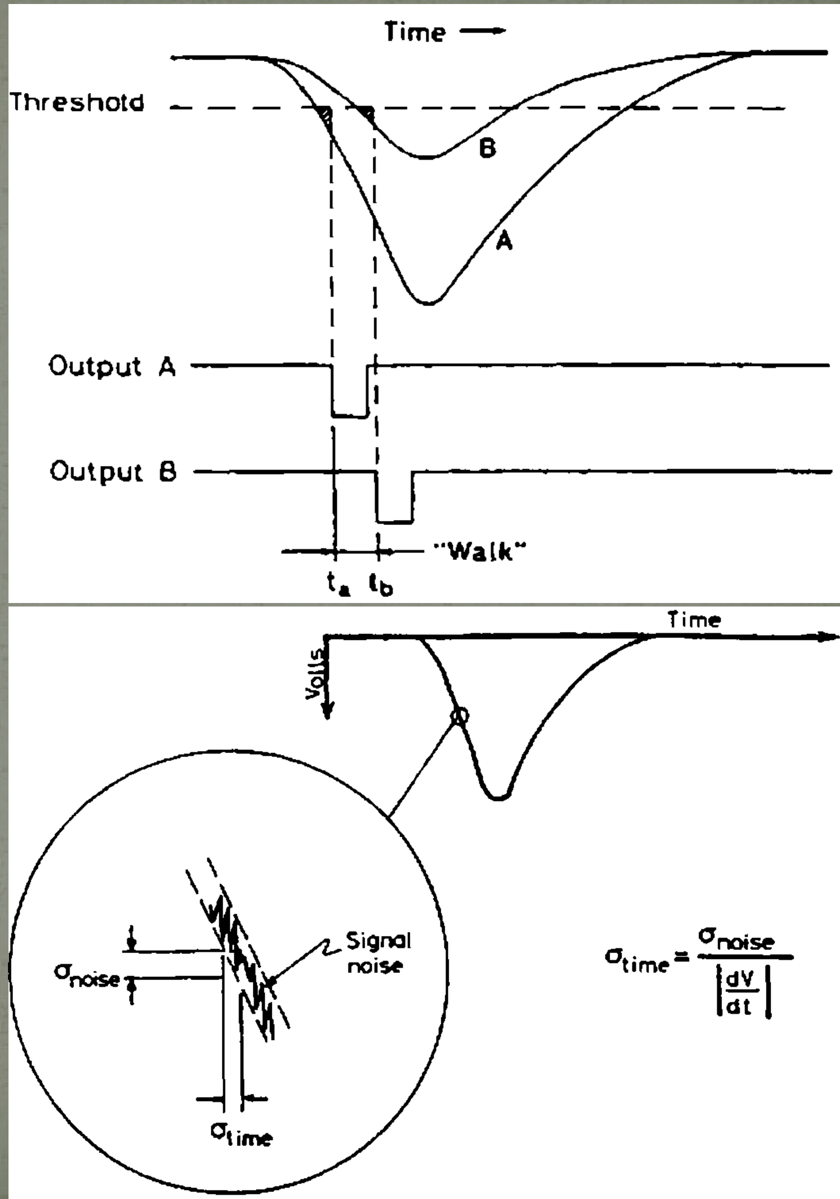


RPC's preamp output pulses



Two common problems

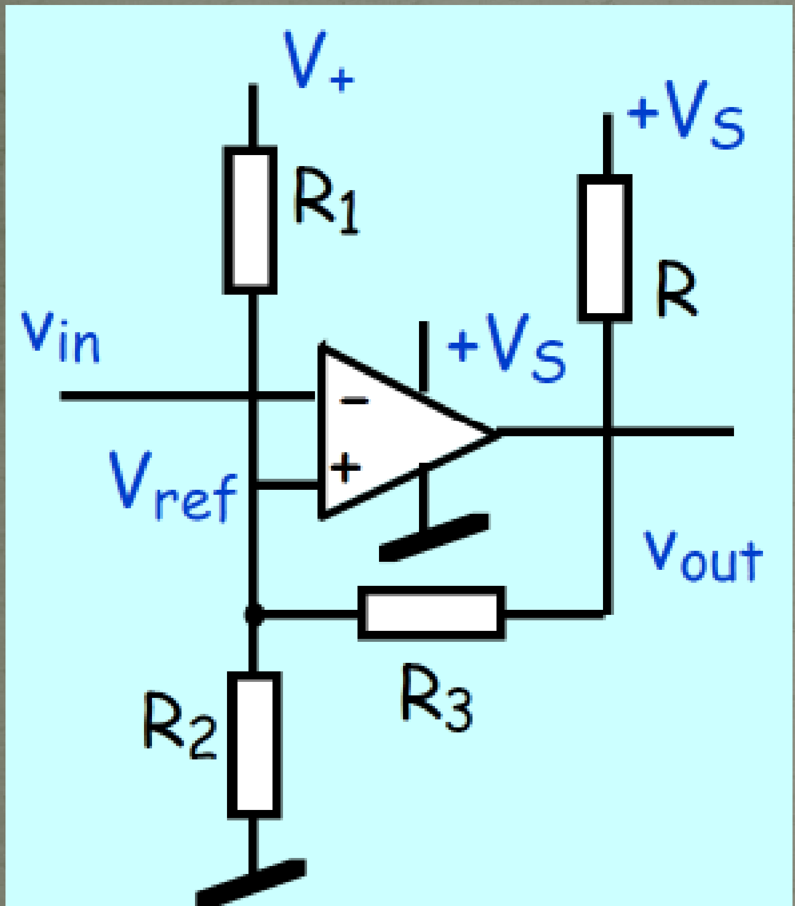
- Walk (due to variations in the amplitude and rise time, finite amount of charge required to trigger the discriminator)
- Jitter (due to intrinsic detection process – variations in the number of charges generated, their transit times and multiplication factor etc.)



Considerations for discriminators

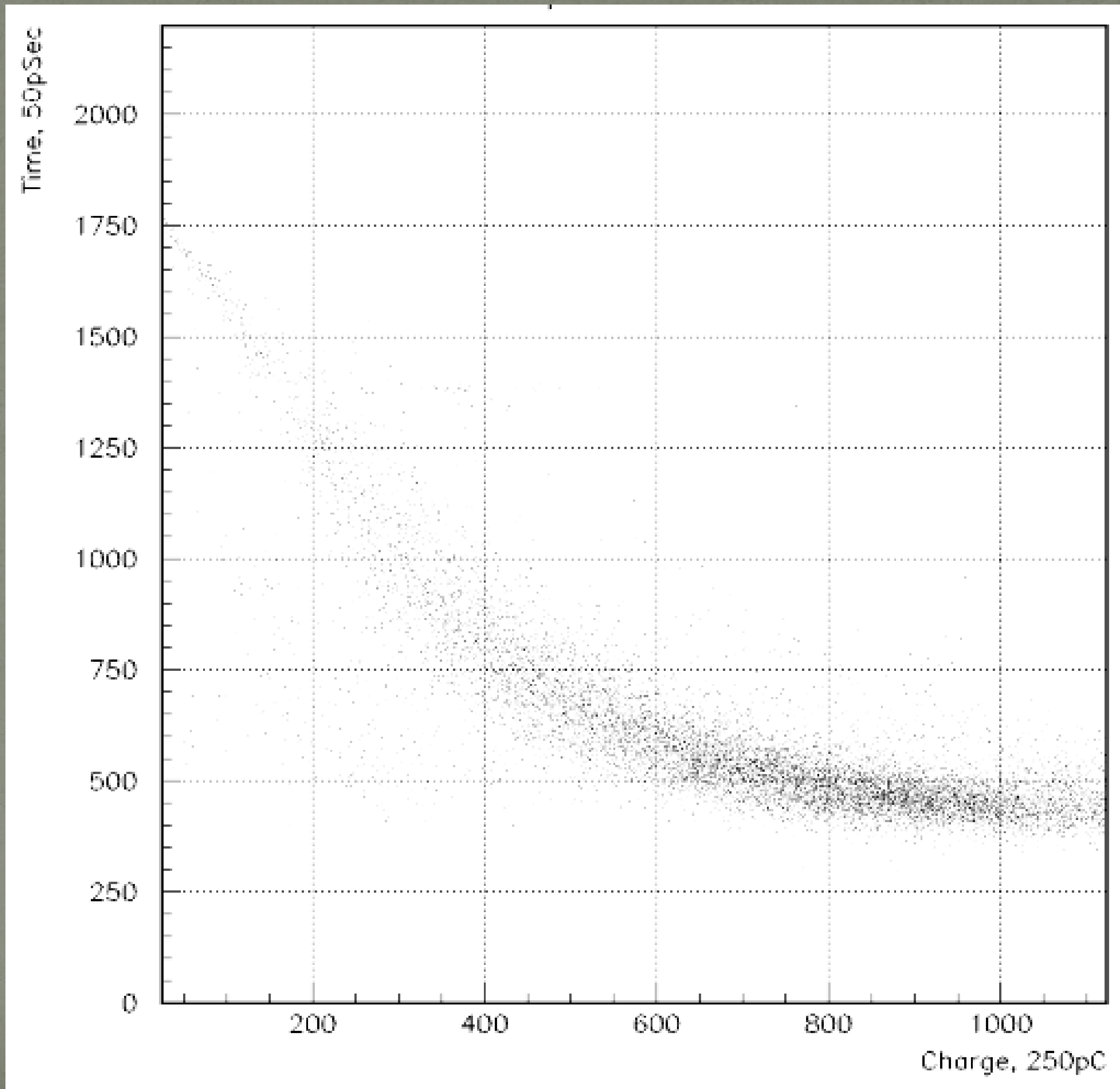
- Two common problems
  - Walk
  - Jitter
- Time-Pickoff methods
  - Leading edge triggering
  - Fast zero-crossing triggering
  - Constant fraction triggering
  - Amplitude and risetime compensated triggering

Leading edge discriminators



- Fine with if input amplitudes restricted to small range.
- For example:
  - With 1 to 1.2 range, resolution is about 400ps.
  - But at 1 to 10 range, the walk effect increases to ±10ns.
- That will need off-line corrections for time-walk using charge or time-over-threshold (TOT) measurements.

Off-line corrections of time-walk



Zero-crossing and Constant fraction

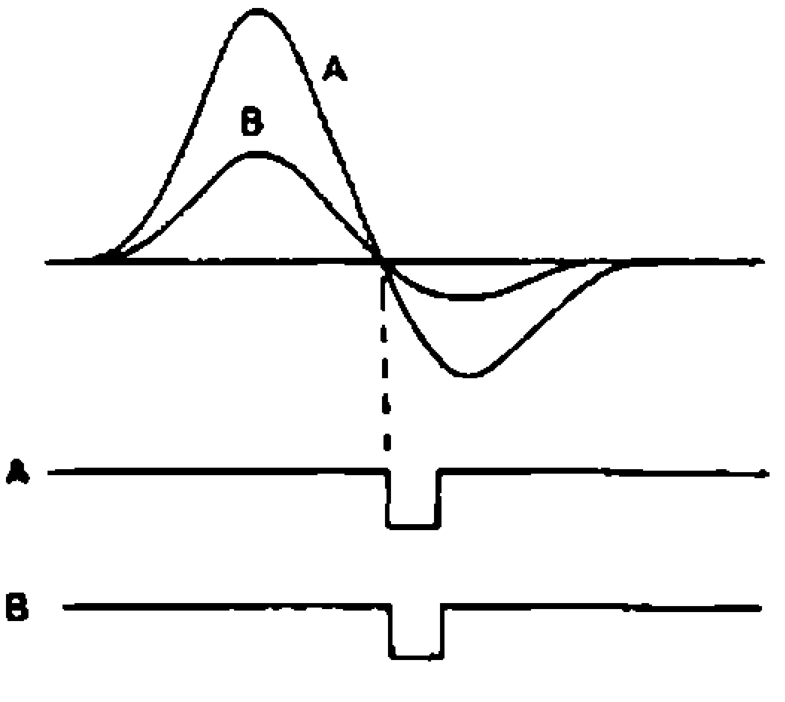


Fig. 17.3. Zero-crossing timing. Variations in the cross-over point are known as *zero-crossing walk*

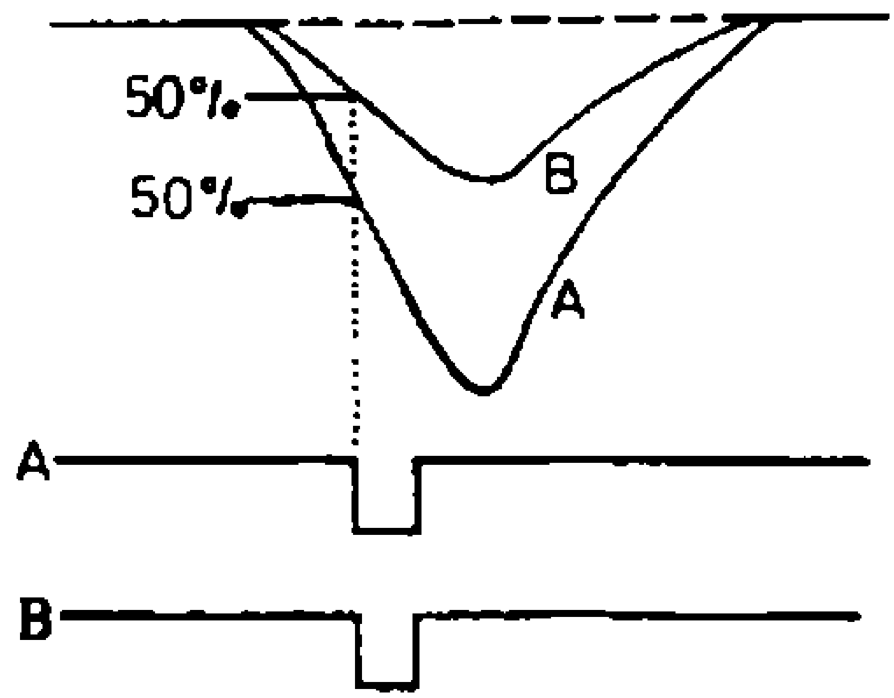


Fig. 17.4. Constant fraction discrimination

❖Zero-crossing triggering:

- Timing resolution 400ps, if amplitude range is 1 to 1.2
- Timing resolution 600ps, even if the amplitude range is 1 to 10
- But, requires signals to be of constant shape and rise-time.

Constant fraction triggering

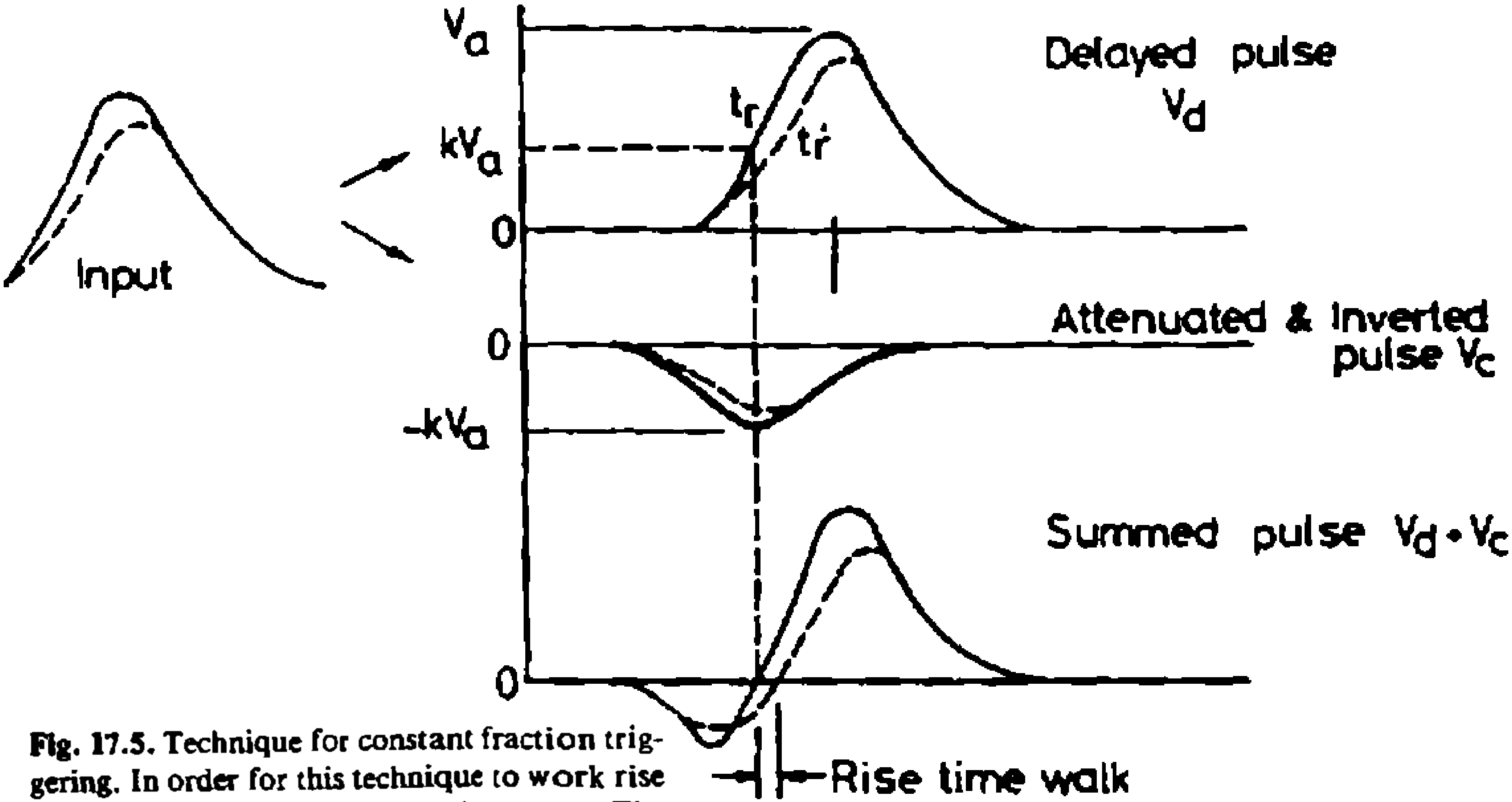
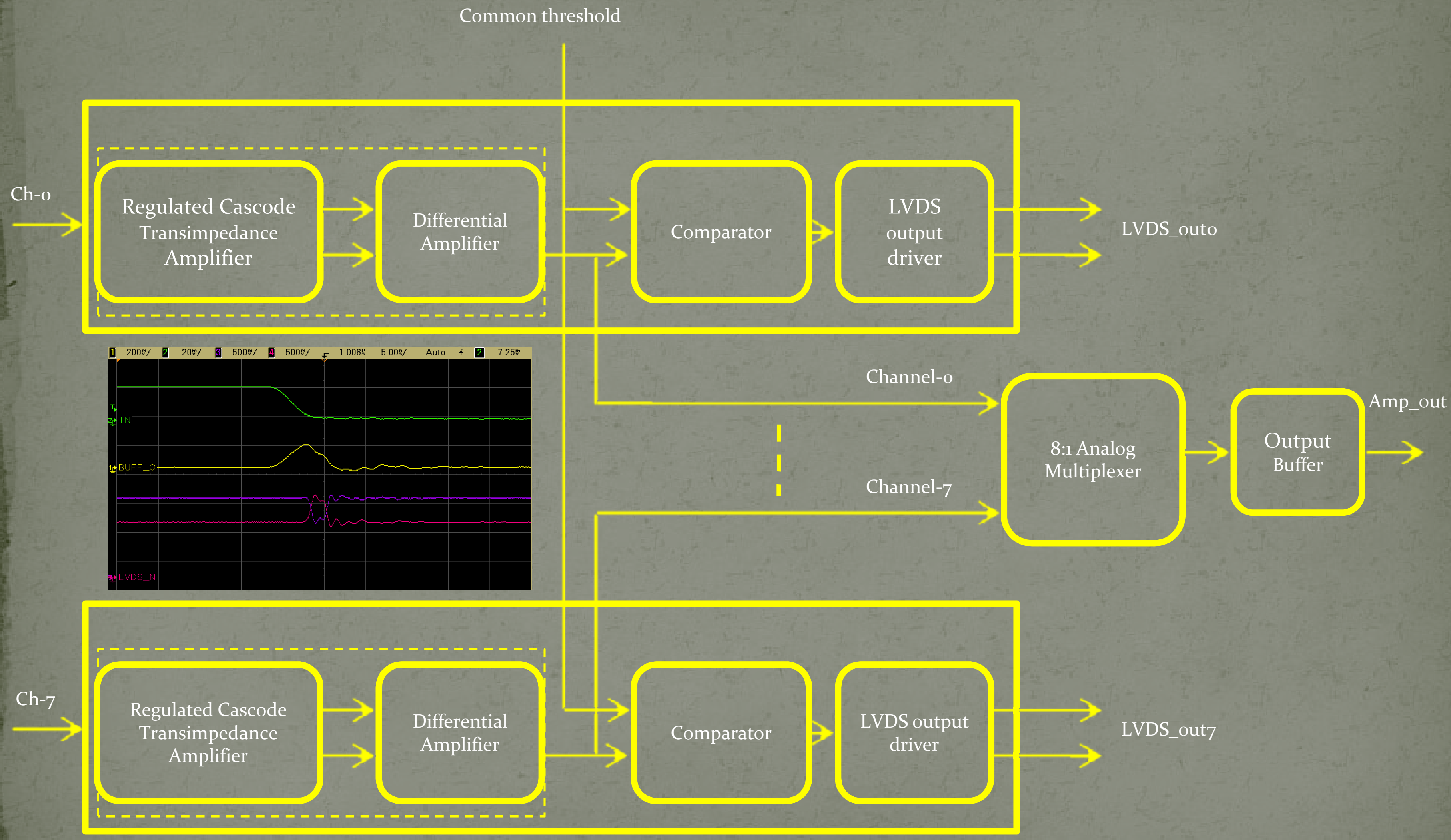
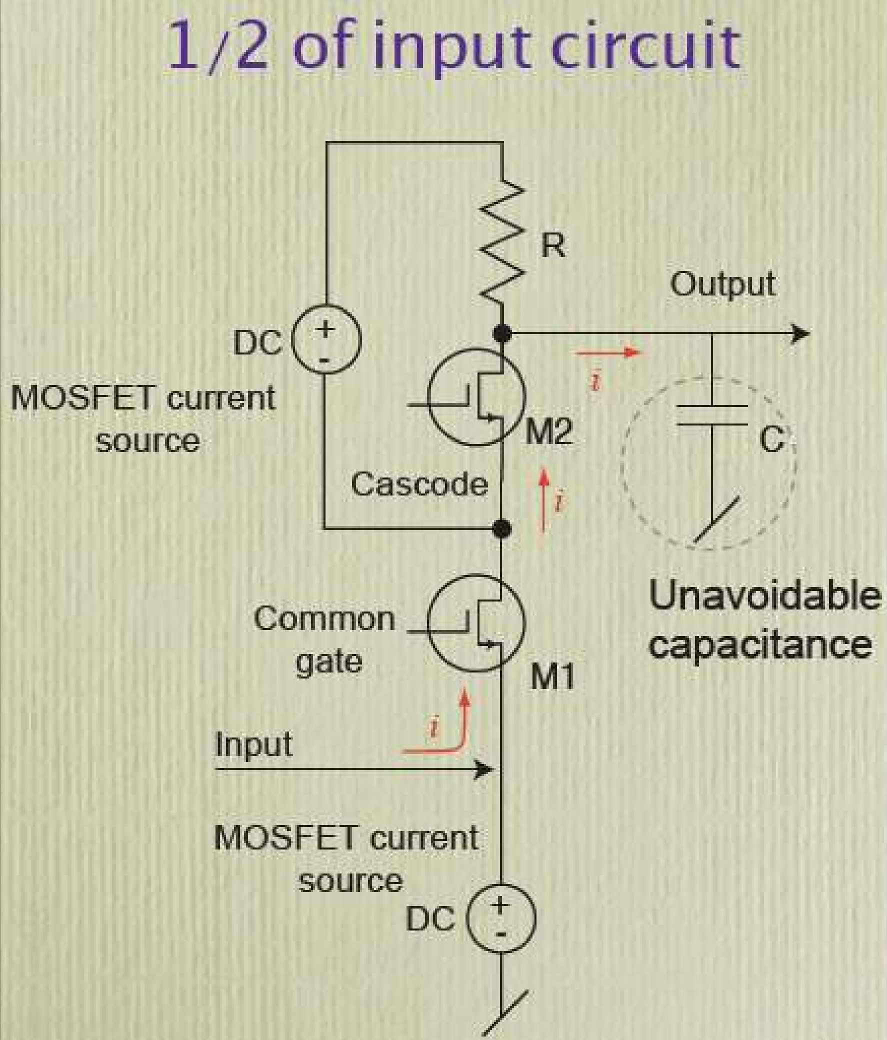


Fig. 17.5. Technique for constant fraction triggering. In order for this technique to work rise times of all signals must be the same. The dotted line shows the result with a different rise time signal

Functional diagram of FE ASIC

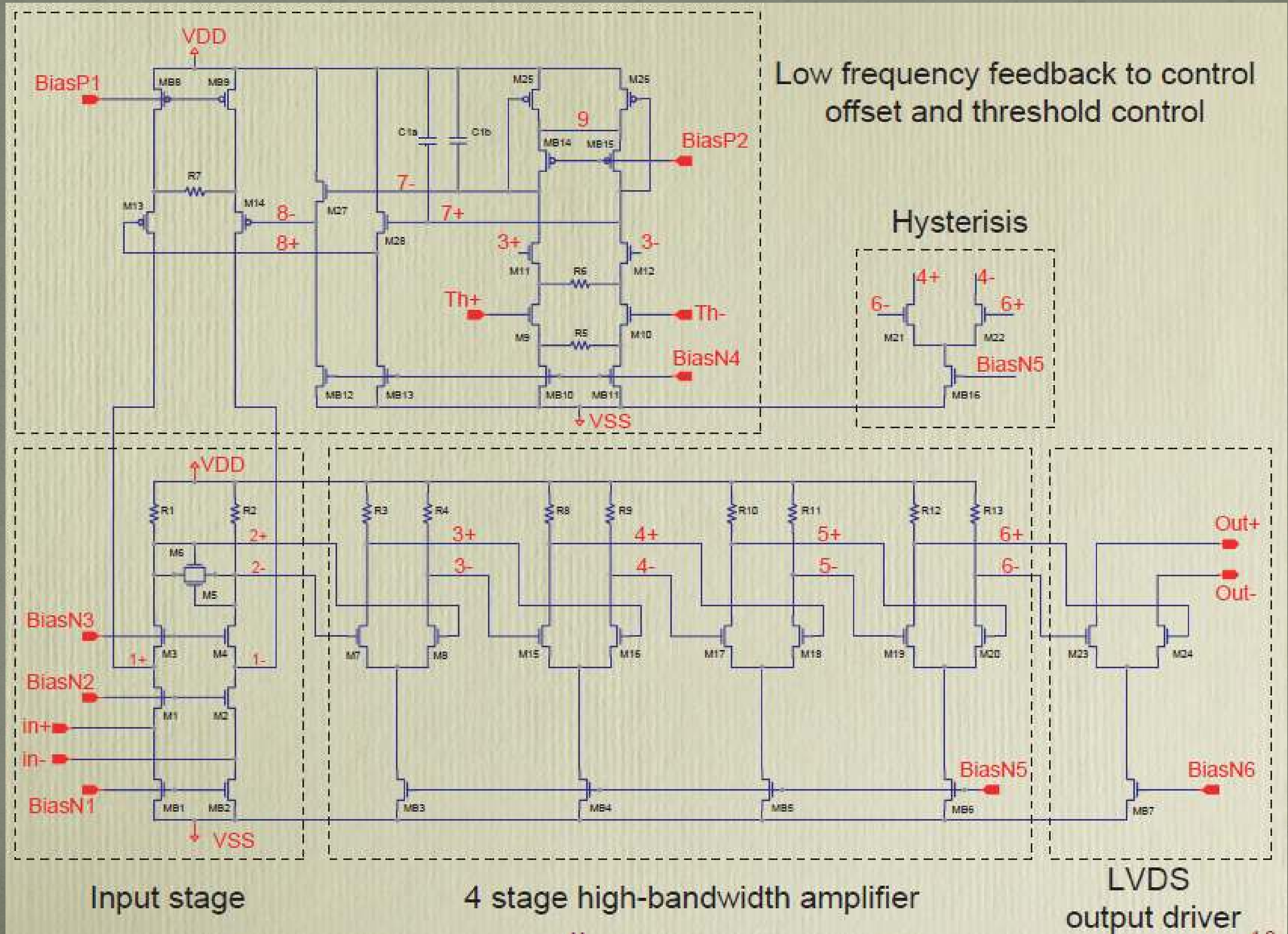


NINO input stage



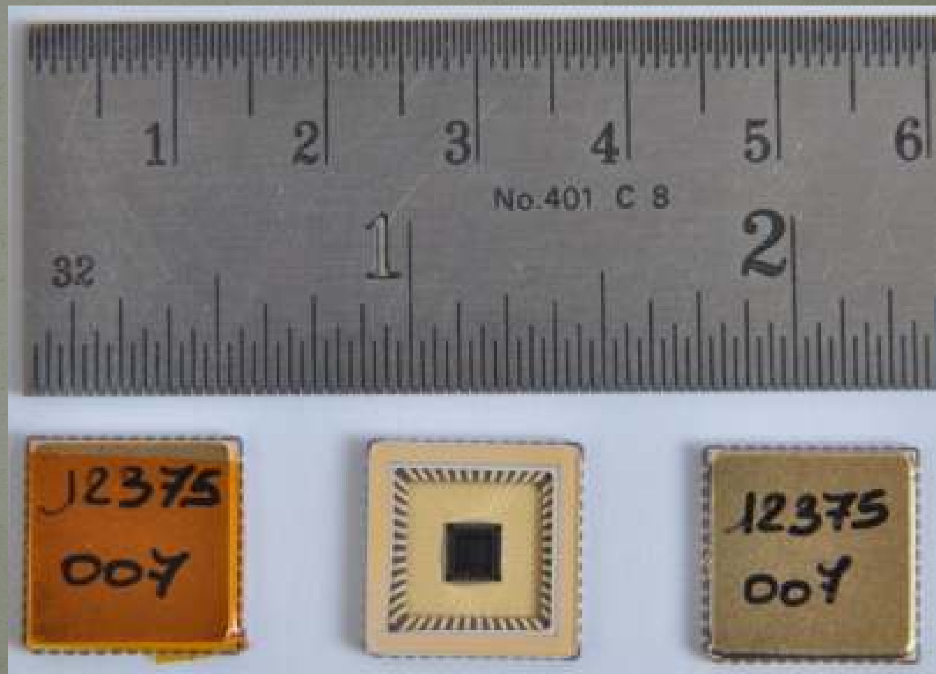
- The input current flows through the two transistors and charges the capacitor at the output (need to minimise C for maximum voltage)
- Trailing-edge of voltage pulse at output has RC time constant
- The impedance seen at the input is mainly the $1/g_m$ of the input transistor.
- The advantage of this configuration is the high bandwidth with excellent stability due to the absence of feedback element.

Complete circuit of NINO chip

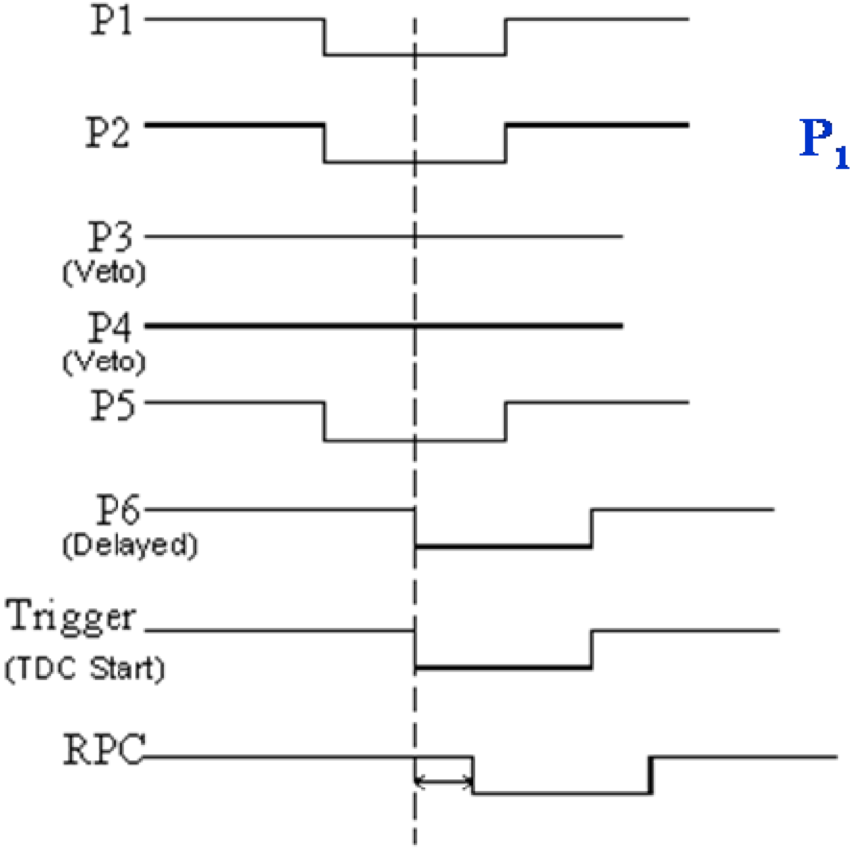


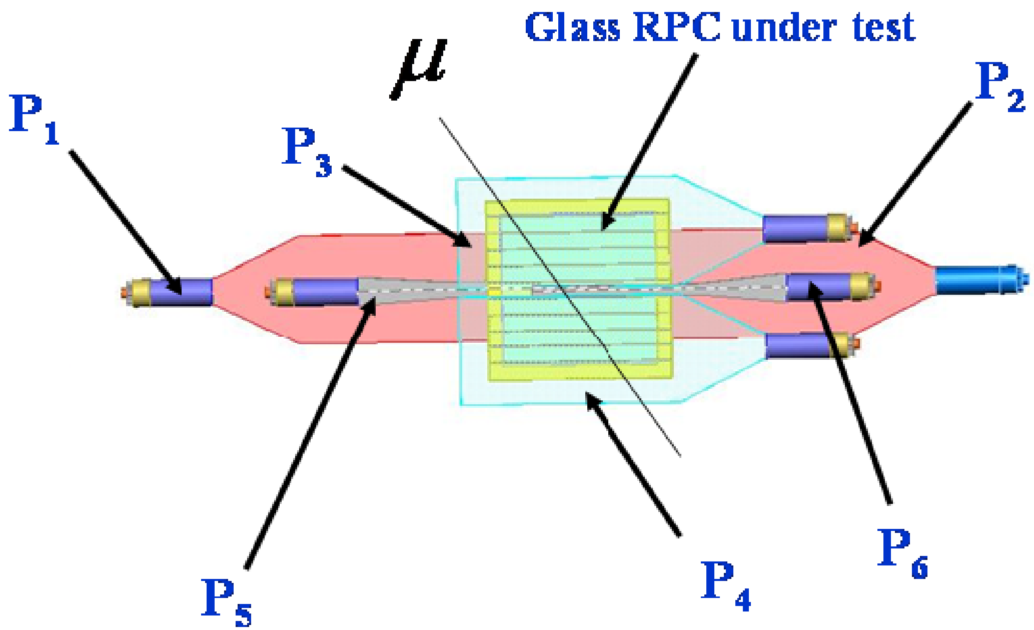
Features of ICAL FE ASIC

- IC Service: Europractice (MPW), Belgium
- Service agent: IMEC, Belgium
- Foundry: austriamicrosystems
- Process: AMSc35b4c3 (0.35µm CMOS)
- Input dynamic range:18fC – 1.36pC
- Input impedance: 45Ω @350MHz
- Amplifier gain: 8mV/µA
- 3-dB Bandwidth: 274MHz
- Rise time: 1.2ns
- Comparator's sensitivity: 2mV
- LVDS drive: 4mA
- Power per channel: < 20mW
- Package: CLCC48(48-pin)
- Chip area: 13mm²



Coincidence scheme for a muon telescope



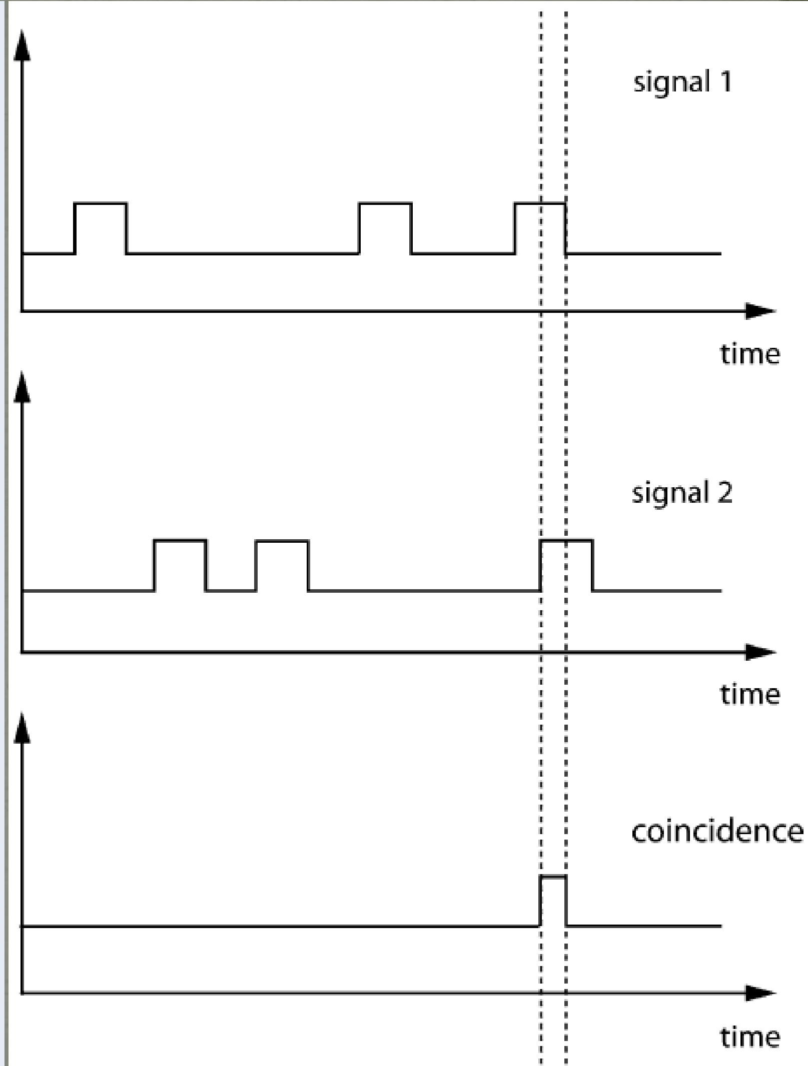


Muon Trigger = $P_1 \bullet P_2 \bullet \overline{P_3} \bullet \overline{P_4} \bullet P_5 \bullet P_6$

Coincidence of signals

- To see if an event occurred simultaneously with some other event, the electronics will look for the simultaneous presence of two logical signals within some time Window.
- In coincidence counting, one should be aware of the possibility to have random coincidences.
- These are occurrences of a coincidence caused by two unrelated events arriving by chance at the same time.
- The rate of random coincidences between two signals is proportional to the rate of each type of signal times the duration of the coincidence window.

$$\frac{dN_{random}}{dt} = \frac{dN_1}{dt} \times \frac{dN_2}{dt} \times \Delta t$$



Basic coincidence technique

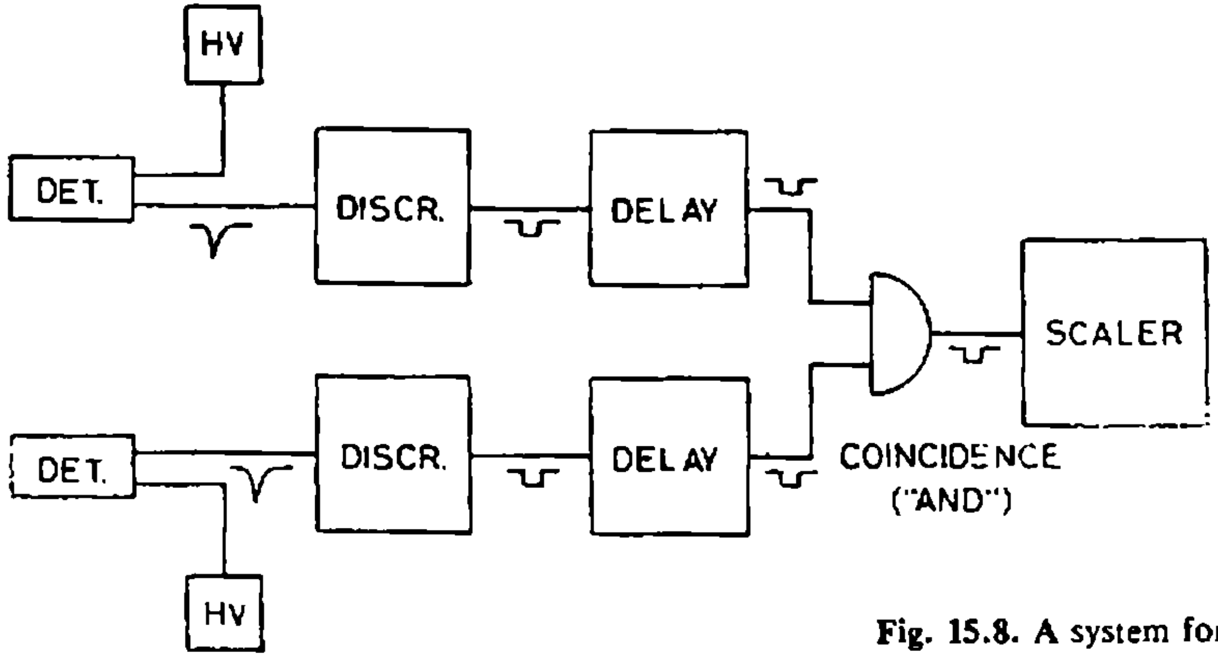


Fig. 15.8. A system for coincidence measurement

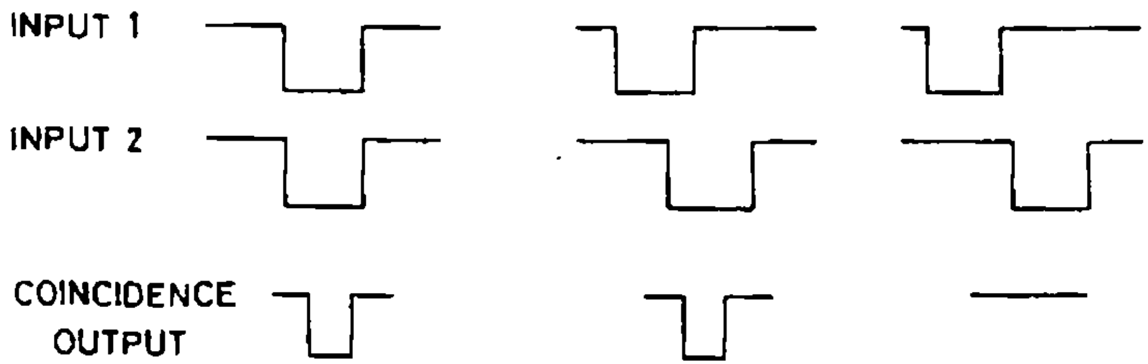
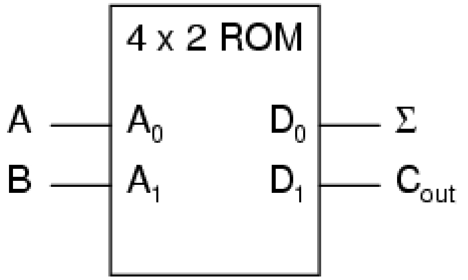
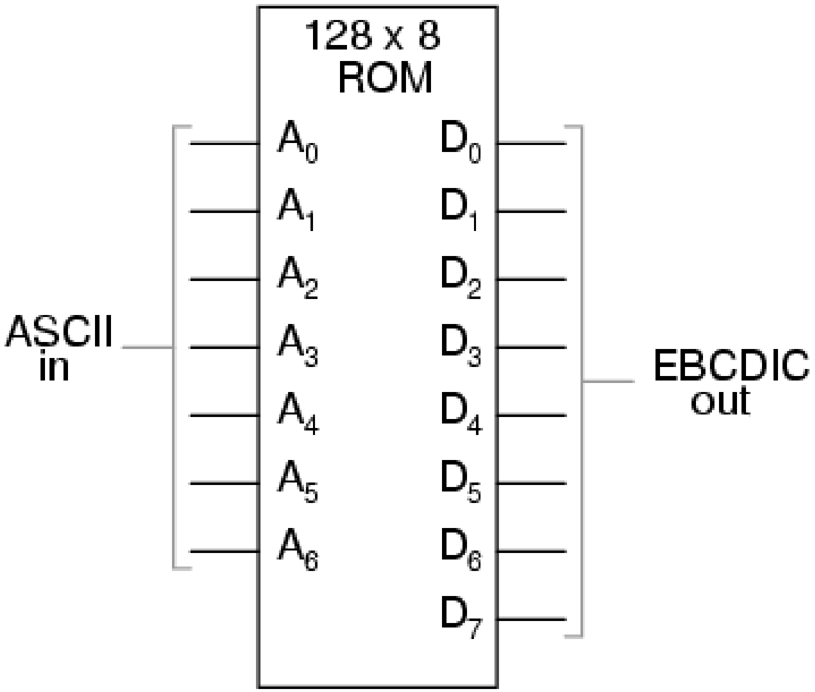


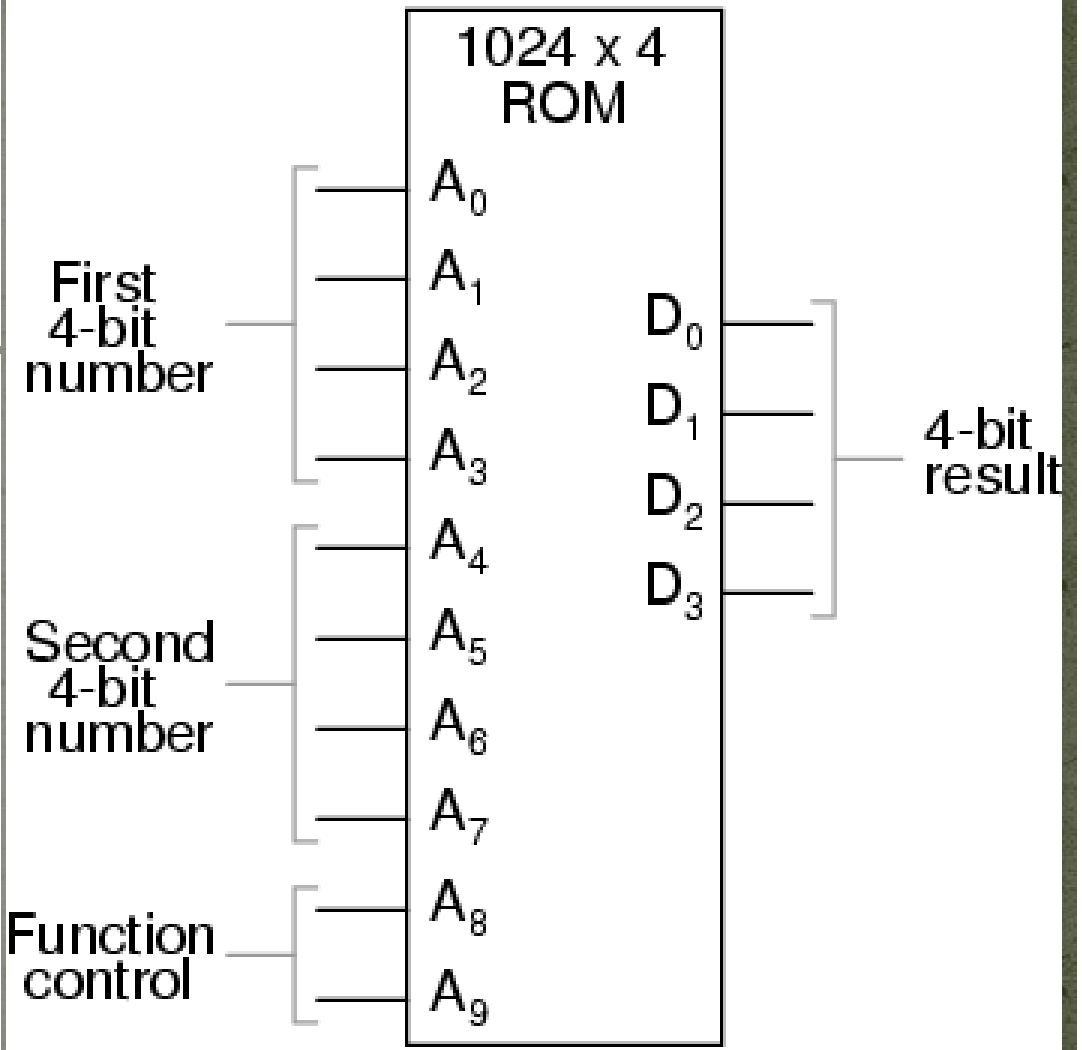
Fig. 15.9.
Coincidence between pulses

Memory-lookup tables



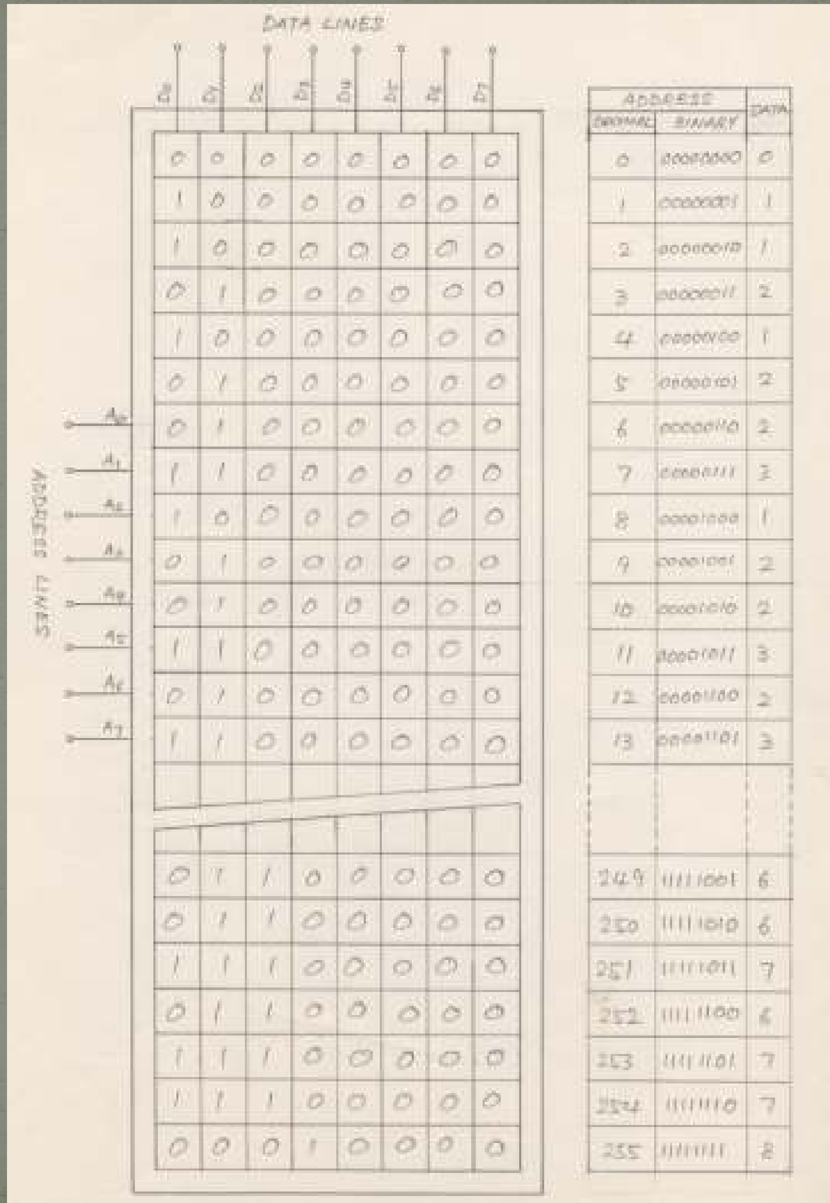
Address		Data	
A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0





Lookup table for trigger generation

Can be implemented in memories or modern VLSI devices, adds flexibility to the system.



D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
1	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0
1	1	0	0	0	0	0	0
1	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0
1	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0
1	1	0	0	0	0	0	0
0	1	1	0	0	0	0	0
0	1	1	0	0	0	0	0
1	1	1	0	0	0	0	0
0	1	1	0	0	0	0	0
1	1	1	0	0	0	0	0
1	1	1	0	0	0	0	0
0	0	0	1	0	0	0	0

ADDRESS		DATA
DECIMAL	BINARY	
0	00000000	0
1	00000001	1
2	00000010	1
3	00000011	2
4	00000100	1
5	00000101	2
6	00000110	2
7	00000111	3
8	00001000	1
9	00001001	2
10	00001010	2
11	00001011	3
12	00001100	2
13	00001101	3
249	11111001	6
250	11111010	6
251	11111011	7
252	11111100	6
253	11111101	7
254	11111110	7
255	11111111	8

Lecture - III

Wednesday, January 30, 2013

- ✓ Analog-to-Digital Converters
- ✓ Spectroscopy systems
- ✓ Time-to-Digital Converters
- ✓ Waveform digitisers

Analogue to Digital Conversion

- Turns electrical input (voltage/charge) into numeric value
- Parameters and requirements
  - Resolution
    - the granularity of the digital values
  - Integral Non-Linearity
    - proportionality of output to input
  - Differential Non-Linearity
    - uniformity of digitisation increments
  - Conversion time
    - how much time to convert signal to digital value
  - Count-rate performance
    - how quickly a new conversion can begin after a previous event
  - Stability
    - how much values change with time

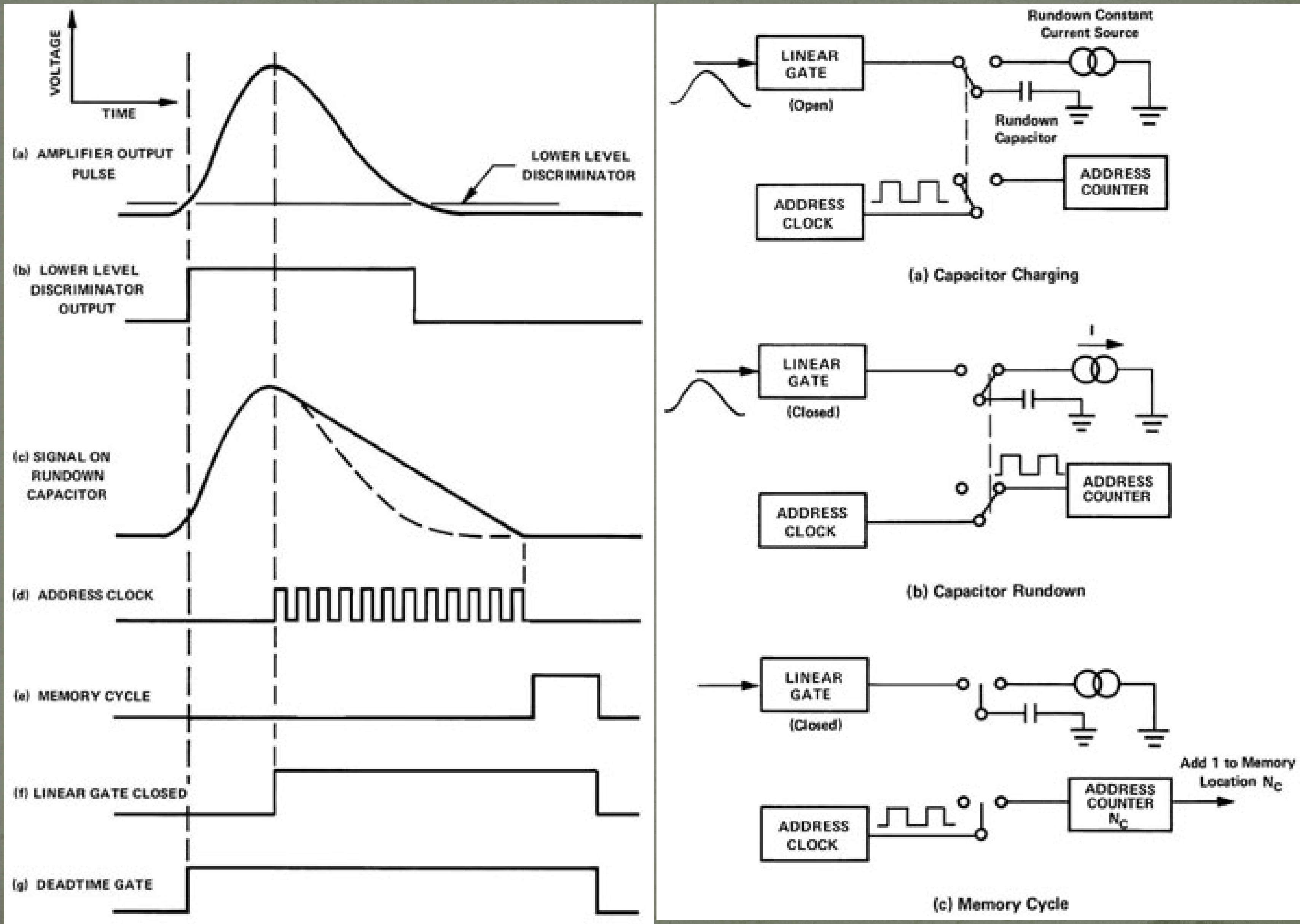
Analog-to-Digital Converters (ADCs)

- Peak-sensing
  - Maximum of the voltage signal is digitised
  - Ex: Signal of the PMT in voltage mode (slow signals, already integrated)
- Charge sensitive
  - Total integrated current digitised
  - Ex: Signal of the PMT in the current mode (fast signals)
- Time of integration or the time period over which the ADC seeks a maximum is determined by the width of the gate signal

Types of ADCs

- ❖ Ramp or Wilkinson
- ❖ Successive approximation
- ❖ Flash or parallel
- ❖ Sigma-delta ADC
- ❖ Hybrid (Wilkinson + successive approximation)
- ❖ Tracking ADC
- ❖ Parallel ripple ADC
- ❖ Variable threshold flash ADC
- ❖ …

Ramp or Wilkinson ADC



Successive approximation ADC

- analogous to binary search

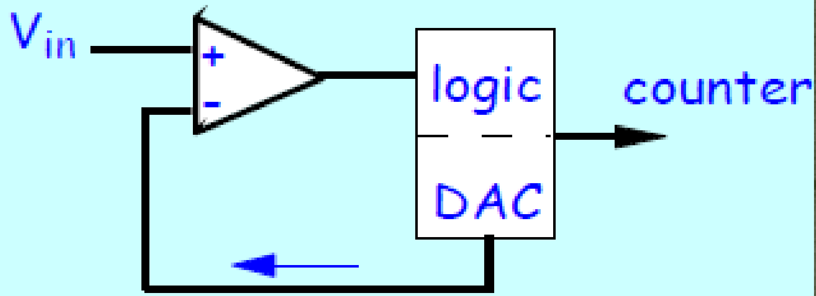
  generate $V_{ref} = \Delta V \times (2^{N-1}, 2^{N-2}, \ldots 2^0)$ in N steps

  set bit = 1

  if $V_{in} > V_{ref}$

  leave

  else bit = 0



DAC = digital to analogue converter
ie number -> voltage

- Pros

  speed ~ *µsec*

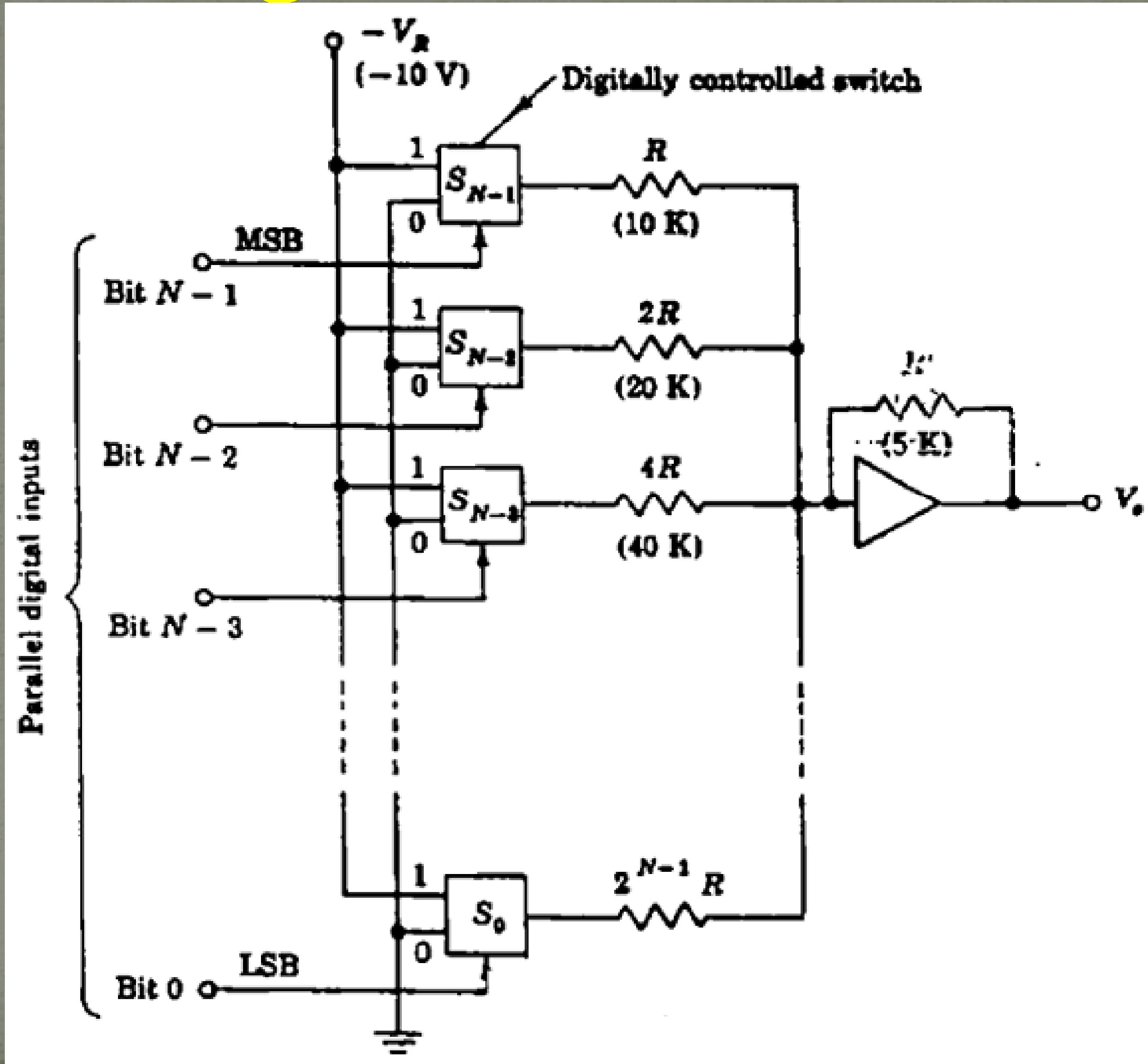
  high resolution

- Cons

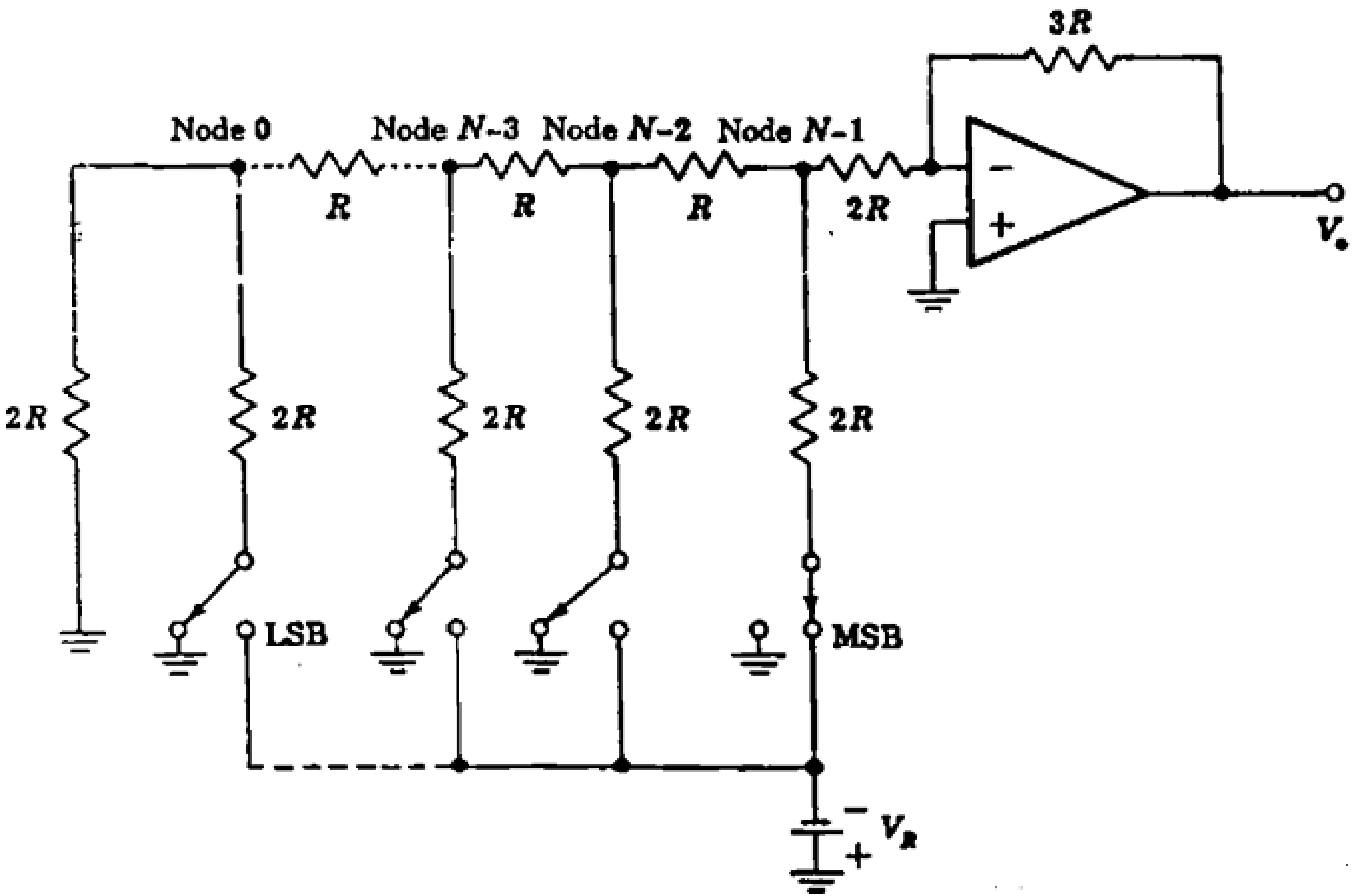
  DNL 10-20%

  very precise resistors required with DAC for V_{ref}

Weighted resistor DAC

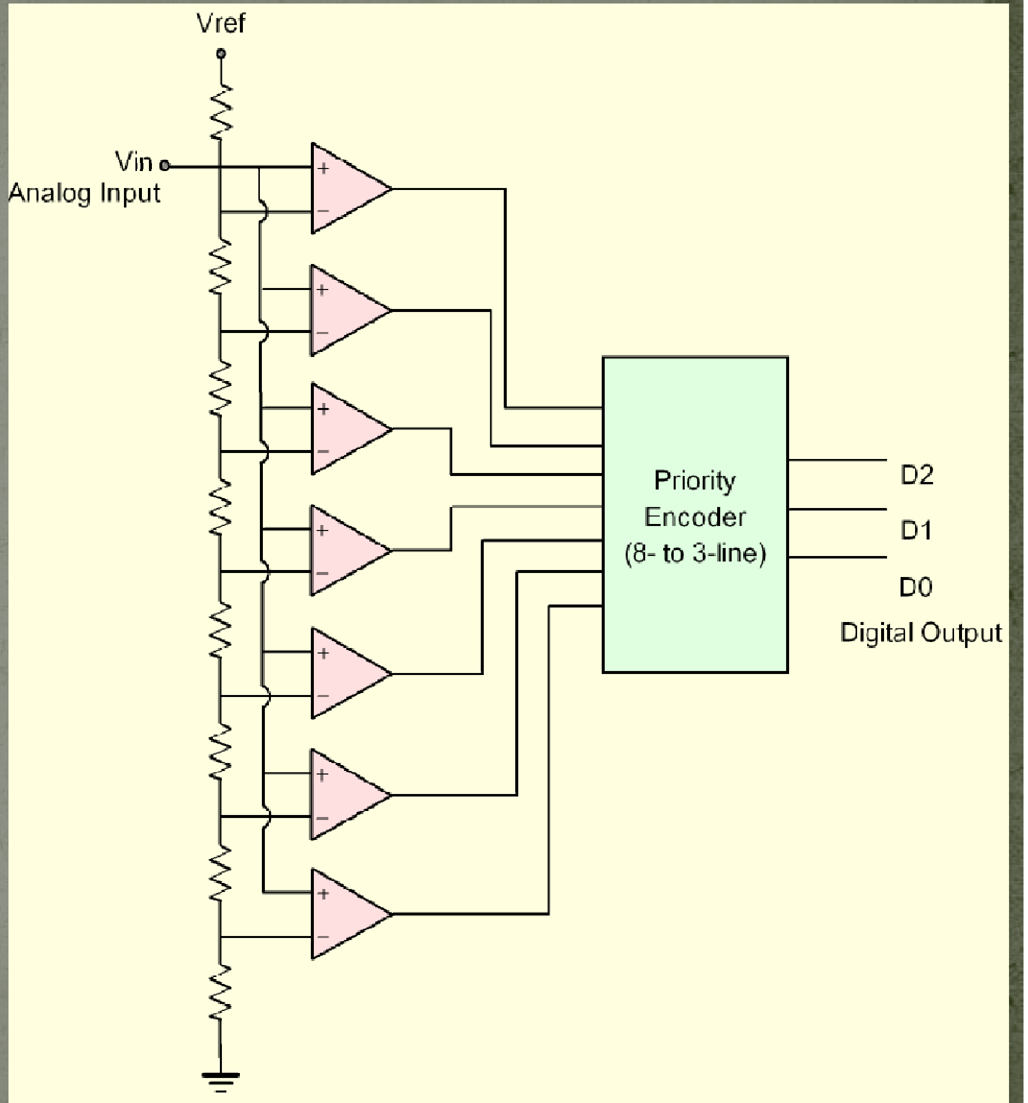


R-2R ladder DAC



Flash or parallel ADC

- Flash ADC is the fastest ADC type available. The digital equivalent of the analog signal will be available right away at it output – hence the name "flash".
- The number of required comparators is $2^n - 1$, where n is the number of output bits.
- Since Flash ADC comparisons are set by a set of resistors, one could set different values for the resistors in order to obtain a non-linear output, i.e. one value would represent a different voltage step from the other values.



Sigma-delta ADC

- Digitise the signal with 1-bit resolution at a high sampling rate (MHz).

  useful for high resolution conversion of low-frequency signals, to 20bits

  low-distortion conversion of audio signals

  good linearity and high accuracy.

- Operation - At t = 0, assume V_{ref} = 0

  V_{out} high

  integrator charges -ve

  at rate ~ V_{in}

  comparator flips

  counter goes low

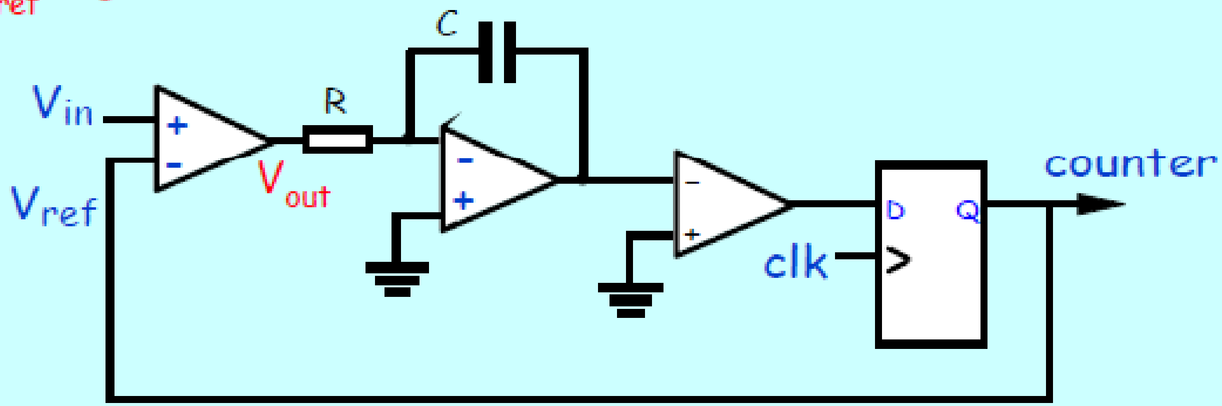
  clock increments... etc,...

  V_{in} = 0 => output = 000000...

  V_{in} = (1/2)V_{in}(max) => output = 101010...

  V_{in} = V_{in}(max) => output = 111111...

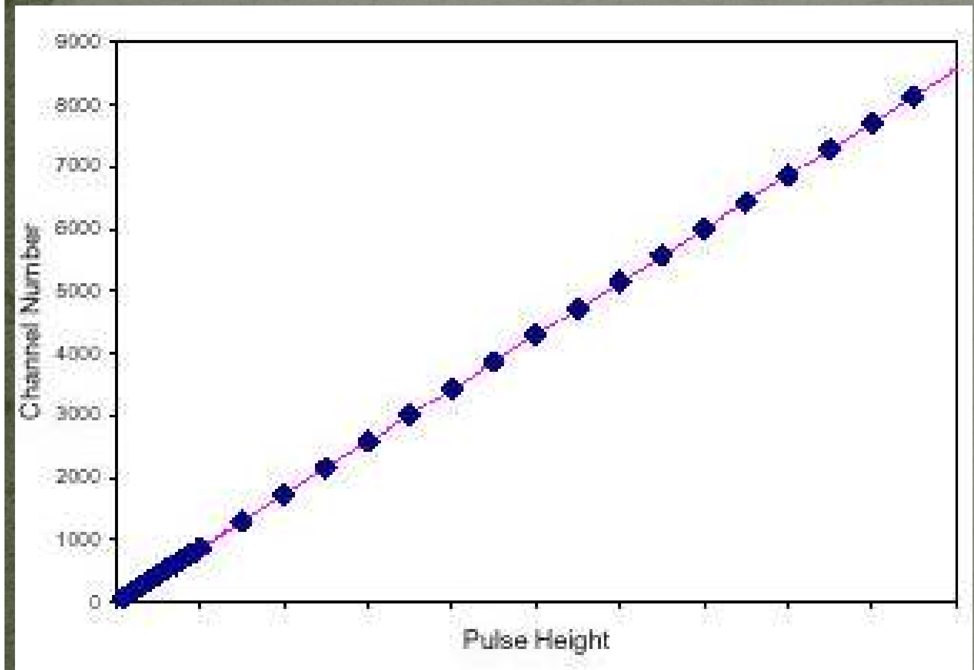
  the higher the input voltage, the more 1's at the serial digital output.

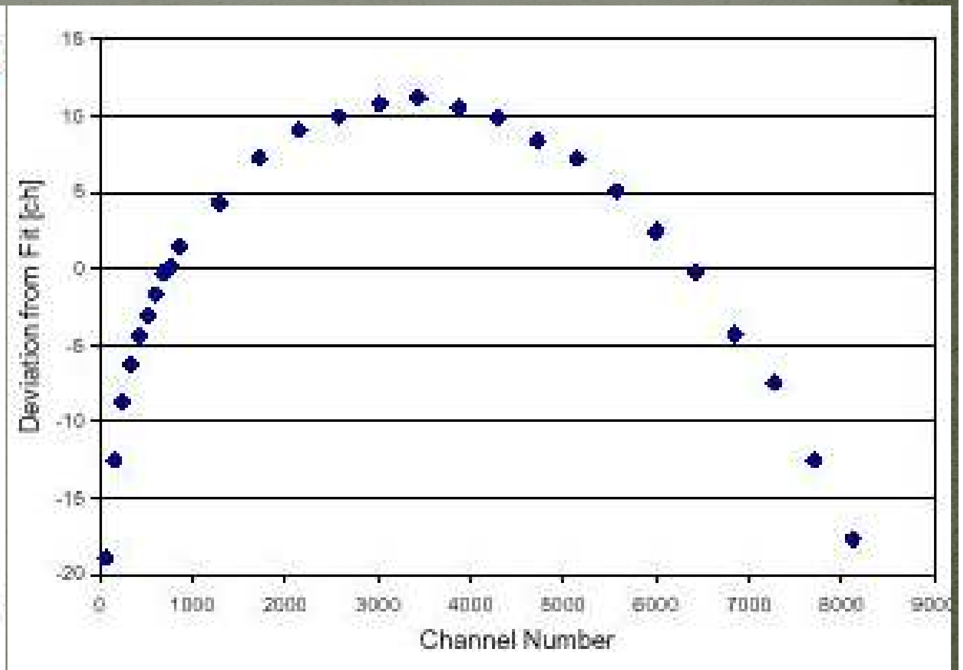


Integral non-linearity

- Output value D should be linearly proportional to V
- Check with plot

- For more precise evaluation of INL fit to line and plot deviations
- Plot D_i-D_{fit} vs nchan

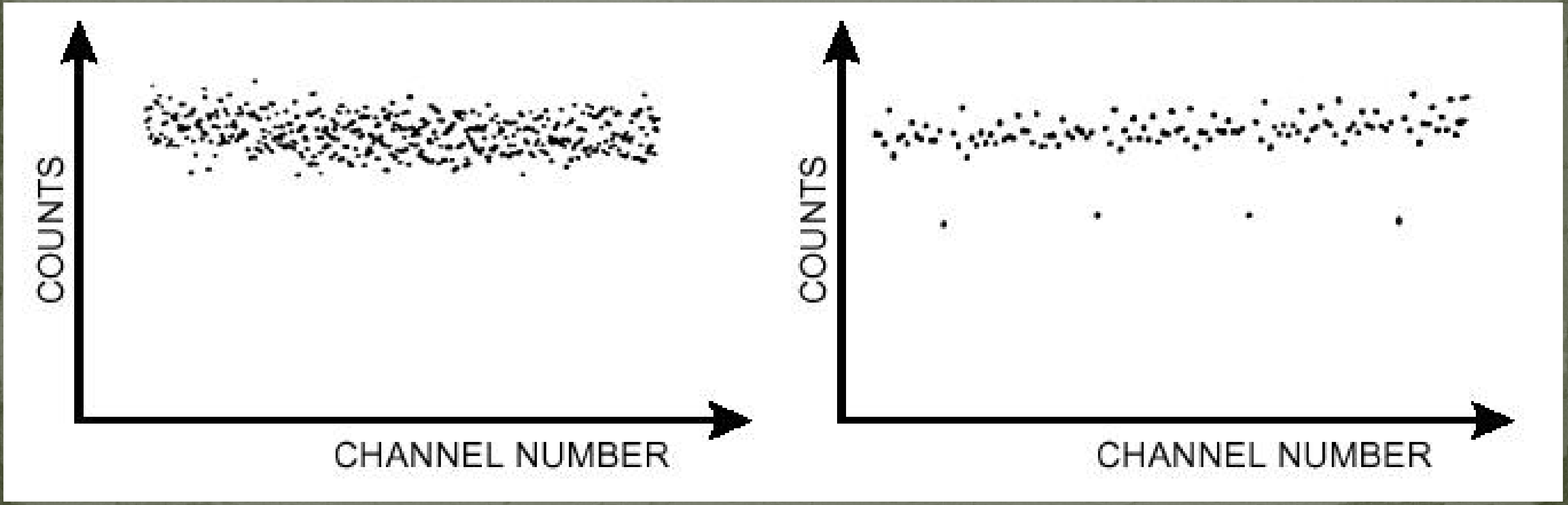




B.Satyanarayana, TIFR, Mumbai Signal Processing Electronics WSHEP, BHU, Varanasi

Differential non-linearity

- Measures non-uniformity in channel profiles over range
  - $DNL = DV_i / \langle DV \rangle - 1$
  - DV_i = width of channel i
  - $\langle DV \rangle$ = average width
- RMS or worst case values may be quoted
  - DNL ~ 1% is typical but 10^{-3} can be achieved
  - can show up systematic effects, as well as random



Resolution

- To convert an analogue value, eg voltage, to digital two parameters are required

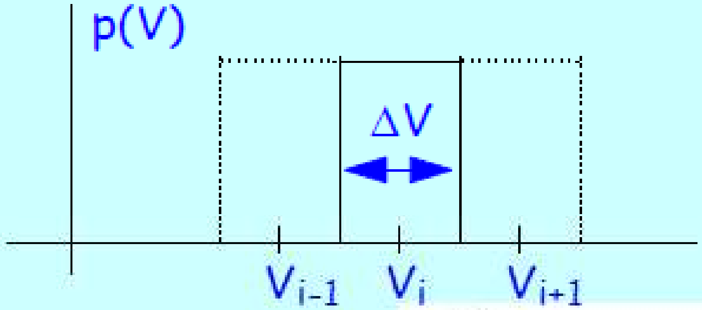
  range and number of bits

  quantum = $\Delta V = (V_{max} - V_{min}) * 2^{-N}$ referred to as 1LSB (least significant bit)

- eg 10 bits = 2^{10} = 1024, $V_{max} - V_{min}$ = 1V => ΔV = 1V/1024 ≈ 1mV

- Ideal ADC behaviour

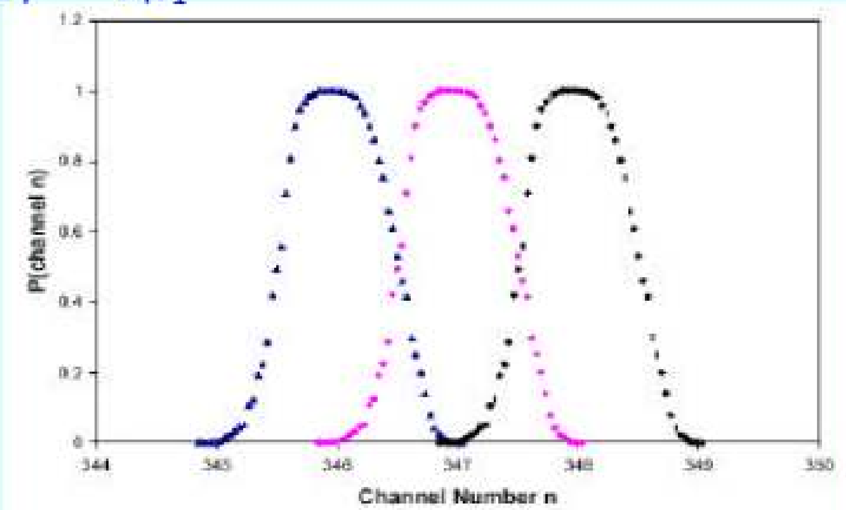
  probability vs amplitude



- Real ADC behaviour

  noise in digitisation process

  smears resolution



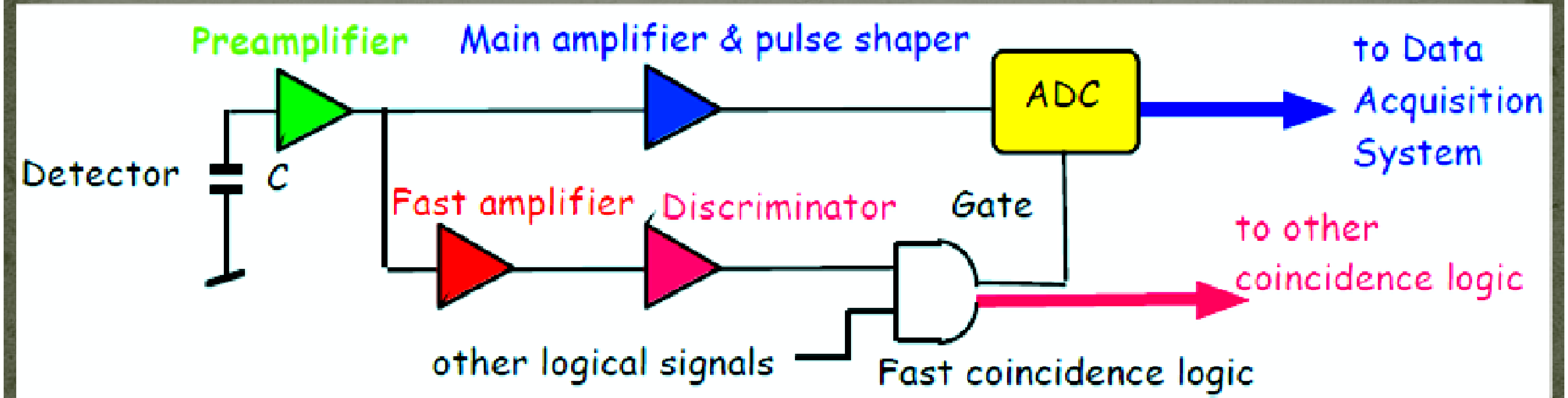
$\sigma_{noise} < \Delta V/4$

Other variables

- Conversion time
  - finite time is required for conversion and storage of values
  - may depend on signal amplitude
  - gives rise to dead time in system
  - i.e. system cannot handle another event during dead time
  - may need accounting for, or risk bias in results
- Rate effects
  - results may depend on rate of arrival of signals
  - typically lead to spectral broadening
- Stability
  - temperature effects are a typical cause of variations
- A partial solution to most of these problems is regular calibration, preferably under real operating conditions, as well as control of variables

Amplifier systems for spectroscopy

- Typical application - precise measurements of x-ray or gamma-ray energies



- Pre-amplifier - *first stage of amplification*
- Main amplifier - *adds gain and provides bandwidth limiting*
  - ADC - analog to digital conversion - *signal amplitude to binary number*
- Fast amplifier and logic
  - Start ADC ("gate") and flag interesting "events" to DAQ system
  - Most signals arrive randomly in time.
  - Other logic required to maximise chance of "good" event, ex. second detector

MCA Vs MCS

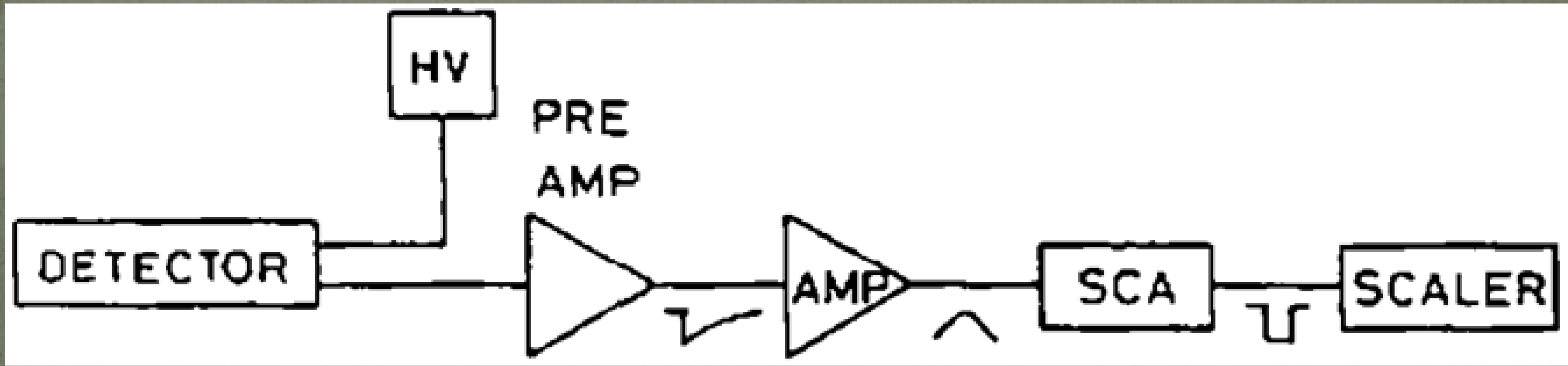
Multi Channel Analyser (MCA)

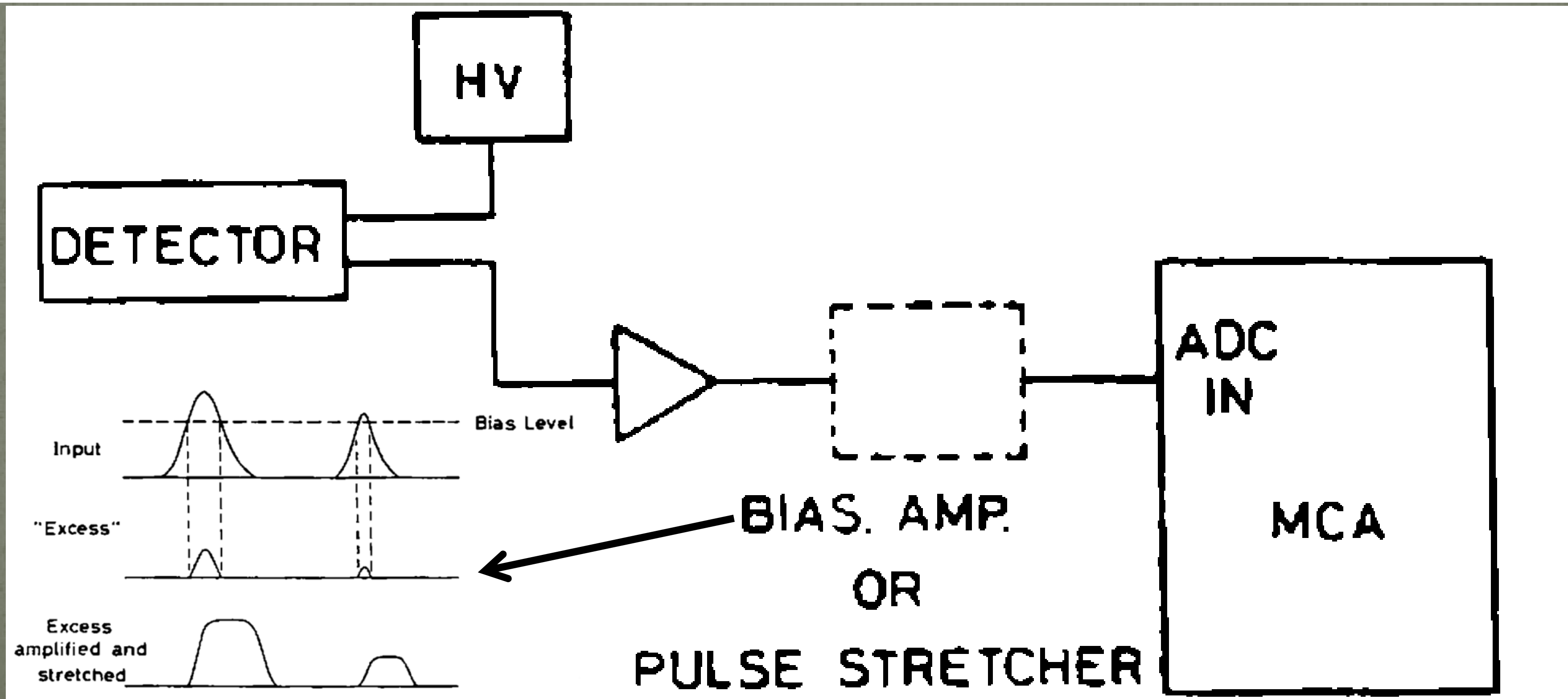
- Uses ADC
- Sorts incoming pulses according to their pulse heights
- Channel represent pulse height
- Total channels → Conversion gain
- Application: Spectroscopy

Multi Channel Scaler (MCS)

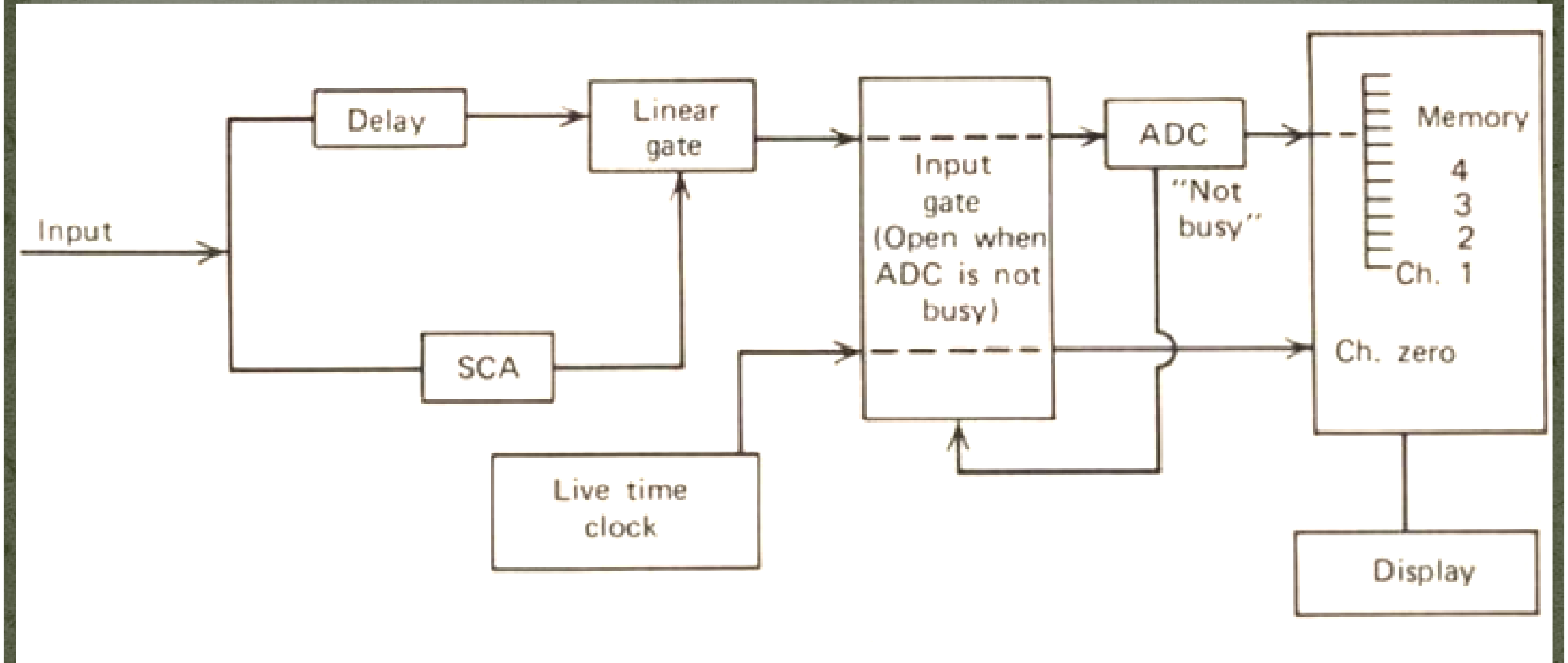
- Uses comparator and counter
- Counts incident pulse signals (regardless of amplitude) for a certain *dwell time*
- Channels represent bins in time
- Application: Decay curves of radioactive isotopes

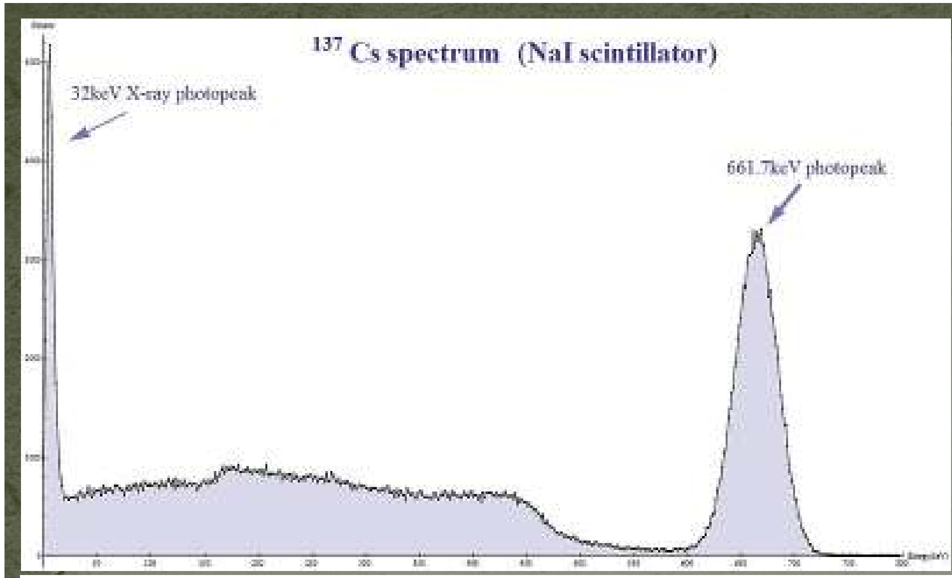
SCA and MCA schemes





Functional block diagram of a MCA





Two gamma rays with energies of 1.17 and 1.33 MeV

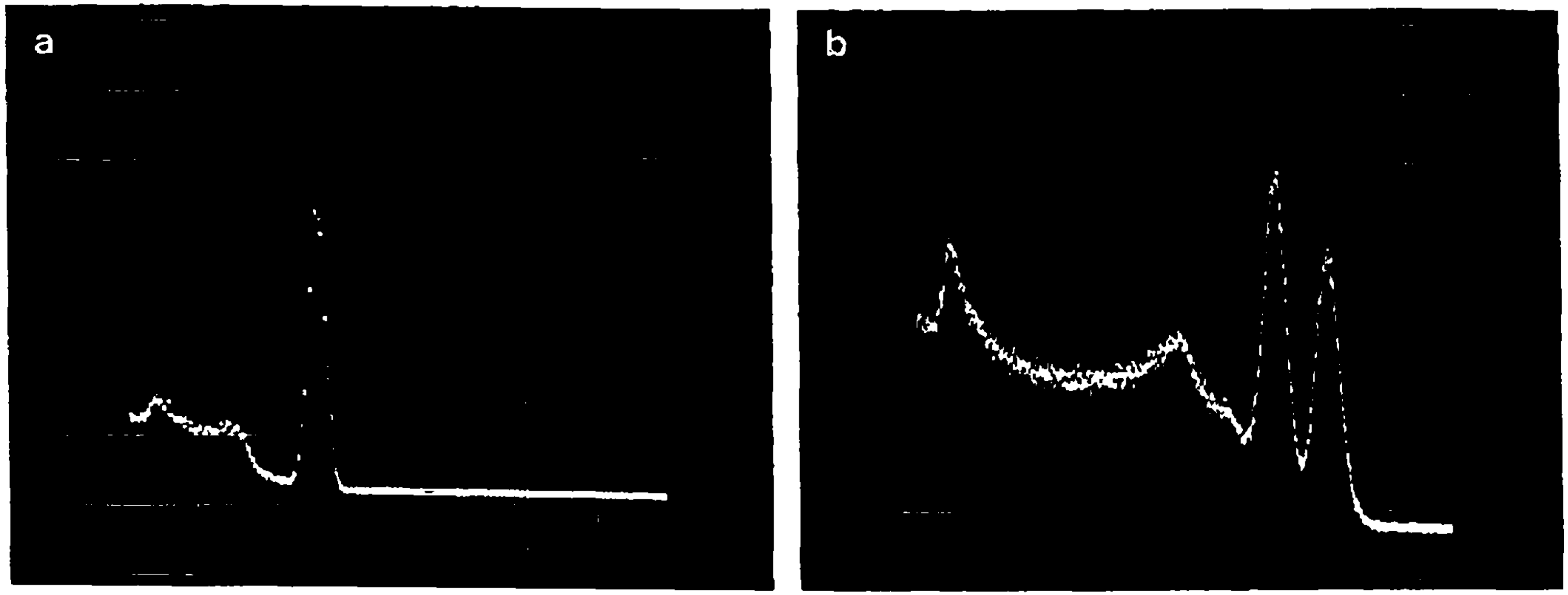
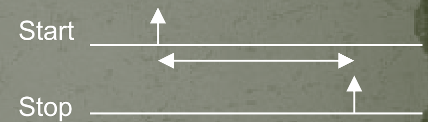


Fig. 15.6. Sample MCA pulse height spectra from a NaI detector: (a) ^{137}Cs, (b) ^{60}Co

Why TDCs?

TDCs are used to measure time or intervals

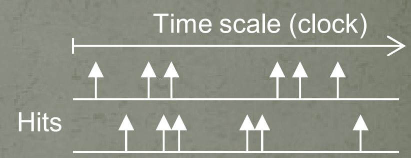
❖ Start – Stop measurement



- Measurement of time interval between two events:
  - Start signal – Stop signal
- Used to measure relatively short time intervals with high precision
- Like a stop watch used to measure sport competitions

❖ Time tagging

- Measure time of occurrence of events with a given time reference:
  - Time reference (Clock)
  - Events to be measured (Hits)



- Used to measure relative occurrence of many events on a defined time scale:
  - Such a time scale will have limited range; like 12/24 hour
  - time scale on your watch when having no date and year

Where TDCs?

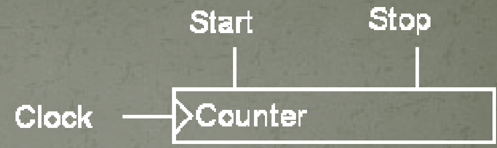
- Special needs for High Energy Physics
  - Many thousands of channels needed
  - Rate of measurements can be very high
  - Very high timing resolution
  - A mechanism to store measurements during a given interval and extract only those related to an interesting event, signaled by a trigger, must be integrated with TDC function
- Other applications
  - Laser/radar ranging to measure distance between cars
  - Time delay reflection to measure location of broken fiber
  - Most other applications only needs one or a few channels

How to compare TDCs?

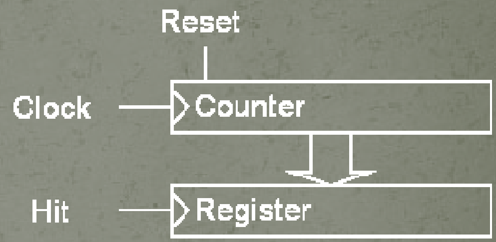
- Merits
  - Resolution
    - Bin size and effective resolution (RMS, INL, DNL)
  - Dynamic range
  - Stability
    - Use of external reference
    - Drift (e.g. temperature)
    - Jitter and Noise
  - Integration issues
    - Digital / analog
    - Noise / power supply sensitivity
    - Sensitivity to matching of active elements
    - Required IC area
    - Common timing block per channel
    - Time critical block must be implemented on chip together with noisy digital logic
- Use in final system
  - Can one actually use effectively very high time resolution in large systems (detectors)
  - Calibration - stability
  - Distribution of timing reference (start signal or reference clock)
  - Other features: data buffering, triggering, readout, test, radiation, etc.

Basic TDC types - I

- Counter type
  - Advantages
    - Simple; but still useful!
    - Digital
    - large dynamic range possible
    - Easy to integrate many channels per chip
  - Disadvantages
    - Limited time resolution (1ns using modern CMOS technology)
    - Meta stability (use of Gray code counter)
- Single Delay chain type
  - Cable delay chain (distributed L-C)
    - Very good resolution (5ps mm)
    - Not easy to integrate on integrated circuits
  - Simple delay chain using active *gates*
    - Good resolution (~100ps using modern tech)
    - Limited dynamic range (long delay chain and register)
    - Only start-stop type
    - Large delay variations between chips and with temperature and supply voltage

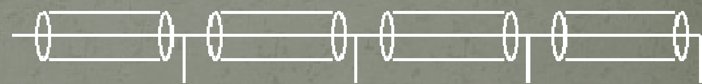


Start-stop type

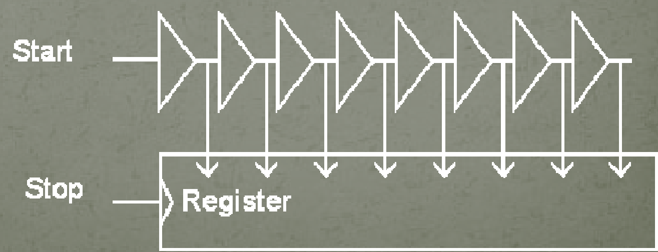


Time tagging type

Cable delay chain



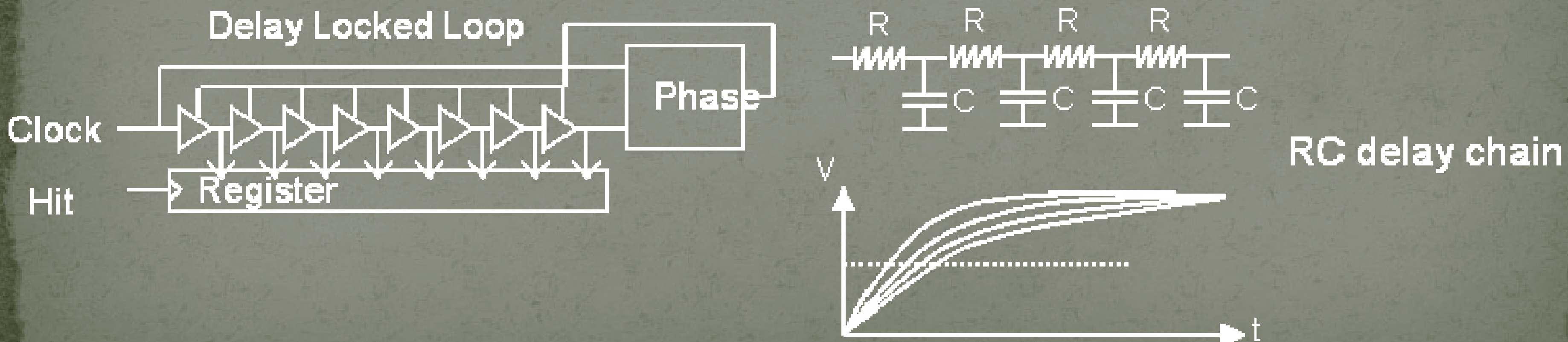
Delay chain with non-inverting gates



Basic TDC types - II

❖Single Delay chain type (Contd …)

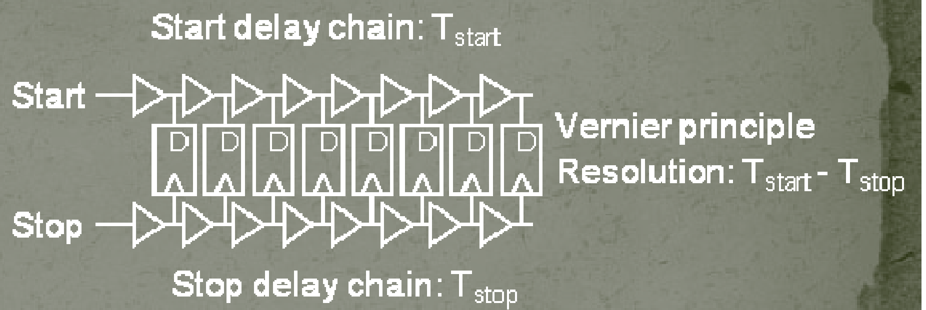
- Delay locked loop
  - Self calibrating using external frequency reference (clock)
  - Allows combination with counter
  - Delicate feedback loop design (jitter)
- R-C delay chain
  - Very good resolution
  - Signal slew rate deteriorates
  - Delay chain with losses; so only short delay chain possible
  - Large sensitivity to process parameters (and temperature)

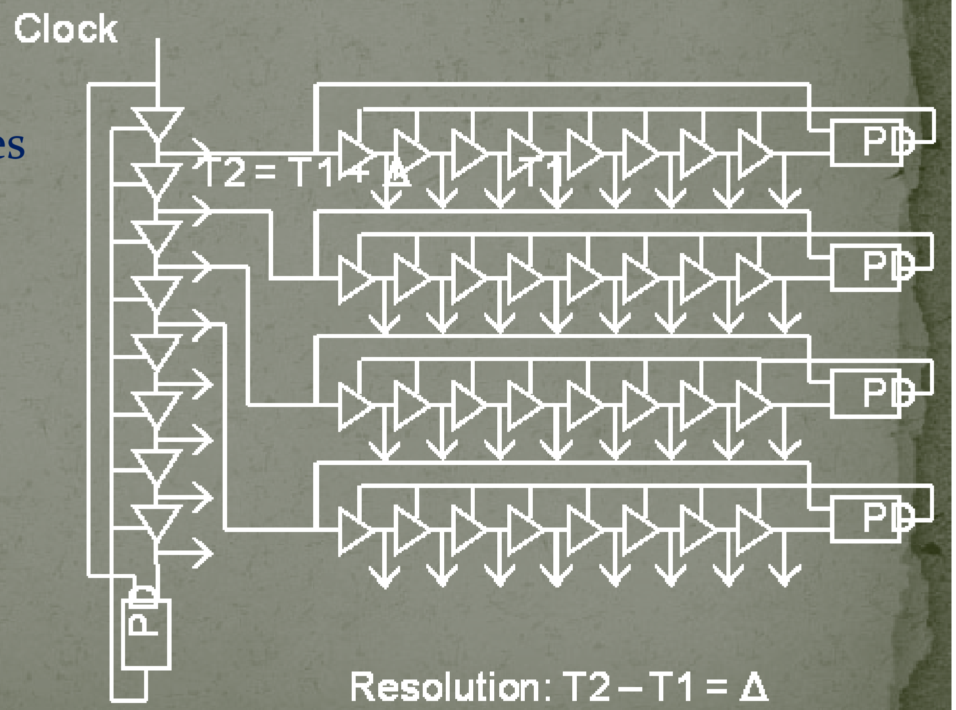


Basic TDC types - III

❖ Multiple delay chain type

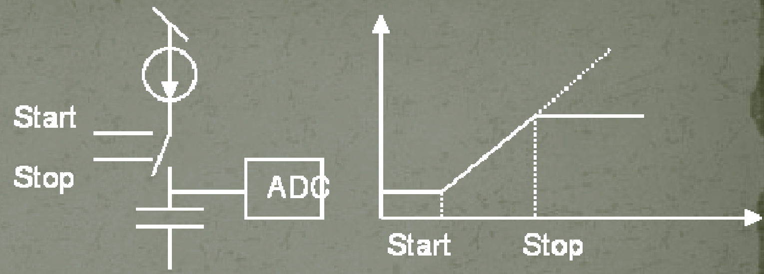
- Vernier delay chain types
  - Resolution determined by delay difference between two chains. Delay difference can be made very small and very high resolution can be obtained.
  - Small dynamic range (long chains)
  - Delay chains can not be directly calibrated using DLL
  - Matching between delay cells becomes critical
- Coupled delay locked loops
  - Sub-delay cell resolution (¼)
  - All DLLs use common time reference (clock)
  - Common timing generator for multiple channels
  - Jitter analysis not trivial

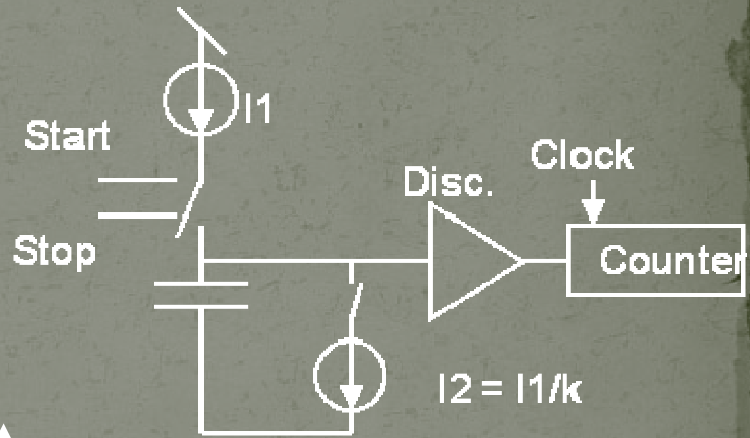


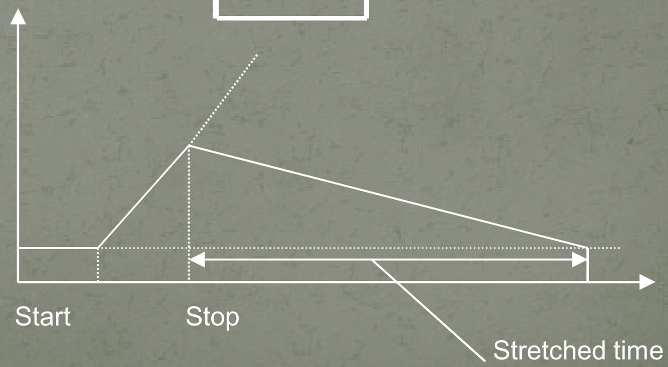


Basic TDC types - IV

- ❖ Charge integration
  - Using ADC (TAC)
    - High resolution
    - Low dynamic range
    - Sensitive analog design
    - Low hit rate
    - Requires ADC
  - Using double slope (time stretcher)
    - No need for ADC (substituted with a counter)
- ❖ Multiple *exotic* architectures
  - Heavily coupled phase locked loops
  - Beating between two PLLs
  - Re-circulating delay loops
  - Summing of signals with different slew rates

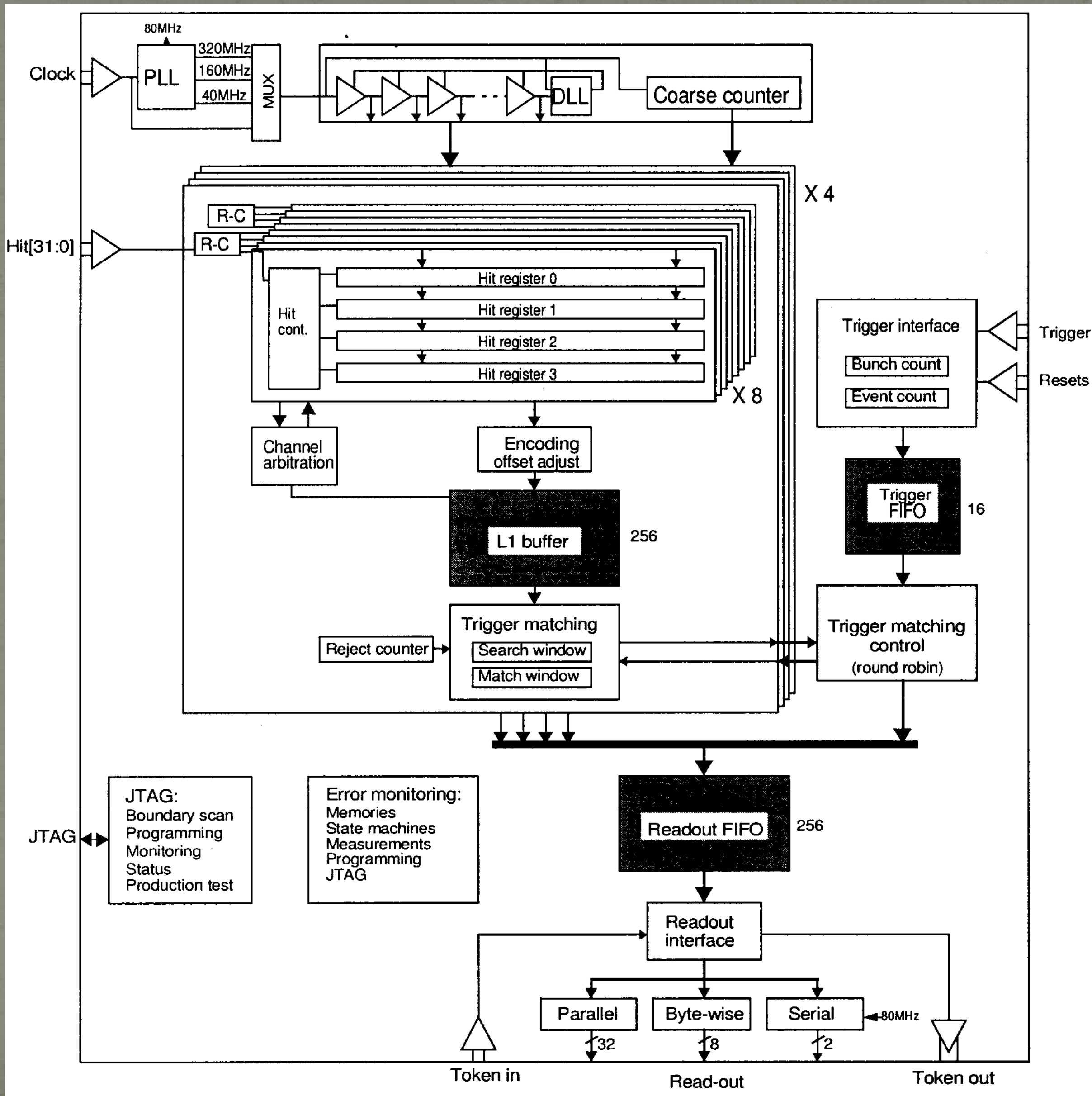






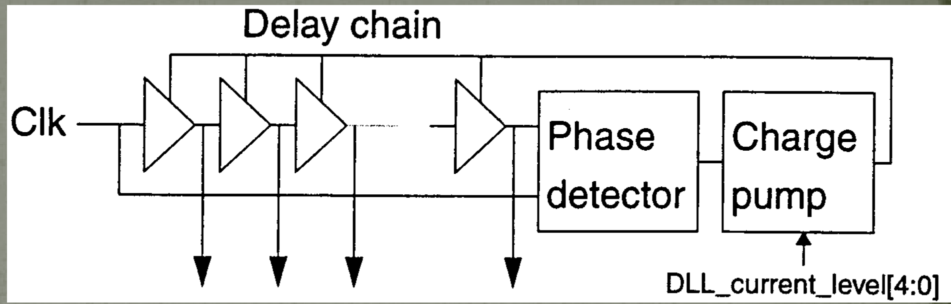
Architecture of HPTDC (ALICE TOF)

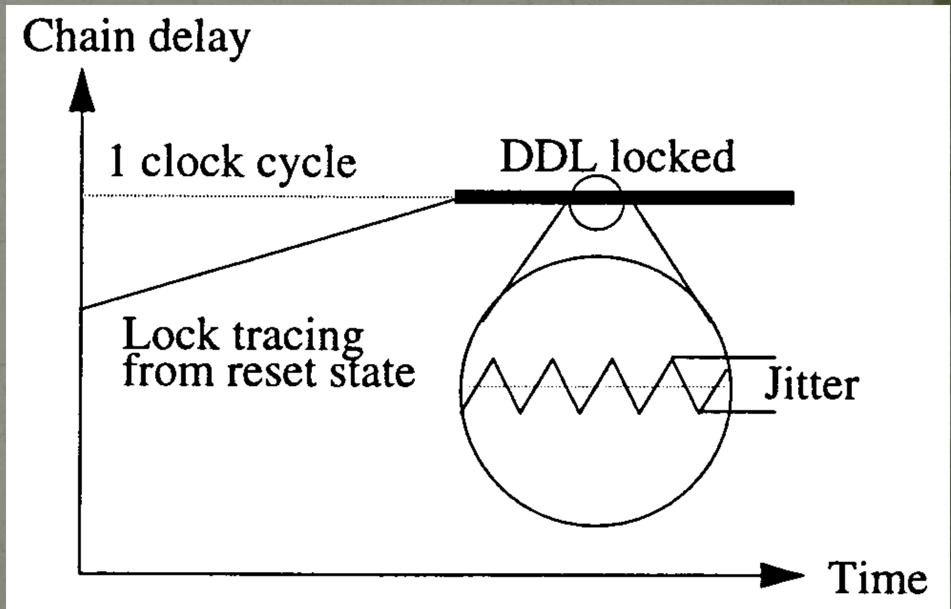
Application Specific Integrated Circuit



Delay Locked Loop (DLL)

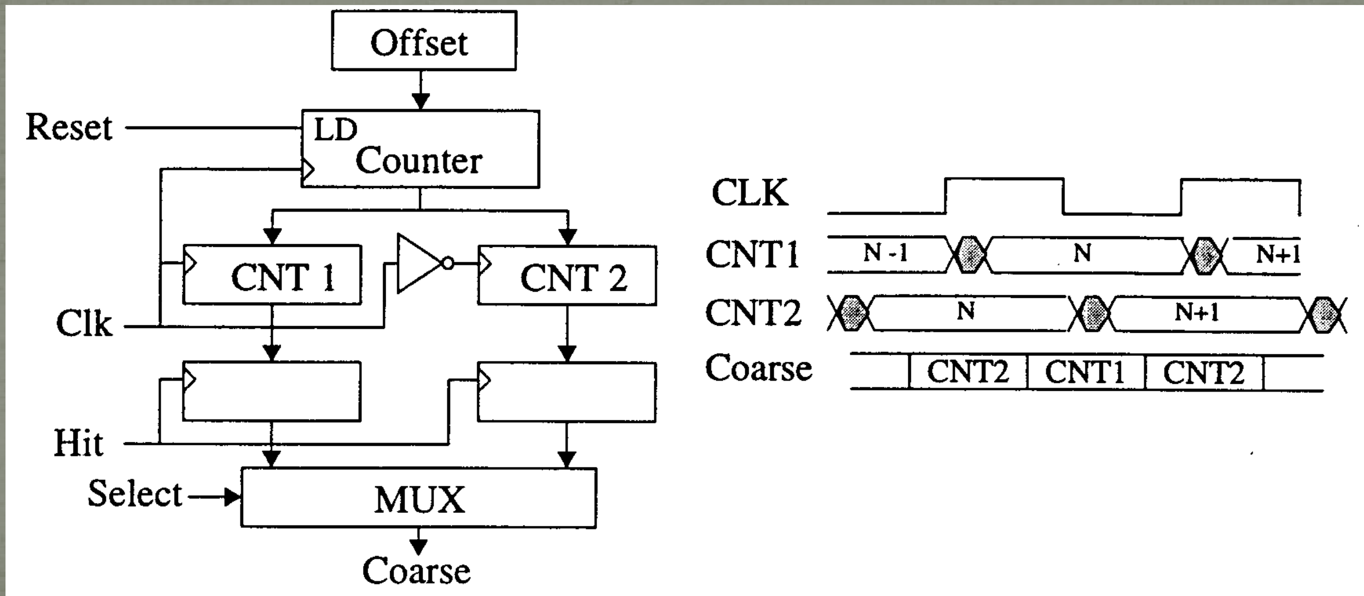
- Three major components:
  - Chain of 32 delay elements; adjustable delay
  - Phase detector between clock and delayed signal
  - Charge pump & level shifter generating control voltage to the delay elements
- Jitter in the delay chain
- Lock monitoring
- Dynamics of the control loop
- Programmable charge pump current level

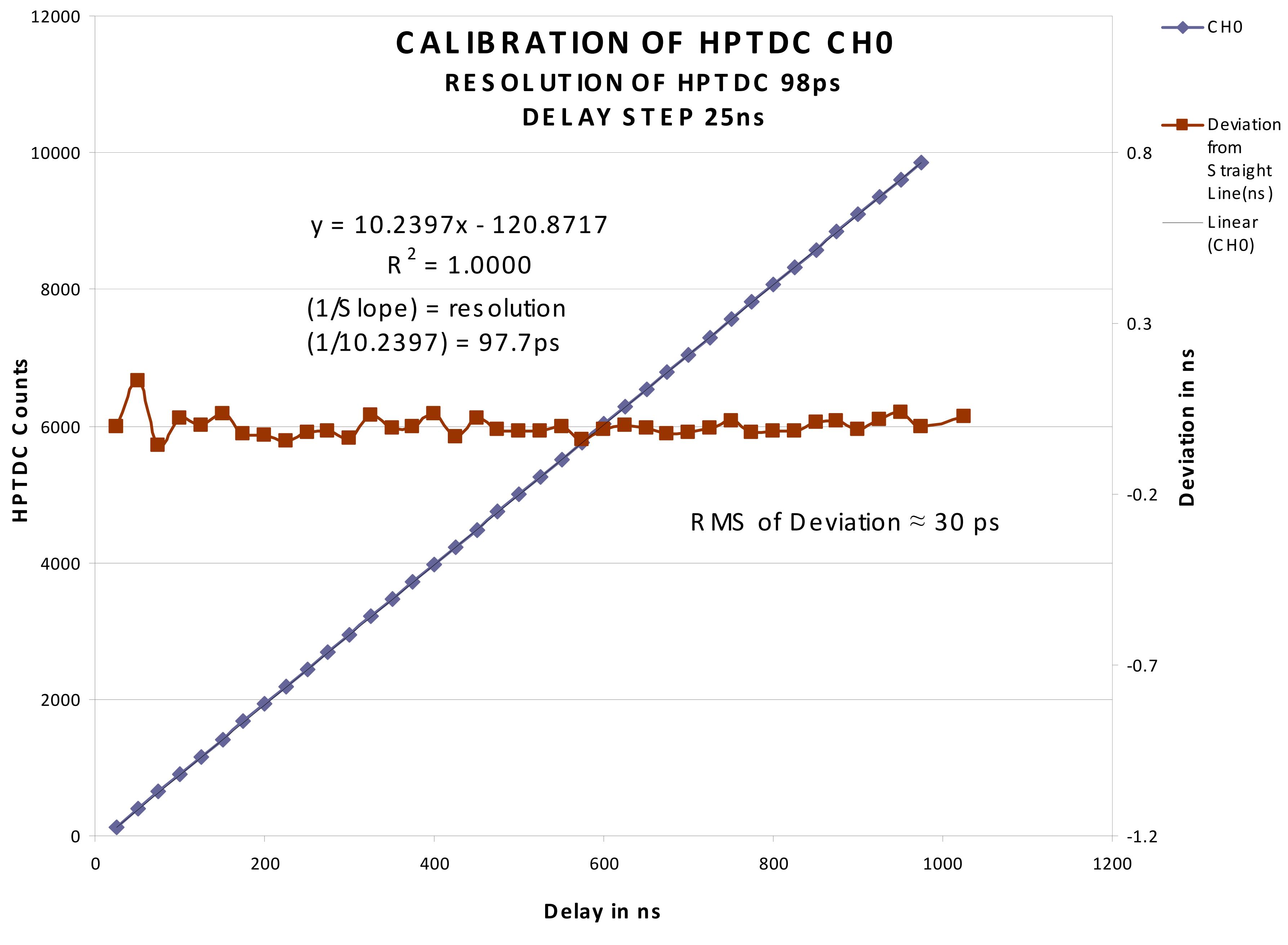




Coarse time count

- Dynamic range of the fine time measurement, extracted from the state of DLL is expanded, by
- Storing the state of a clock synchronous counter
- Hit signal is synchronous to the clocking, so
- Two count values, ½ a clock cycle out of phase stored
- At reset, coarse time counter loaded with time offset

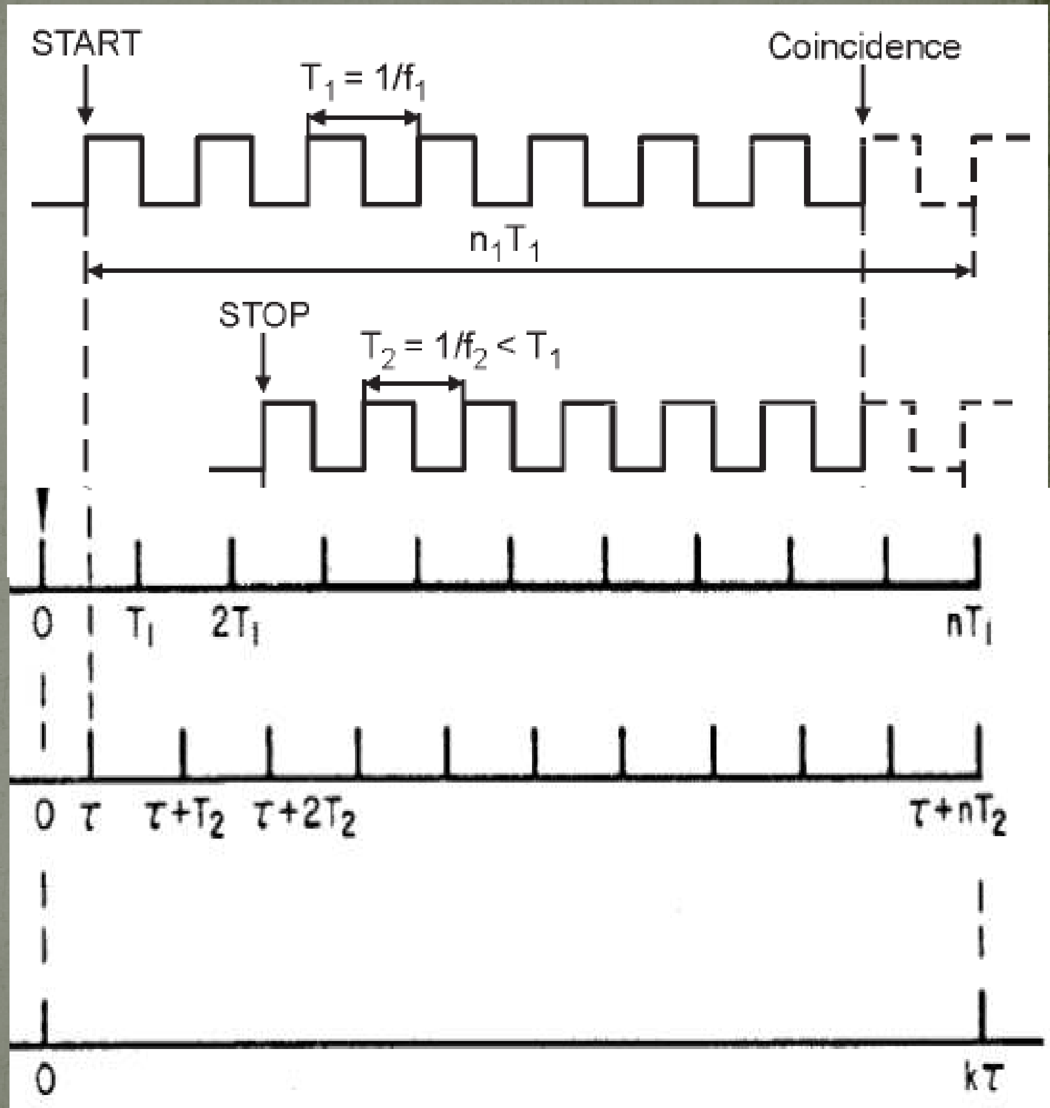



CALIBRATION OF HPTDC CH0
RESOLUTION OF HPTDC 98ps
DELAY STEP 25ns
y = 10.2397x - 120.8717
R 2 = 1.0000
(1/Slope) = resolution
(1/10.2397) = 97.7ps
RMS of Deviation ≈ 30 ps
HPTDC Counts
Deviation in ns
Delay in ns
CH0
Deviation from Straight Line(ns)
Linear (CH0)
12000
10000
8000
6000
4000
2000
0
200
400
600
800
1000
1200
0.8
0.3
-0.2
-0.7
-1.2

Concept of a vernier TDC

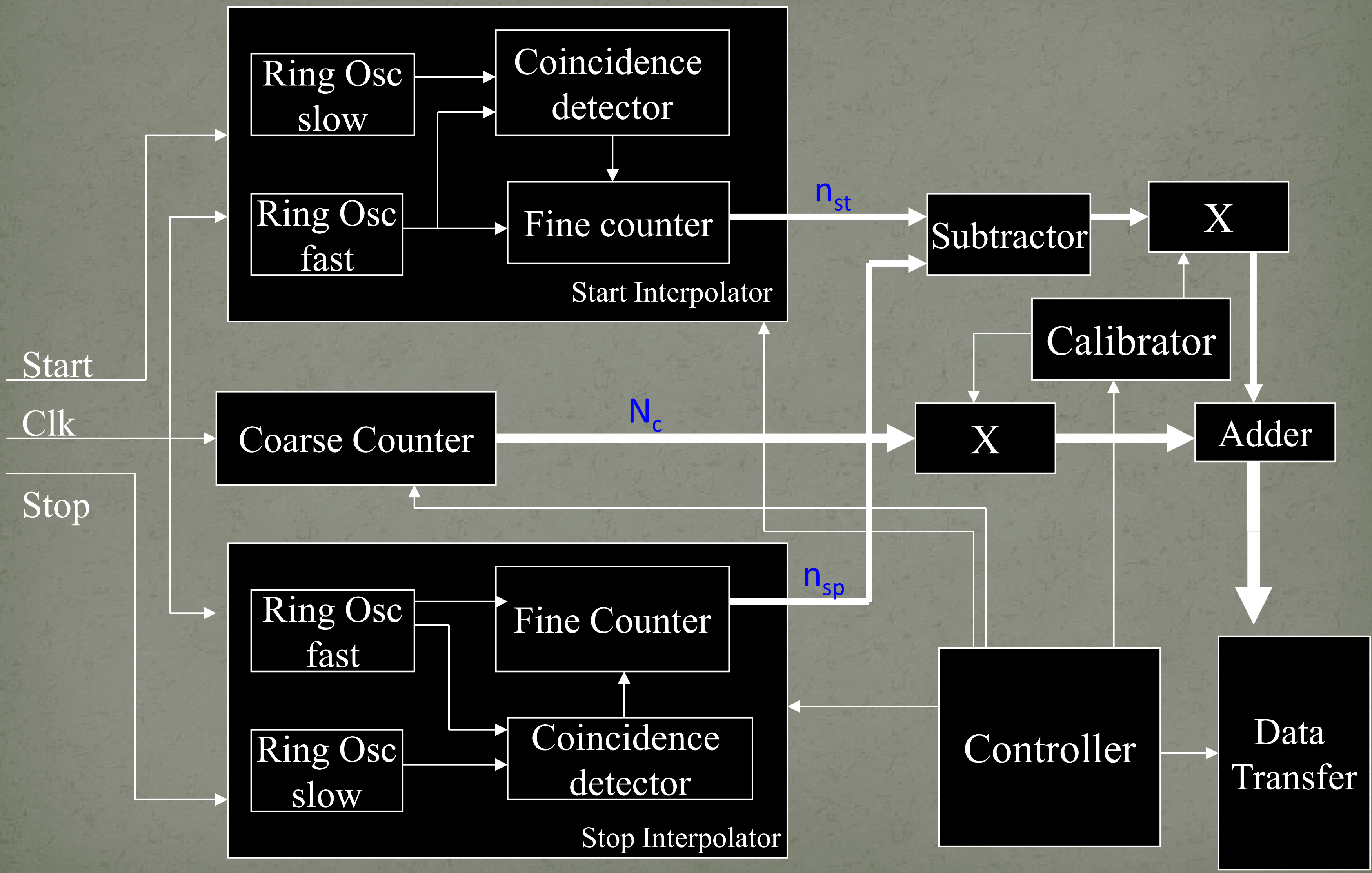
- Two clocks of slightly different periods T_1 and T_2 ($T_1 > T_2$) are employed.
- START pulse will start the slow oscillator (T_1) and STOP pulse will start the fast oscillator (T_2).
- Since $T_2 < T_1$, fast oscillator will catch up with the slow one.
- The time interval between the START and STOP can be measured as:

  $\tau = (N_1 - 1)\, T_1 - (N_2 - 1)\, T_2$
- Two counters for N_1 and N_2 are needed.



B.Satyanarayana, TIFR, Mumbai Signal Processing Electronics WSHEP, BHU, Varanasi

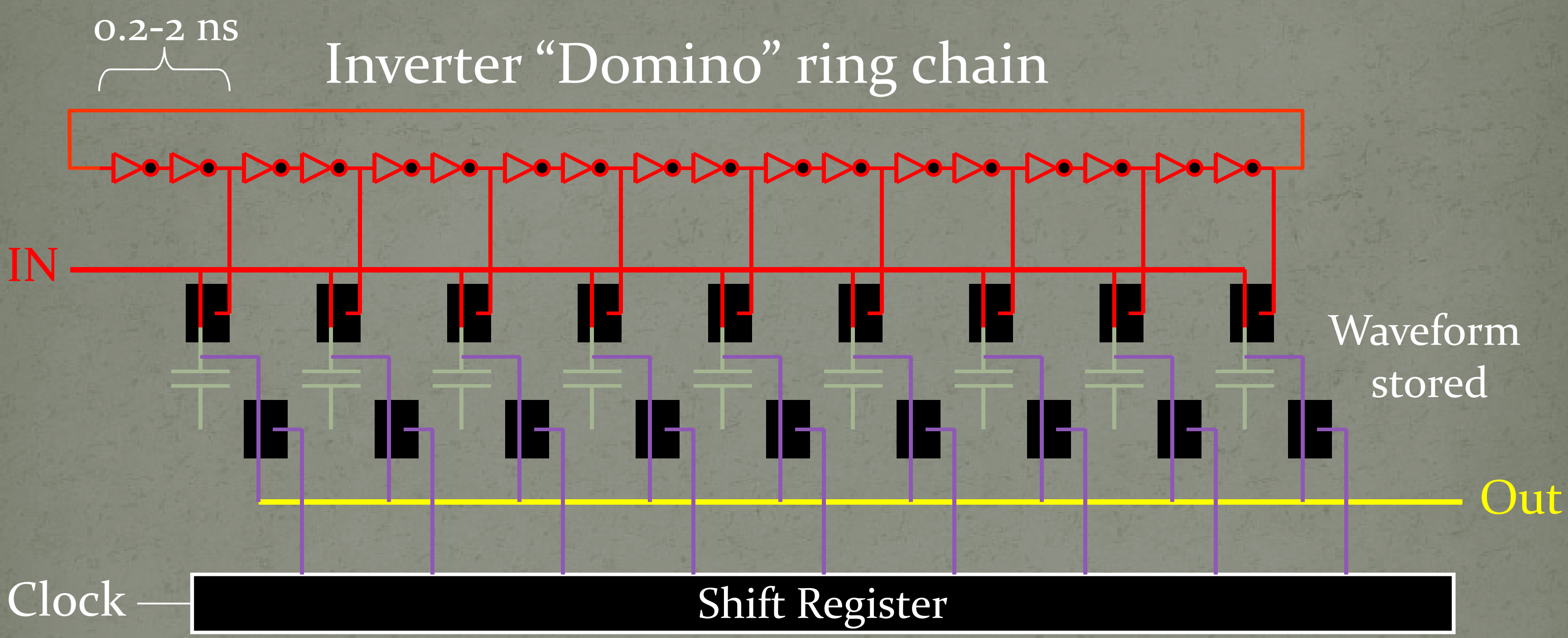
Schematic of a vernier TDC



Digital waveform samplers

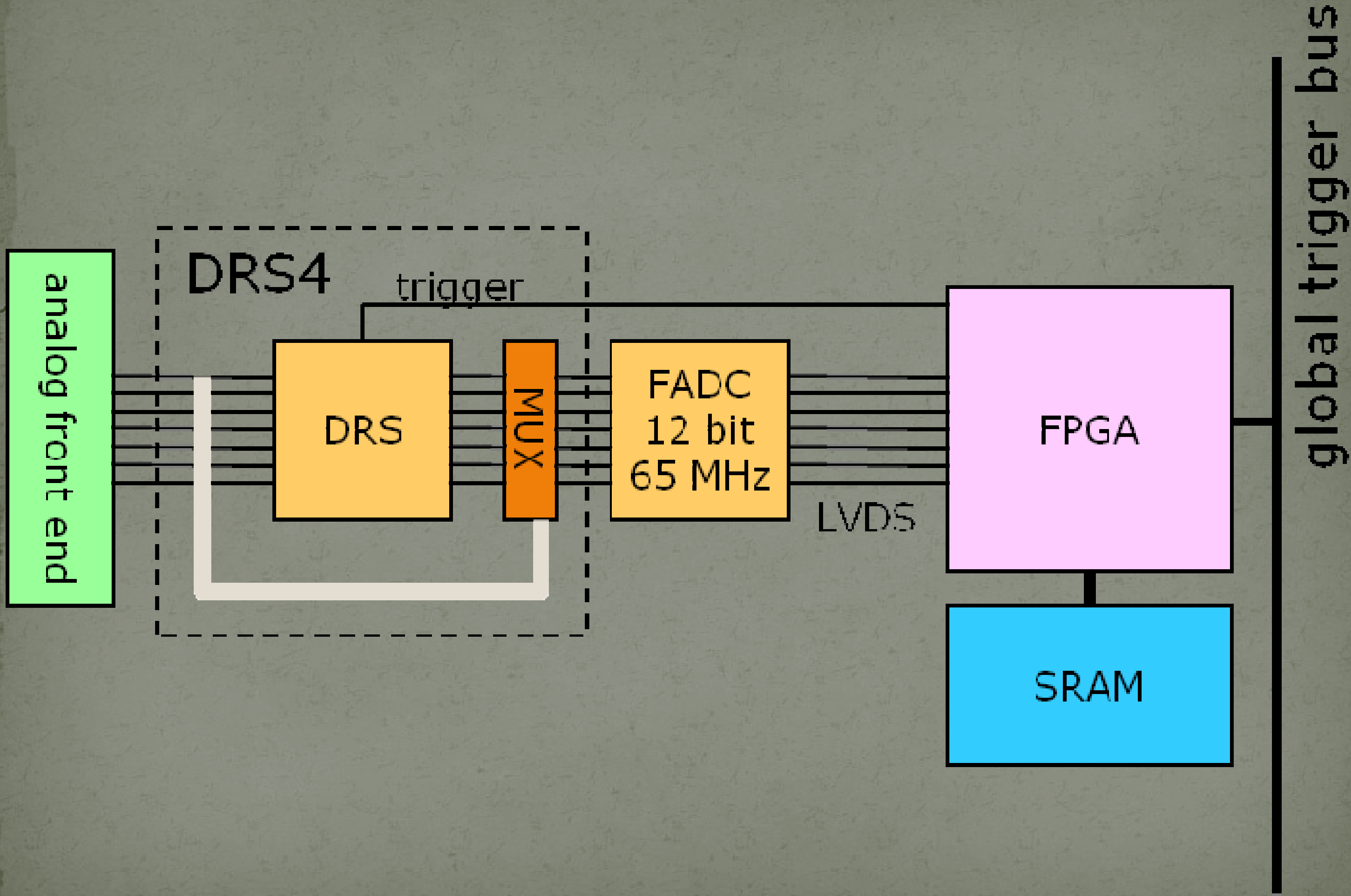
- ❖ Versatile element, which can perform simultaneously functions of several DAQ building blocks discussed so far:
  - Peak sensing Analog to Digital Conversion
  - Charge to Digital Conversion
  - Time to Digital Conversion
  - Hit registering
  - Pulse width measurement
  - Pulse profile monitor
  - Pulse shape discrimination
  - Counting rate scaler
  - And so on …
- ❖ Made possible due to breakthroughs in VLSI technology and other techniques☺
- ❖ On flipside, it produces a large data size to be handled☹

Switched Capacitor Array (SCA)



“Time stretcher” GHz → MHz

Data acquisition through DRS chip



Lecture - IV

Wednesday, January 30, 2013

- ✓ Digital circuits and systems
- ✓ CPLDs, FPGAs and ASICs
- ✓ Instrumentation and interface standards
- ✓ Data acquisition systems

Digital electronics

- Explosive growth over 10-20 years - now dominates applications, still growing...

  computing

  communications: mobile/fixed phones, radio, data links,...

  other: digital audio, consumer goods,...

- Why?

  binary logic

  almost complete noise immunity

  high speed, still increasing

  Ethernet: ~Gb/s, phones, links: >Gb/s, computing ~GHz

  ease of use

  many analogue functions now easier to implement by digital summation, etc

  availability

  basic logic to complete IC assemblies of big range of complex functions

- Bits, Bytes & Words

  byte = 8 bits word: usually multiple of bytes 8, 16, 32, 64 bits

Basic logic

- bits can be represented in several ways, almost invariably voltage

  0/1: Low/High (voltage level) … or High/Low

  values and range depend on families, most common are...

- TTL (bipolar) Transistor-Transistor Logic

  usually V_S = 0 to +5V

  $V_T \sim 1.5V$ $\Delta V \sim 1V$

  outputs & inputs sink/source currents

  not identical levels

- CMOS - now most common

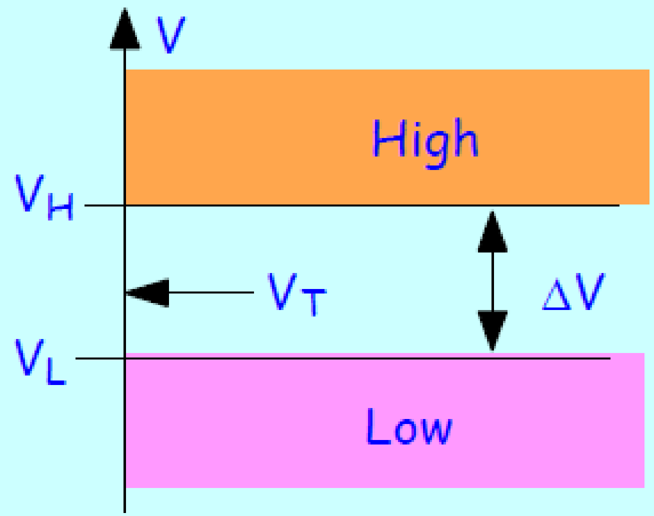
  V_S = 0 to +5V but +12V, +3.5V and lower

  $V_T \sim V_S/2$ $\Delta V \sim 0.4\ V_S$

  outputs swing between supplies

- ECL Emitter Coupled Logic

  high speed, but power hungry

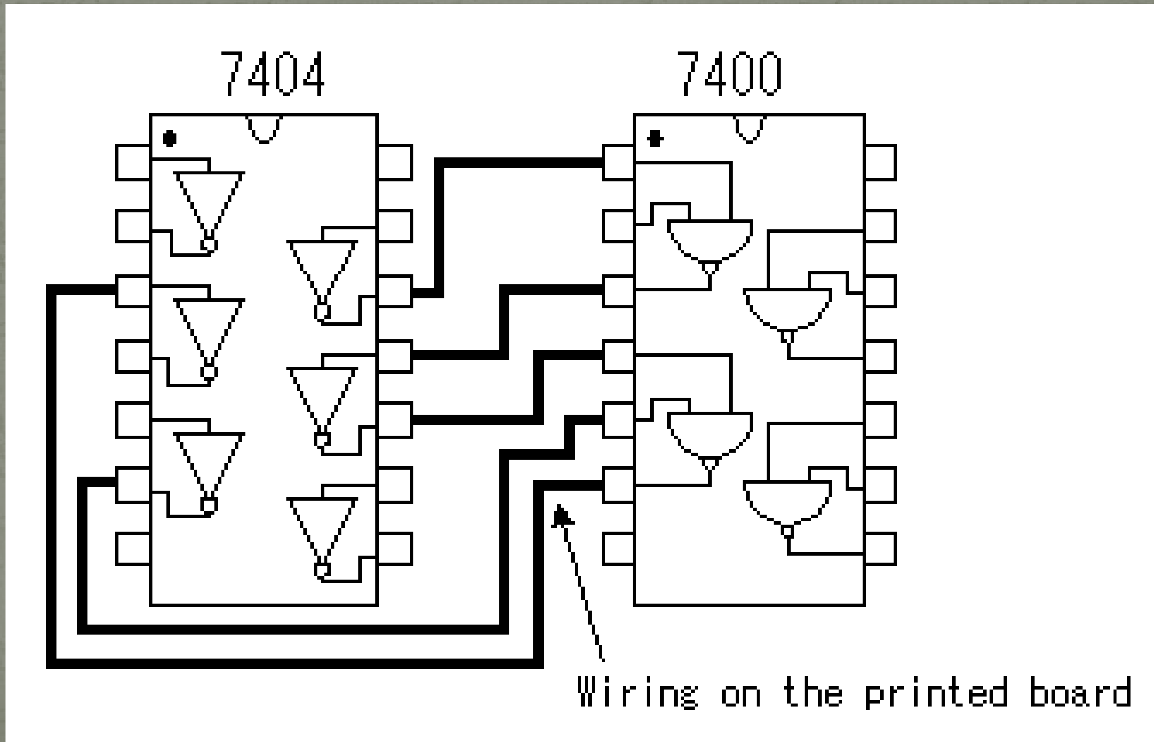


designs must tolerate variations

- component manufacture
- operating temperature
- supply voltage
- loading
- noise

Discrete digital circuits

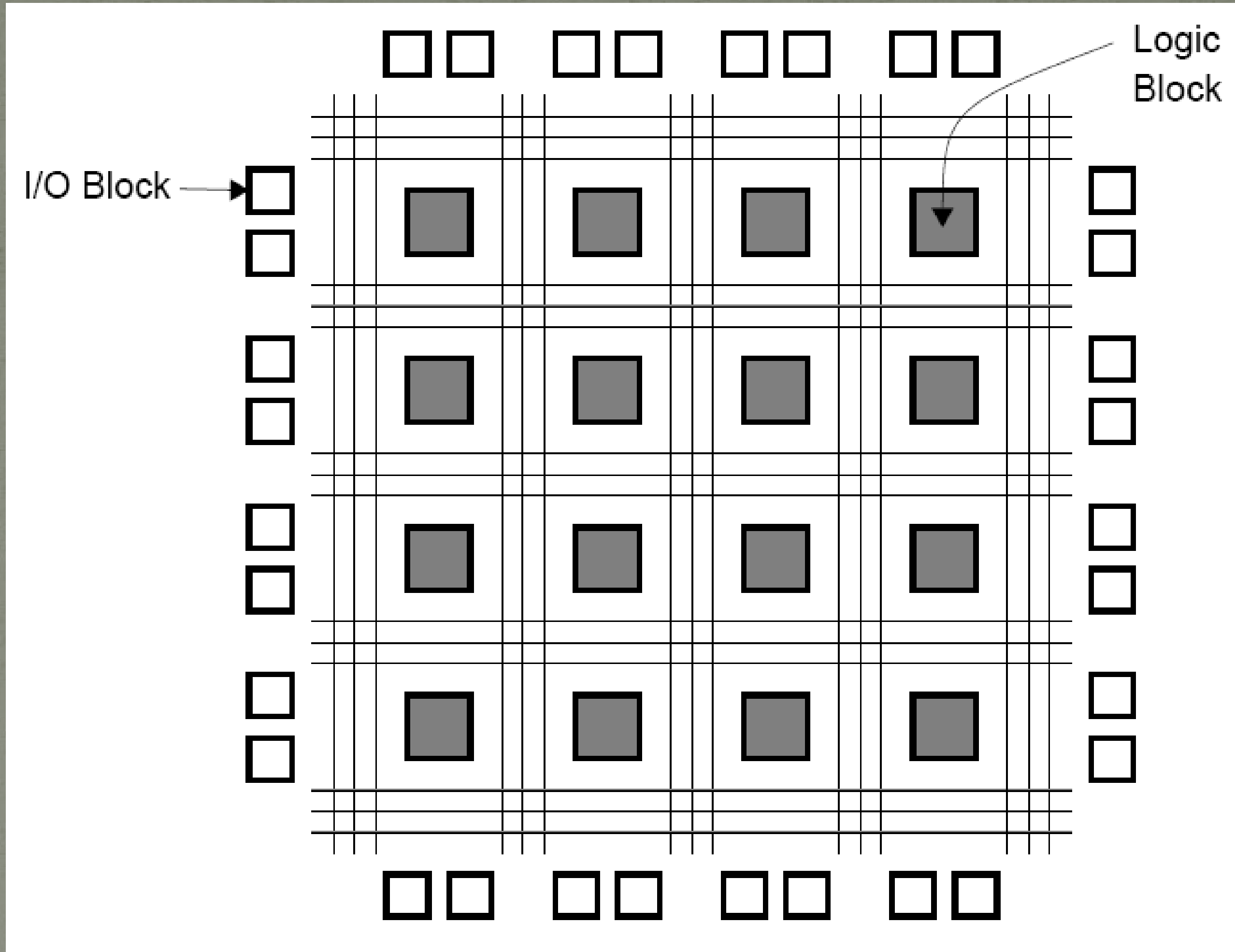
- For example, in case of the 7400 IC, 4 circuits of 2 input NAND gate are housed. In case of 7404, 6 circuits of inverter are housed. These are separate ICs. Therefore, to compose a circuit, it is necessary to do each wiring among the pins using the printed board.



Programmable logic

- For very complex logic, it's time consuming and risky to develop circuits
  - programmable logic solves both problems
- PLA programmable logic array
  - transistor array with connections set by fuses to burn
- FPGA field programmable gate array
  - MOS array of uncommitted gates - few k to several M
  - connections made by downloading code which sets biasing of circuits
  - fully re-programmable
- DSP digital signal processor
  - cut-down microprocessor with limited instruction set
- Various levels of complexity and skills to learn
  - eg 2M gate FPGA needs sophisticated design and simulation software

Structure of a PLD

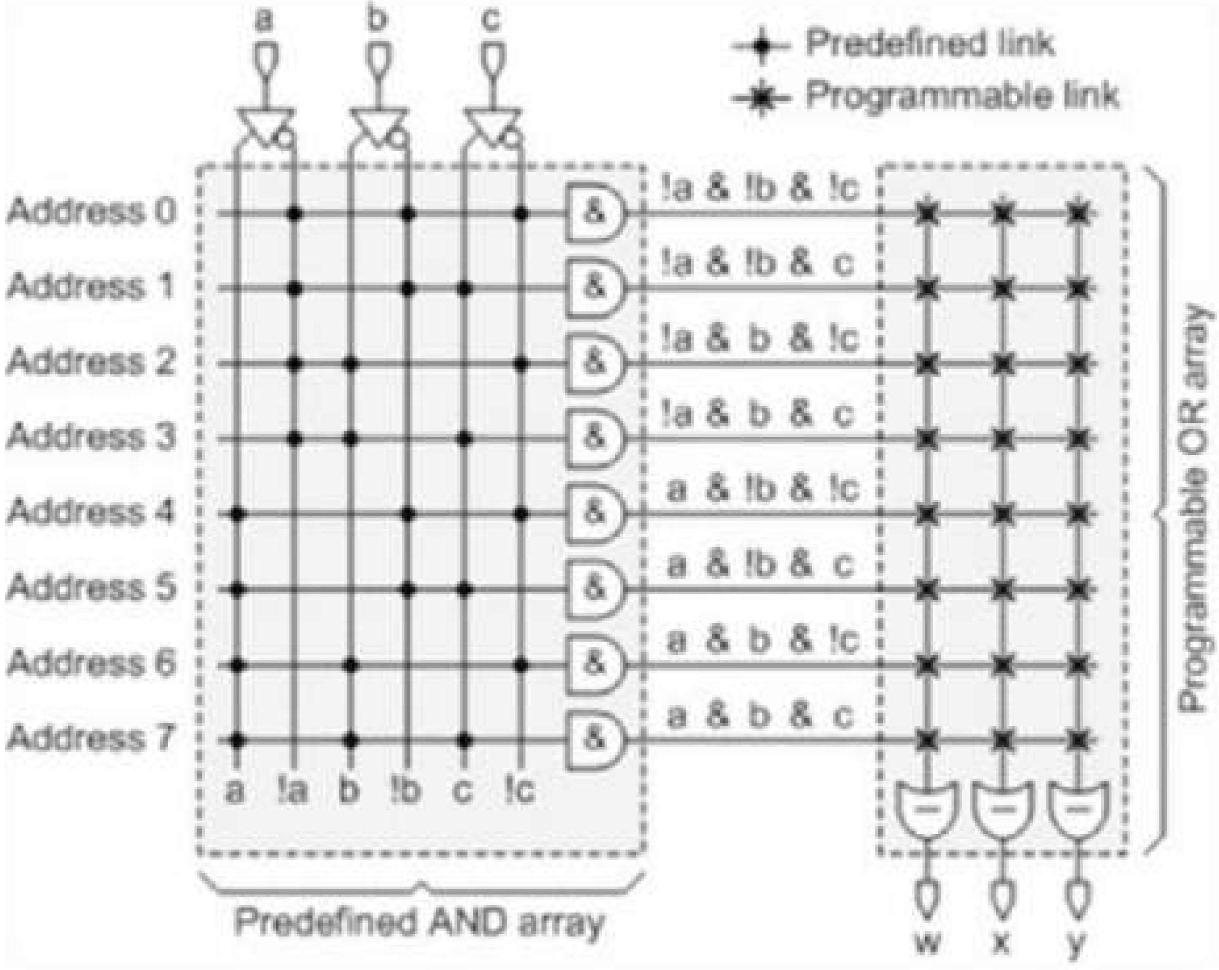


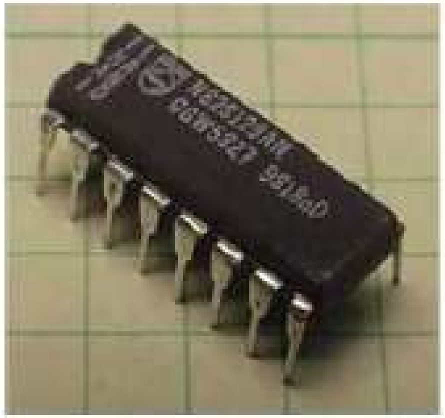
2D array of logic blocks with means for the user to configure:

- The function of each block
- Interconnection between the blocks

Simple PLDs

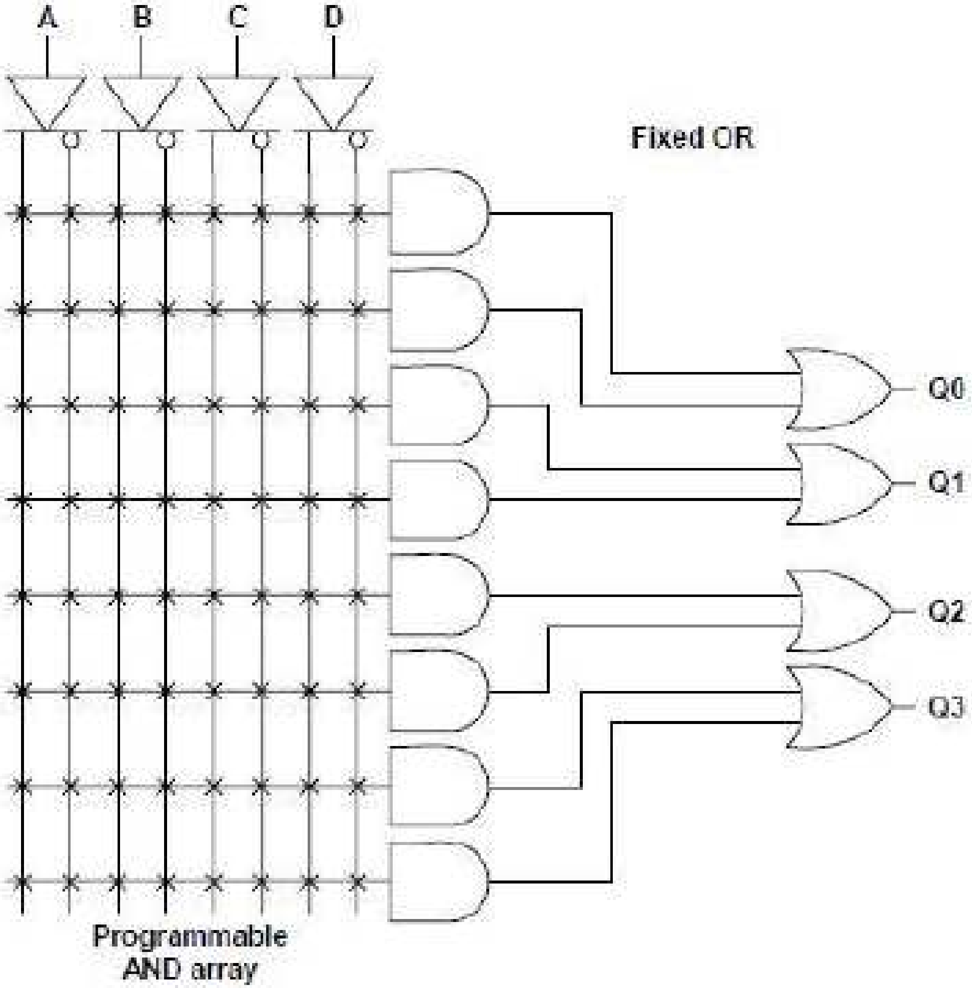
- Programmable Read Only Memory (PROM)





Simple PLDs

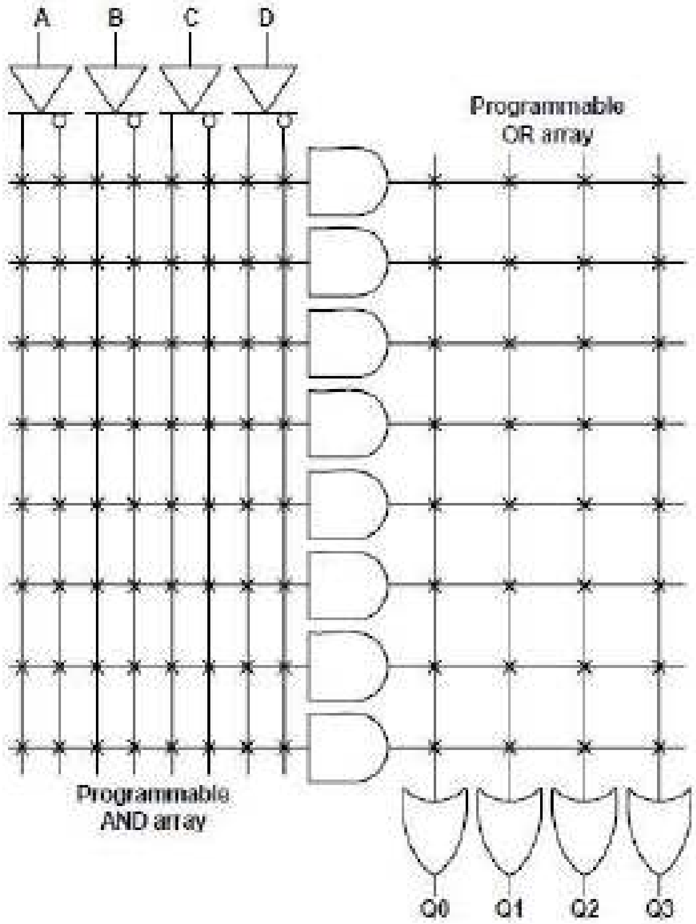
Programmable Array Logic (PAL)



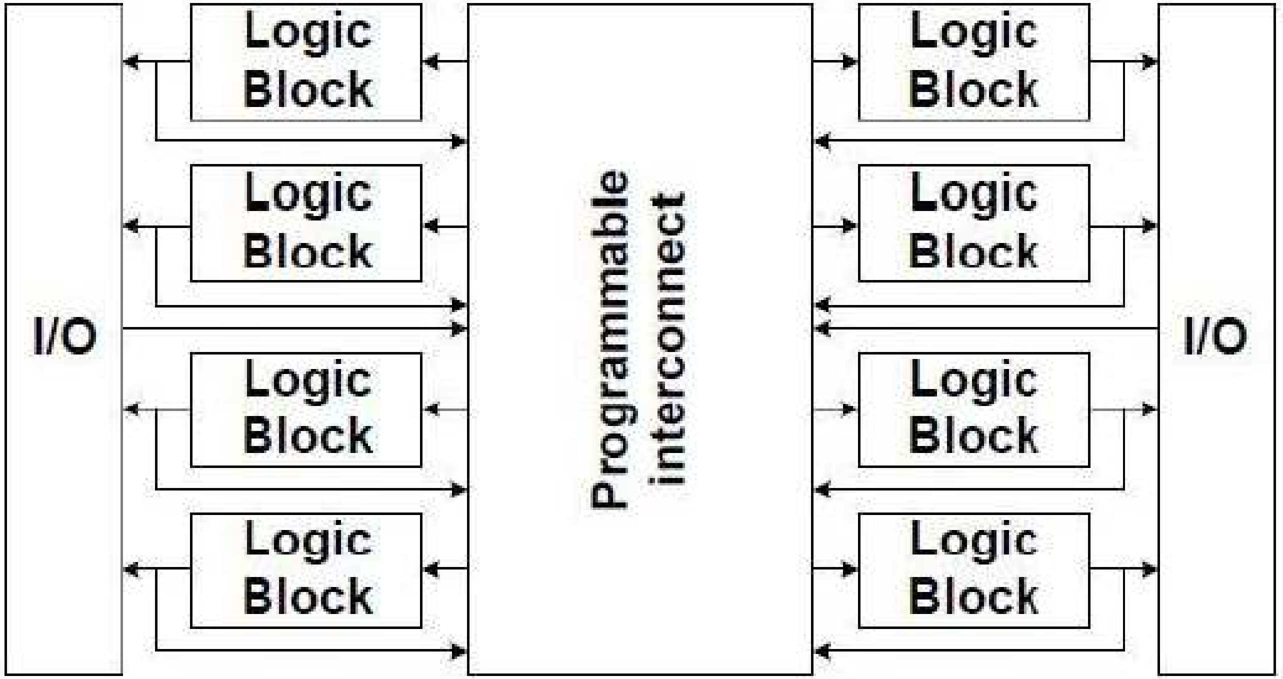
Simple PLDs

Programmable Logic Array (PLA)

- Offers most flexibility in programming
- Slower performance
- Expensive

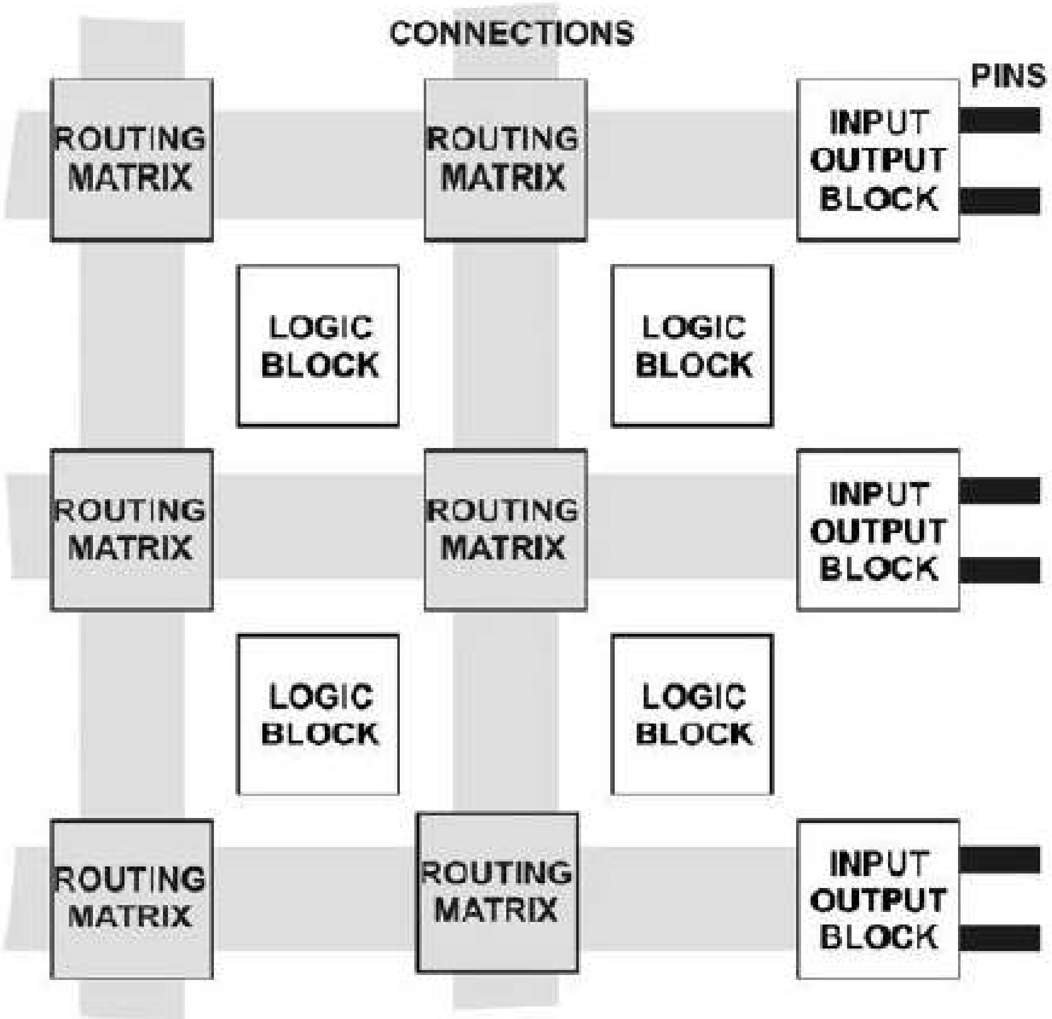


Complex PLDs (CPLDs)



- The capacity of CPLD is limited. There is limitation on the number of the pins, too.
- It is possible to rewrite CPLD many times because it is recording the contents of the circuit to the flash memory.
- In-situ programming of the chip possible.

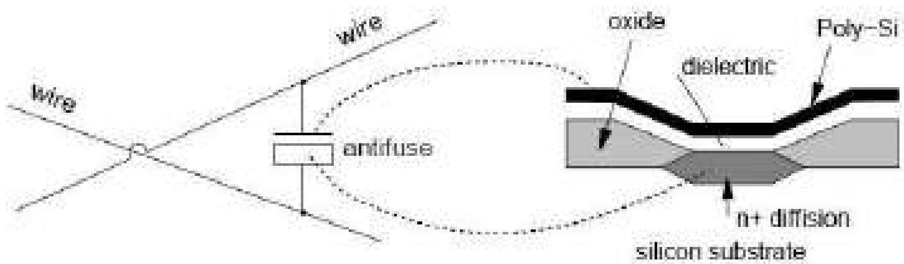
Field Programmable Gate Array (FPGA)

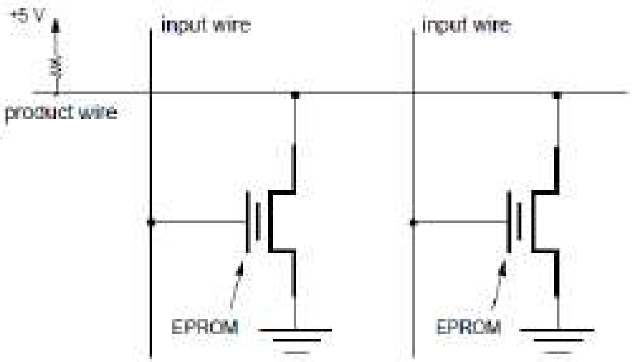


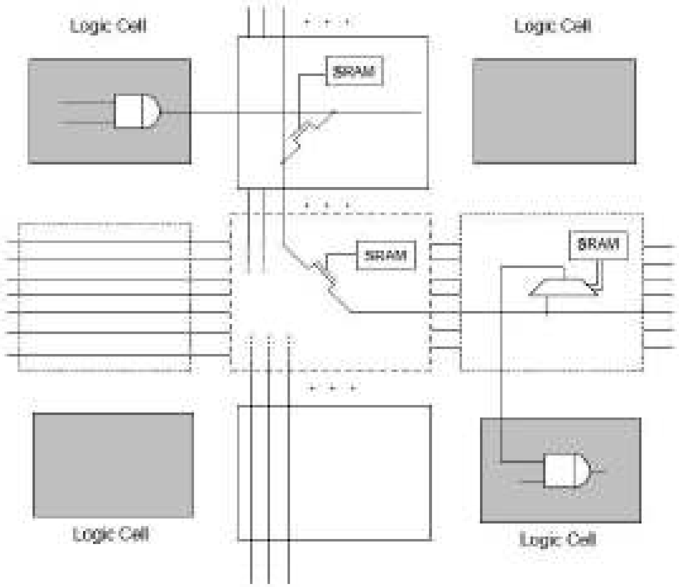
Logic function implemented as look-up table.

LUT may be alternatively configured as RAM or shift register.

Interconnect switches





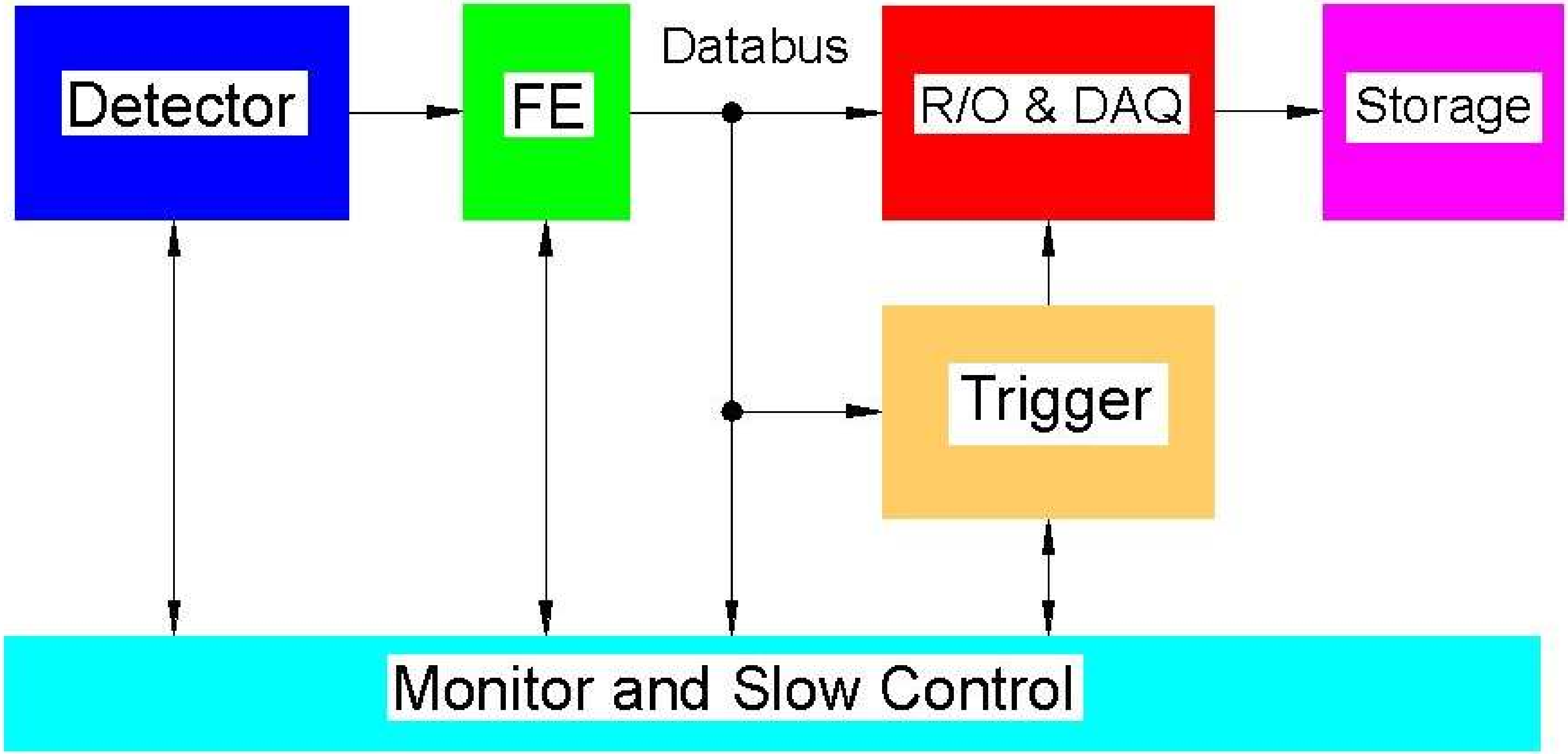


Technology	Volatile	Re-programmable	Area	Speed	Power	Extra fab steps
Antifuse	No	No	Small	Fast	Low	3
Flash	No	Yes	Small	Slow	Medium	>5
SRAM	Yes	Yes	Large	Fast	Medium	0

FPGA versus ASIC

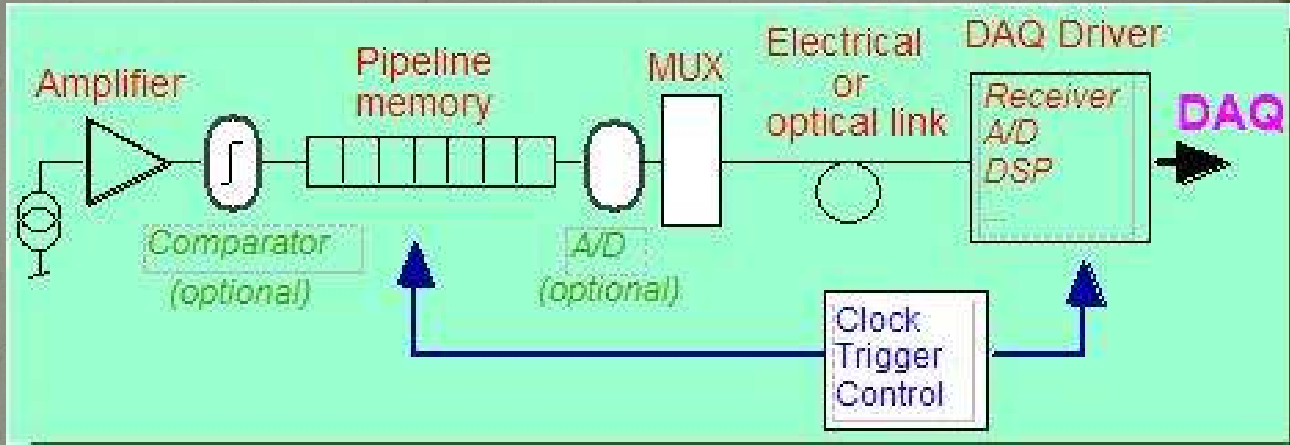
Parameter	FPGA	ASIC
Circuit Design	User programmable	Fully custom
Design Flexibility	Reconfigurable	Rigid
Logic Density	Lower	Higher
Complexity	Limited	High
Speed	Lower	Higher
Power Consumption	Higher	Lower
Area	Large	Small
Development Cycle	Simpler and faster	Complicated and time-consuming
Development Cost	Lower	Extremely high
Production Cost	Effective for small-scale applications	Cheaper for large-volume designs

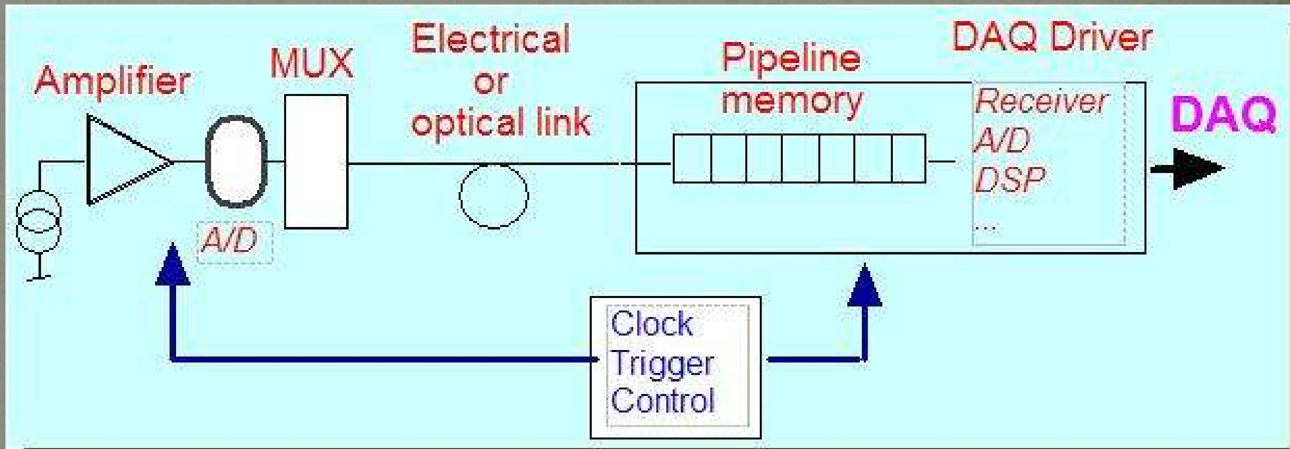
Concept of HEP instrumentation



Generic HEP detector readout systems

- Functions required by all systems
  - Amplification and filtering
  - Analog to digital conversion
  - Association to beam crossing
  - Storage prior to trigger
  - Dead time free readout
  - Pre-DAQ storage
  - Calibration
  - Control
  - Monitoring
- Calorimeter and muon detector functions
  - First level trigger primitive generation
- Optional
  - Location of digitisation & memory





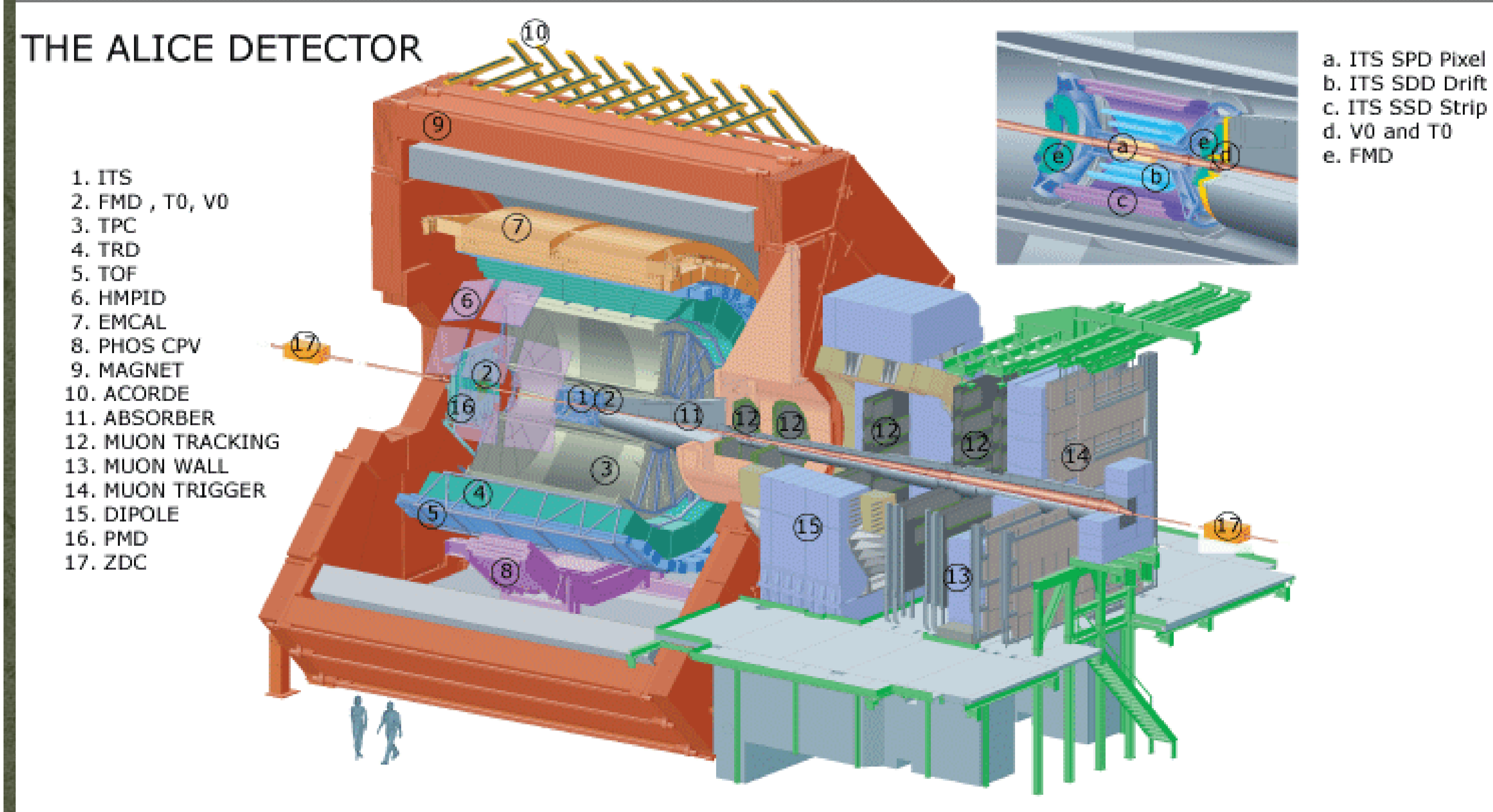
ALICE experiment

- A dedicated heavy-ion detector to exploit the unique physics potential of nucleus-nucleus interactions at LHC energies. It aims to study the physics of strongly interacting matter at extreme energy densities, where the formation of a new phase of matter, the quark-gluon plasma, is expected.
- The existence of such a phase and its properties are key issues in QCD for the understanding of confinement and of chiral-symmetry restoration.
- For this purpose, ALICE intends to carry out a comprehensive study of the hadrons, electrons, muons and photons produced in the collision of heavy nuclei.
- ALICE will also study proton-proton collisions both as a comparison with lead-lead collisions and in physics areas where it is competitive with other LHC experiments.

Detectors of the ALICE experiment

- The Overview
  - First one needs to know the initial conditions, namely how powerful the collision was: this is done by measuring the remnants of the colliding nuclei in detectors made of high density materials located about 110 meters on both sides of ALICE (the ZDC's) and by measuring with the FMD, V0 and T0 the number of particles produced in the collision and their spatial distribution. T0 also measures with high precision the time when the event takes place.
- Tracking particles
  - An ensemble of cylindrical detectors (from inside out: ITS Pixels (ITS Drift, ITS Strips, TPC, TRD) measures at many points (over 100 just the TPC) the passage of each particle carrying an electric charge, so that its trajectory is precisely known. The ALICE tracking detectors are embedded in a magnetic field (produced by the huge red magnet!) bending the trajectories of the particles: from the curvature of the tracks one can find their momentum. The ITS is so precise that particles which are generated by the decay of other particles with a very short life time can be identified by seeing that they do not originate from the point where the interaction has taken place (the "vertex" of the event) but rather from a point at a distance of as small as a tenth of a millimeter.
- The particles' Identity
  - ALICE also wants to know the identity of each particle, whether it is an electron, or a proton, a kaon or a pion. In addition to the information given by ITS and TPC, more specialized detectors are needed: the TOFmeasures, with a precision better than a tenth of a billionth of a second, the time that each particle takes to travel from the vertex to reach it, so that one can measure its speed, while the HMPID measures the faint light patterns generated by fast particles and the TRD measures the special radiation very fast particles emit when crossing different materials, thus allowing to identify electrons. Muons are measured by exploiting the fact that they penetrate matter more easily than most other particles: in the forward region a very thick and complex absorber stops all other particles and muons are measured by a dedicated set of detectors: the muon spectrometer.
- Catching Photons
  - The photons (particles of light), like the light emitted from a hot object, tell us about the temperature of the system. To measure them, special detectors are necessary: the crystals of the PHOS, which are as dense as lead and as transparent as glass, will measure them with fantastic precision in a limited region, while the PMD and in particular the EMCal will measure them over a very wide area. The EMCal will also measure groups of close particles (called "jets") which have a memory of the early phases of the event.

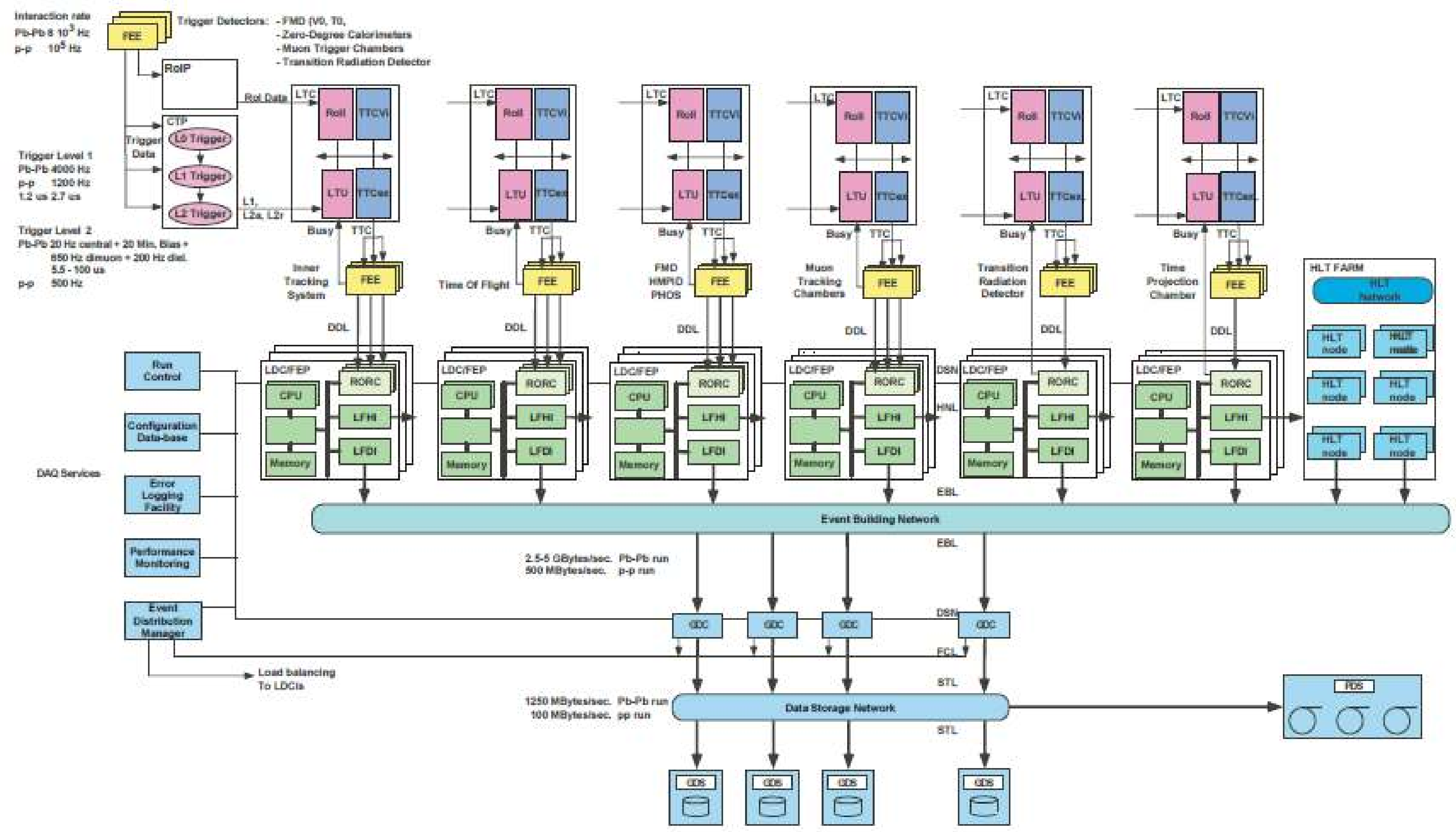
ALICE experiment



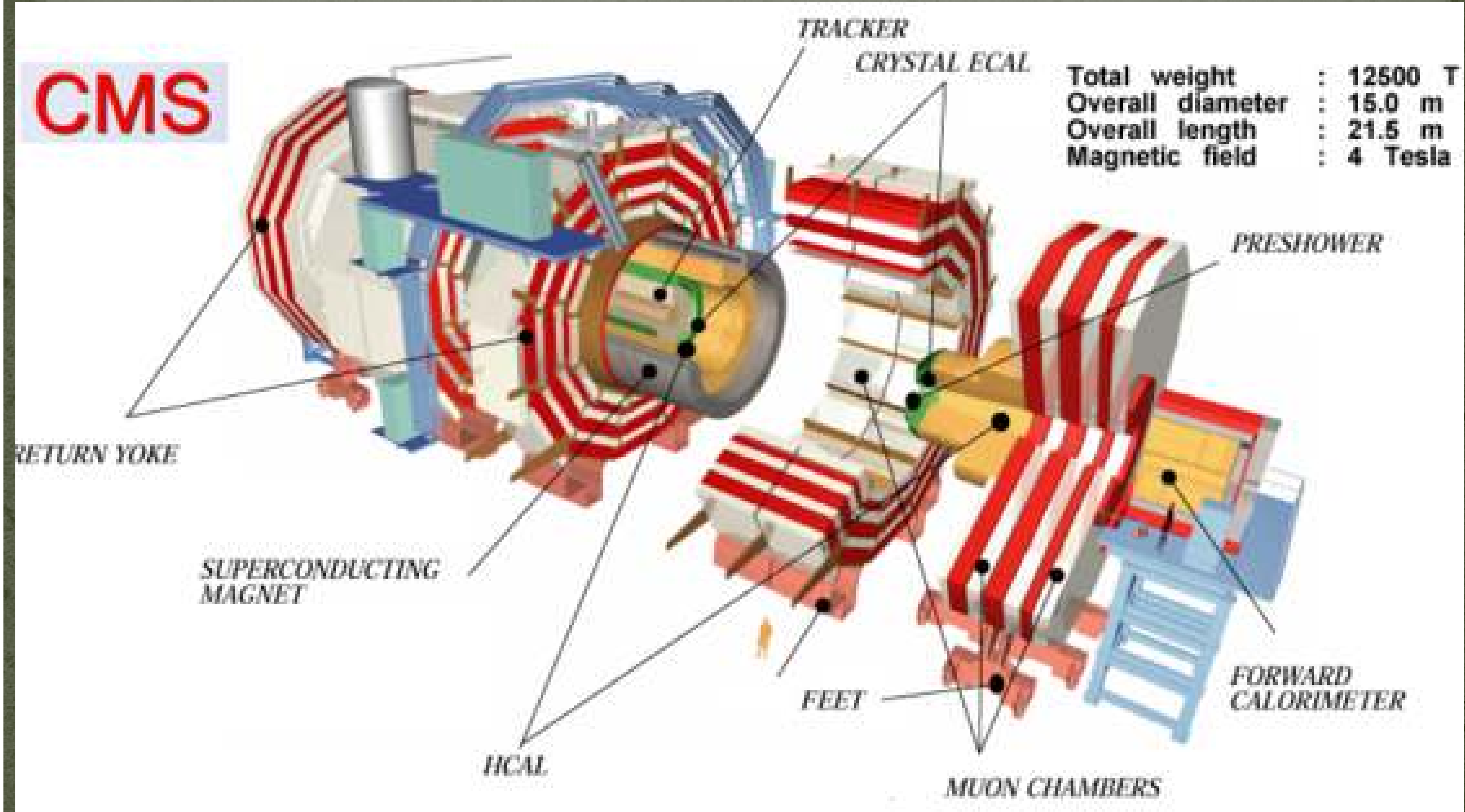
ALICE trigger and DAQ systems

- For every bunch crossing in the LHC machine, the Central Trigger Processor (CTP) decides within less than one microsecond whether to collect the data resulting from a particular collision.
- The trigger decision is distributed to the front-end electronics (FEE) of each detector via the corresponding Local Trigger Unit (LTU) and an optical broadcast system: the Trigger, Timing and Control system (TTC).
- Upon reception of a positive decision, the data are transferred from the detectors over the 400 optical Detector Data Links (DDL) via PCI adapters (RORC) to a farm of 300 individual computers; the Local Data Concentrator/Front-End Processors (LDC/FEP).
- The several hundred different data fragments corresponding to the information from one event are checked for data integrity, processed and assembled into sub events.
- These sub events are then sent over a network for the event building to one of the 40 Global Data Collector computers (GDC), which can process up to 40 different events in parallel.
- 20 Global Data Storage Servers (GDS) store the data locally before their migration and archive in the CERN computing center where they become available for the offline analysis.
- The hardware of the ALICE DAQ system is largely based on commodity components: PC's running Linux and standard Ethernet switches for the event building network. The required performances are achieved by the interconnection of hundreds of these PC's into a large DAQ fabric.
- The software framework of the ALICE DAQ is called DATE (ALICE Data Acquisition and Test Environment). DATE was used during the construction and testing phase of the experiment, while evolving gradually towards the final production system.

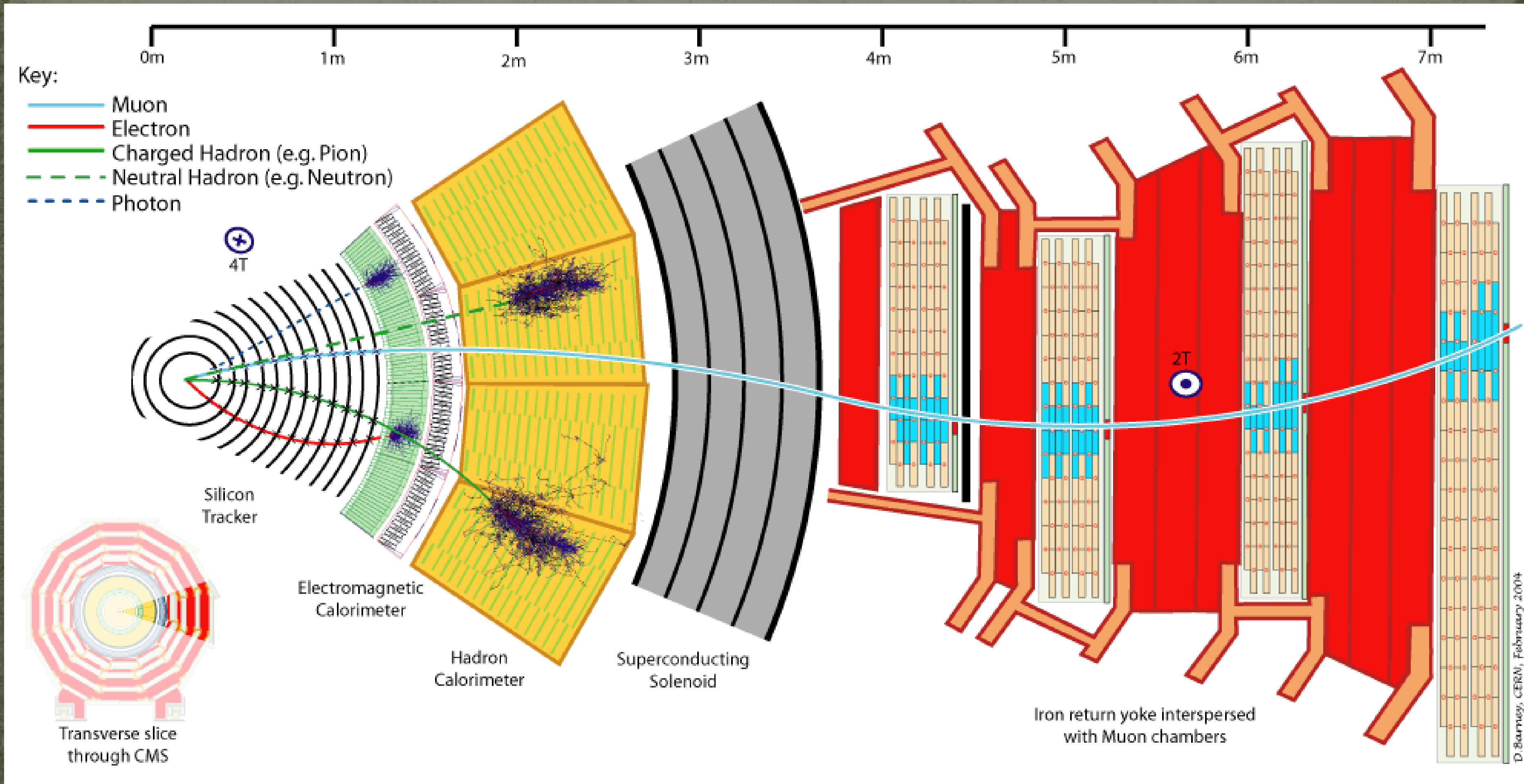
ALICE DAQ system



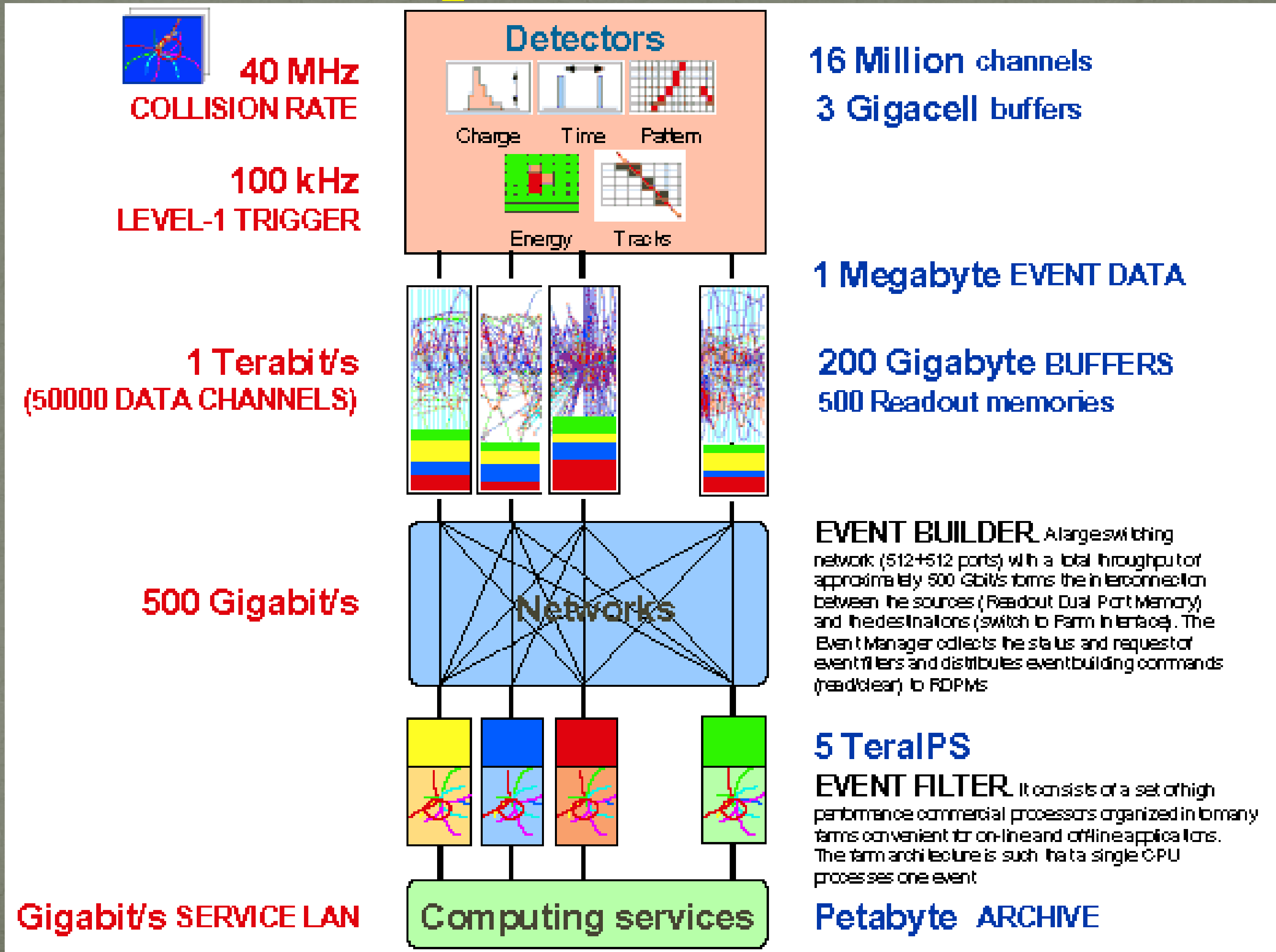
CMS experiment



A slice of CMS experiment



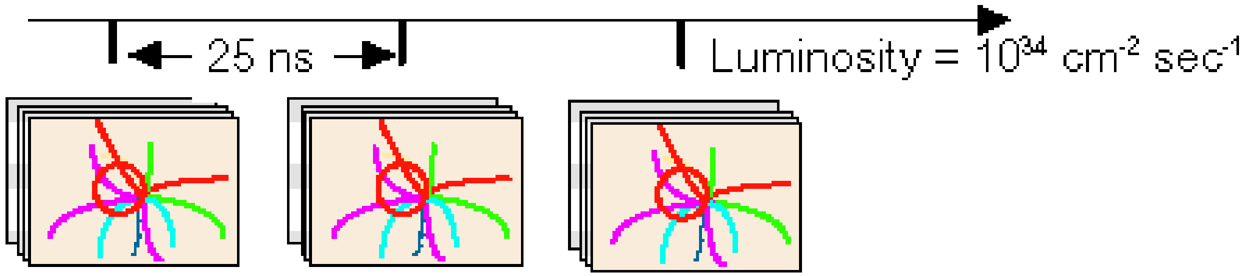
Principle of CMS DAQ



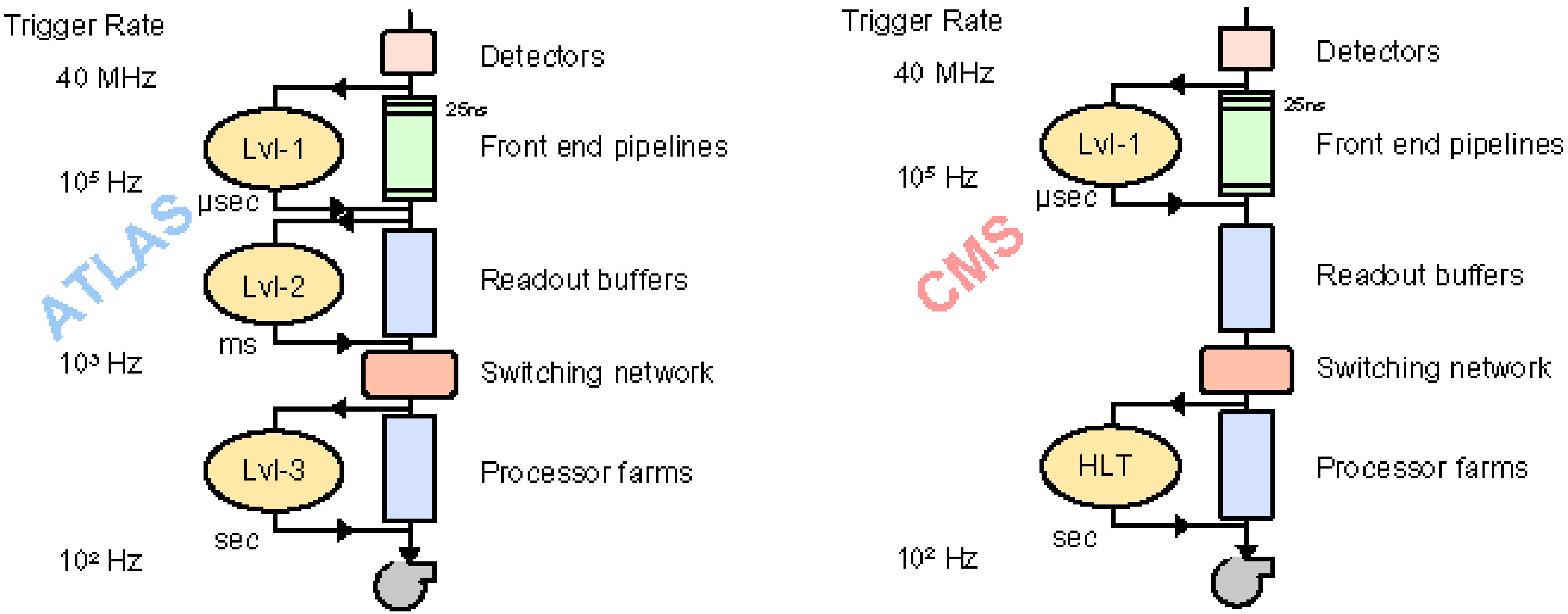
ATLAS/CMS Trigger architectures

- 30 Collisions/25ns
(10^9 event/sec)

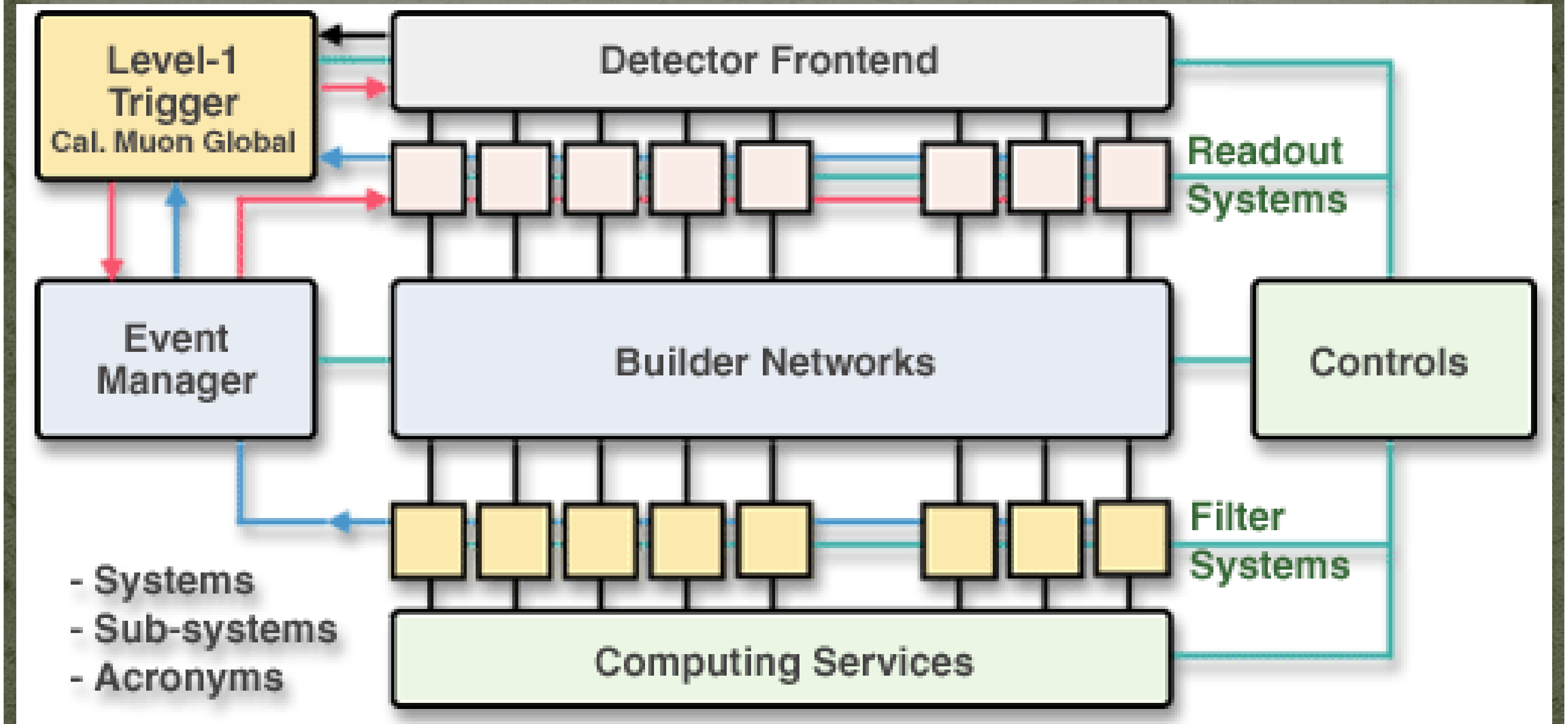
10^7 channels
(10^{16} bit/sec)



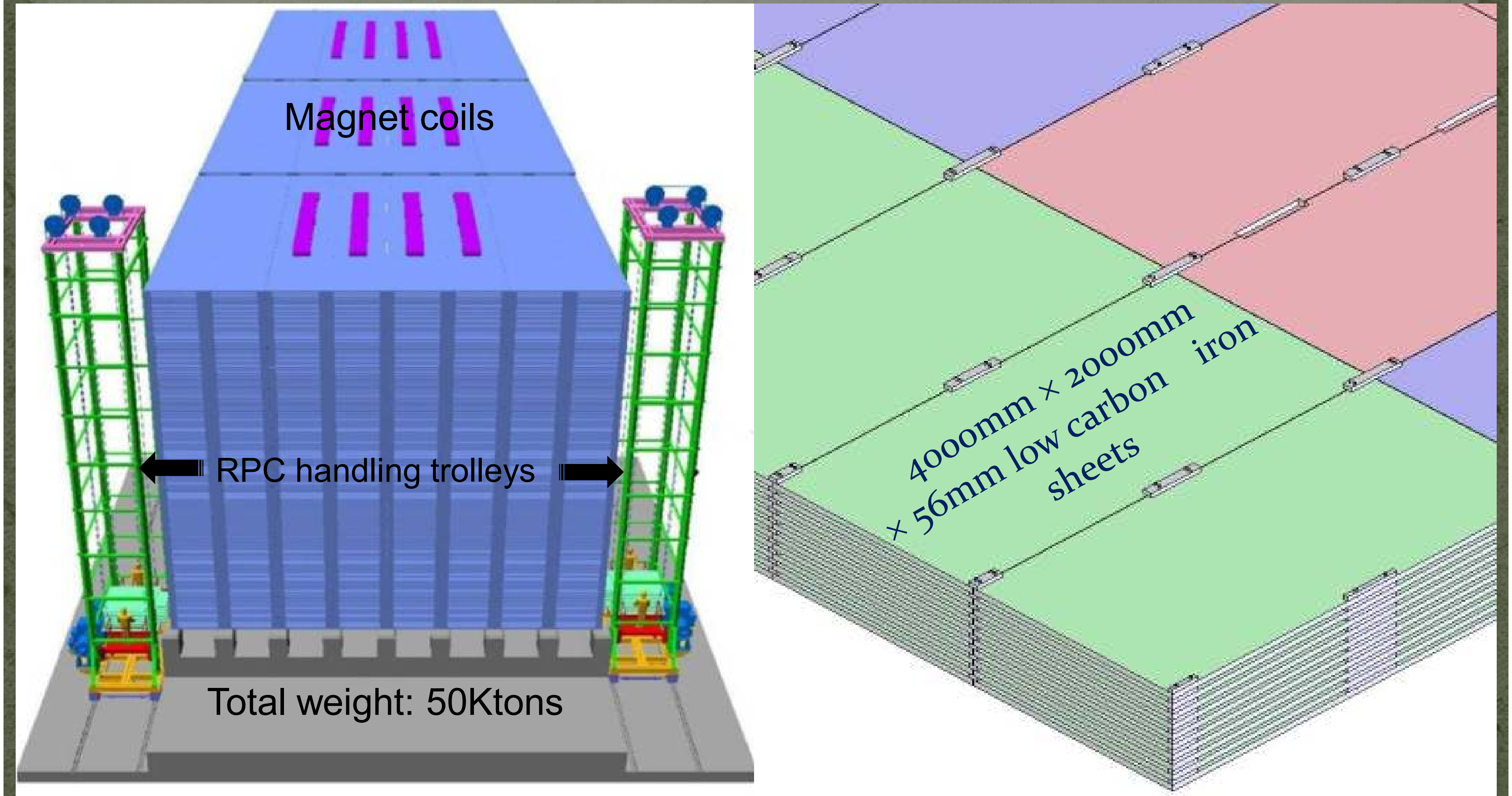
Multilevel trigger and readout systems



DAQ scheme of CMS experiment



INO's ICAL detector

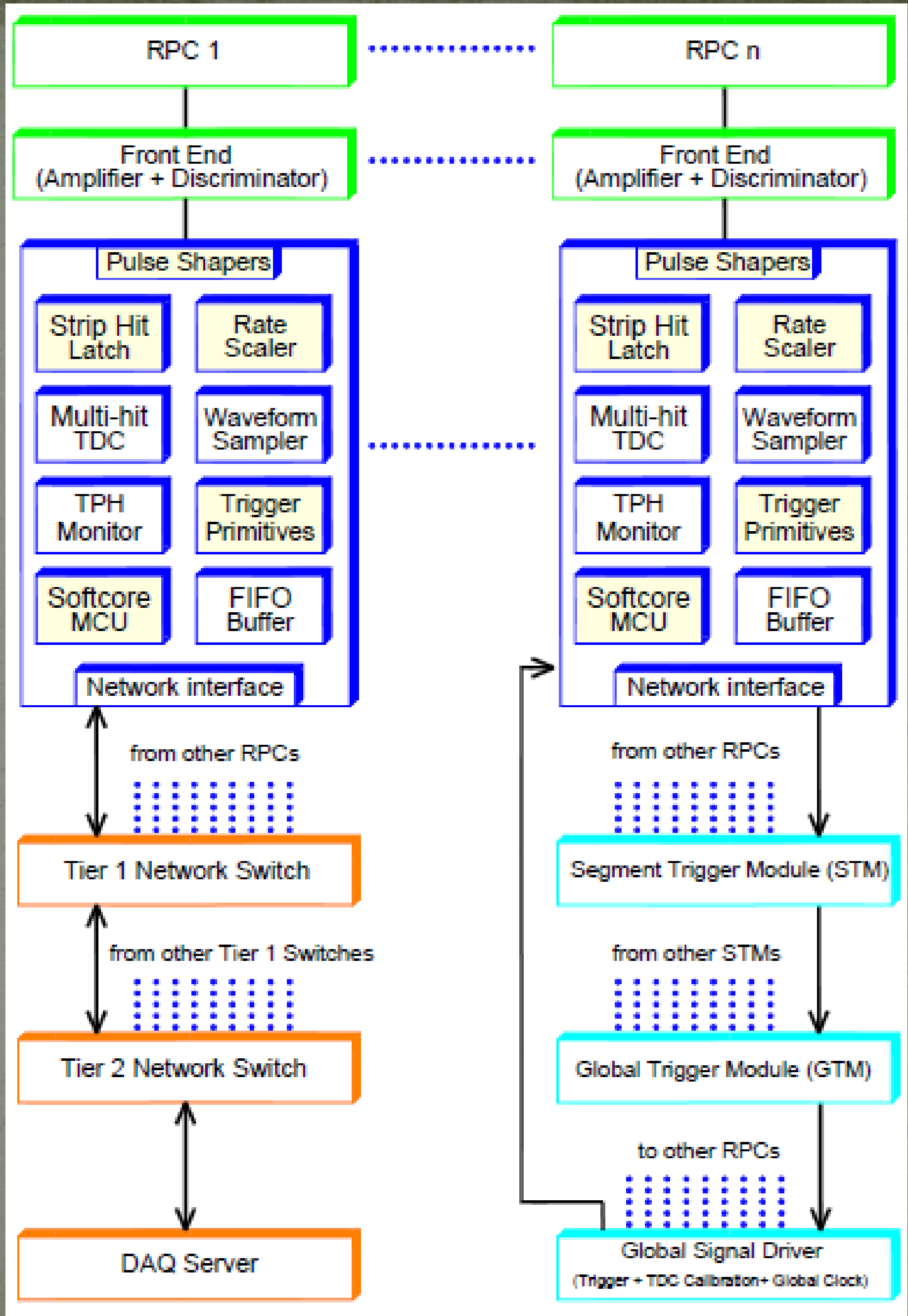


ICAL detector at a glance

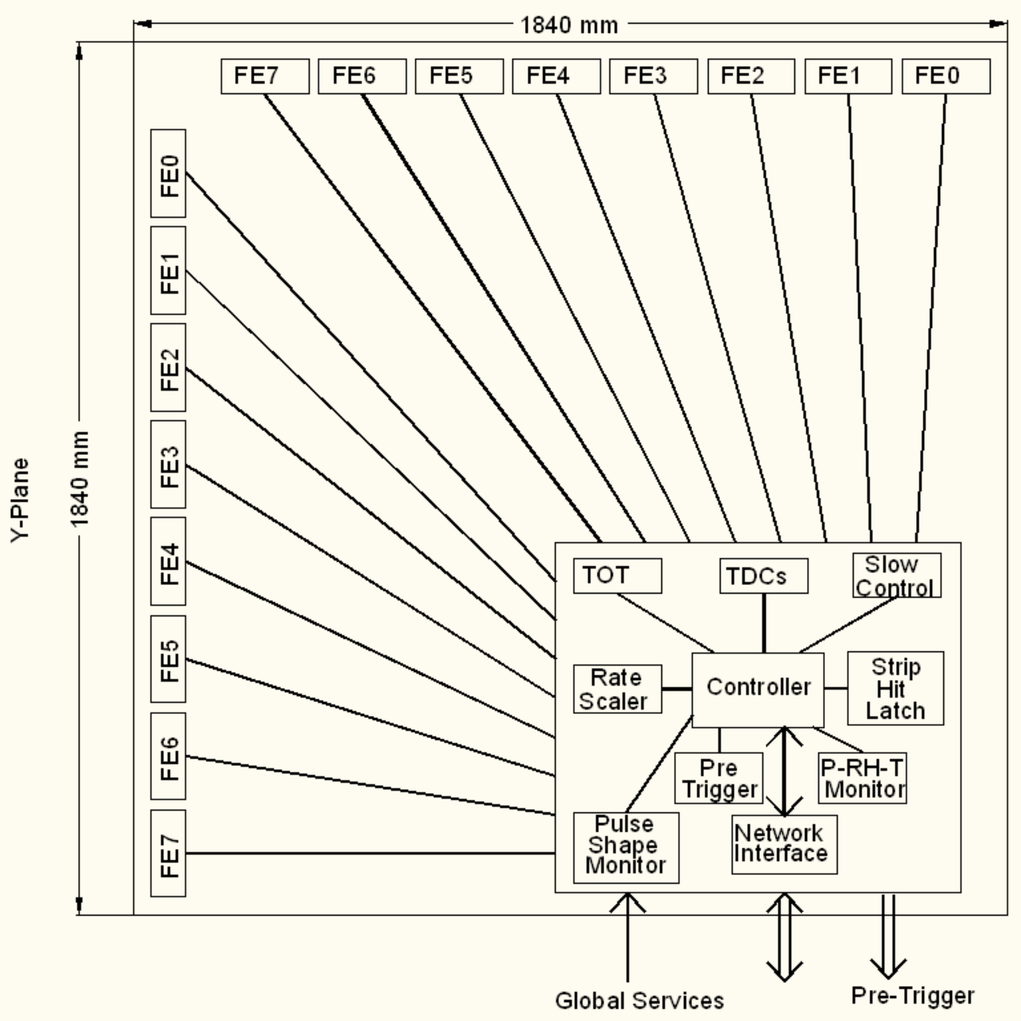
No. of modules	3
Module dimensions	16m × 16m × 14.5m
Detector dimensions	48.4m × 16m × 14.5m
No. of iron layers	151
Iron plate thickness	56mm
Gap for RPC trays	40mm
Magnetic field	1.3Tesla
RPC dimensions	1,950mm × 1,910mm × 26mm
Readout strip pitch	30mm
No. of RPCs/Road/Layer	8
No. of Roads/Layer/Module	8
No. of RPC units/Layer	192
No. of RPC units	28,800 (97,505m^2)
No. of readout strips	3,686,400

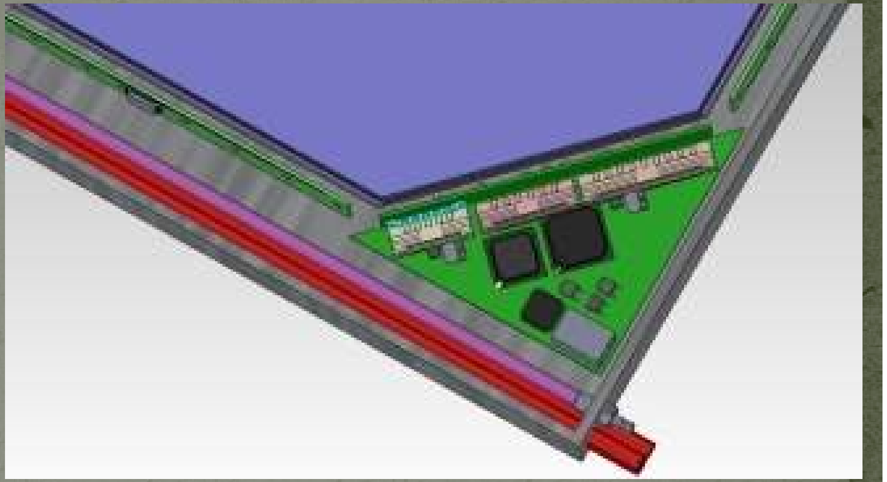
Overall scheme of ICAL electronics

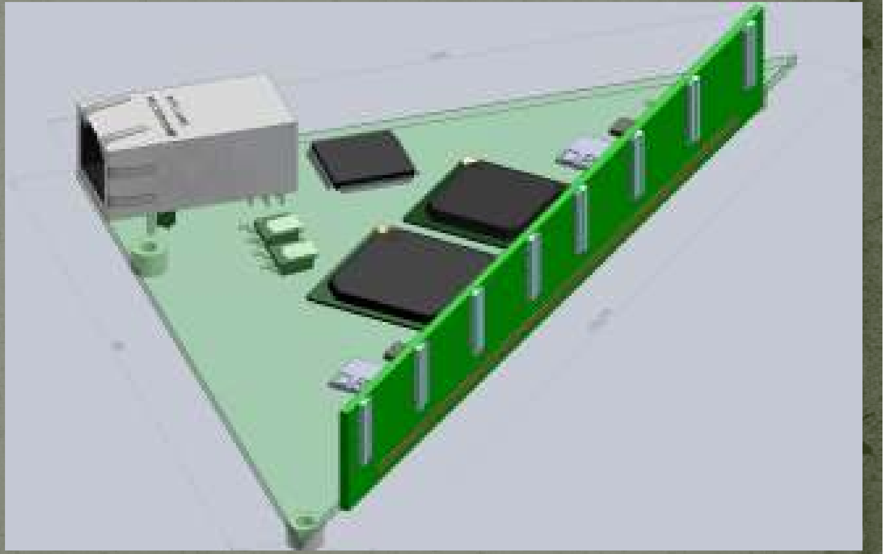
❖ Major elements
- Front-end board
- RPCDAQ board
- Segment Trigger Module
- Global Trigger Module
- Global Trigger Driver
- Tier1 Network Switch
- Tier2 Network Switch
- DAQ Server



Functions & integration of FE-DAQ

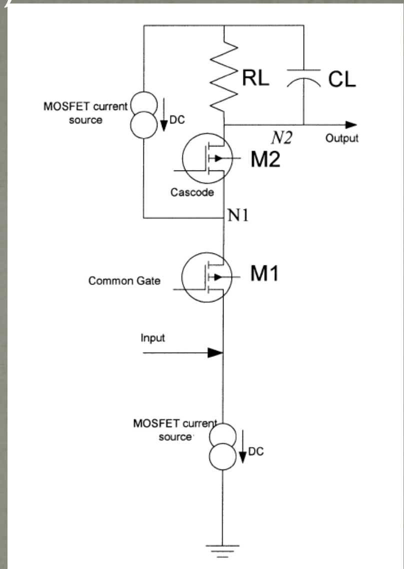


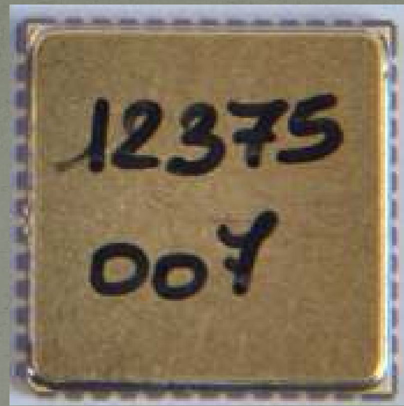


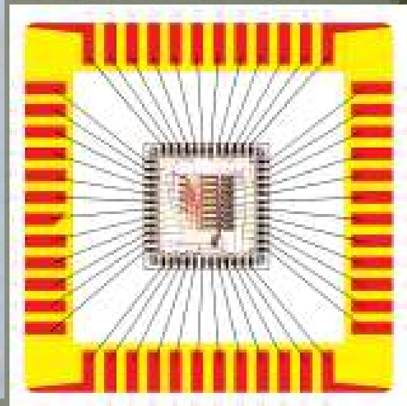


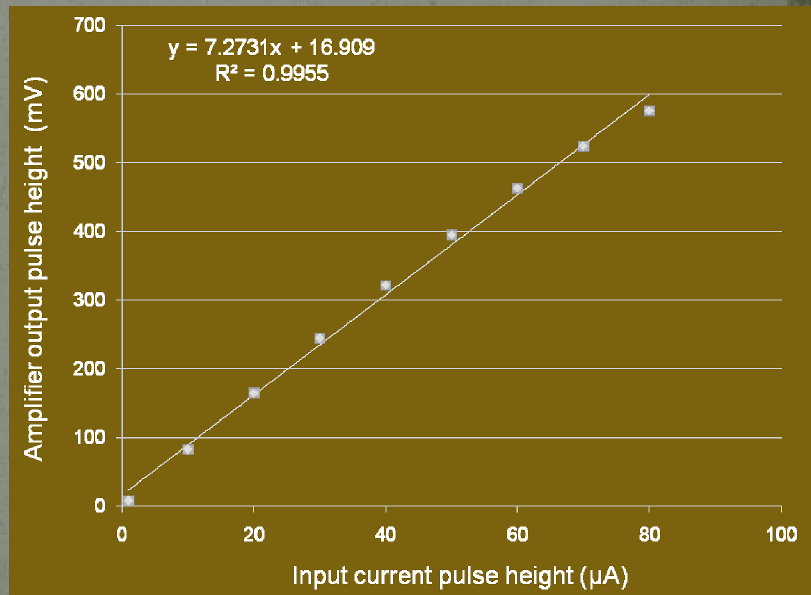
Picking up the tiny charges

- Process: AMSc35b4c3 (0.35um CMOS)
- Input dynamic range: 18fC – 1.36pC
- Input impedance: 45Ω @350MHz
- Amplifier gain: 8mV/μA
- 3-dB Bandwidth: 274MHz
- Rise time: 1.2ns
- Comparator's sensitivity: 2mV
- LVDS drive: 4mA
- Power per channel: < 20mW
- Package: CLCC48(48-pin)
- Chip area: 13mm²



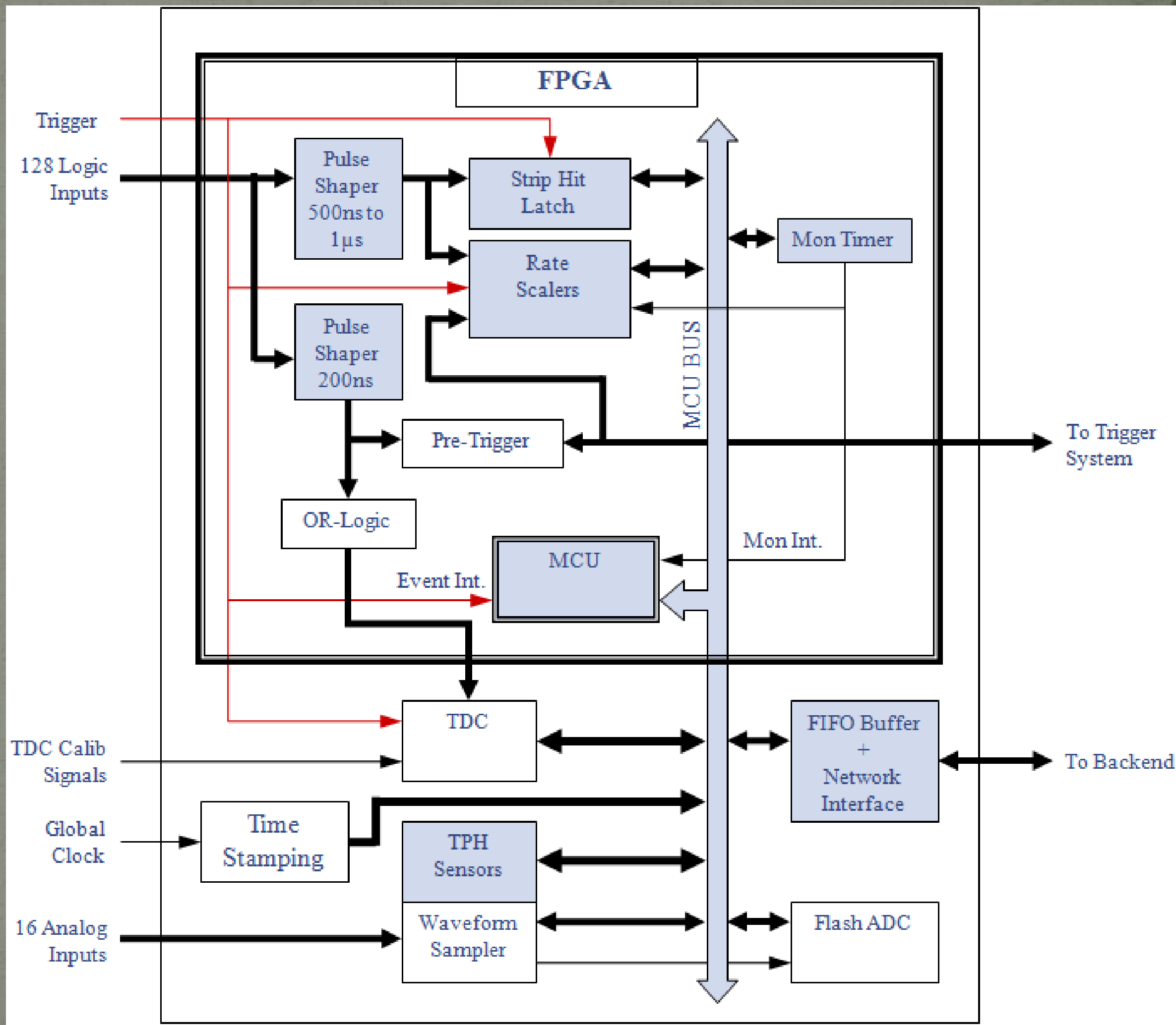






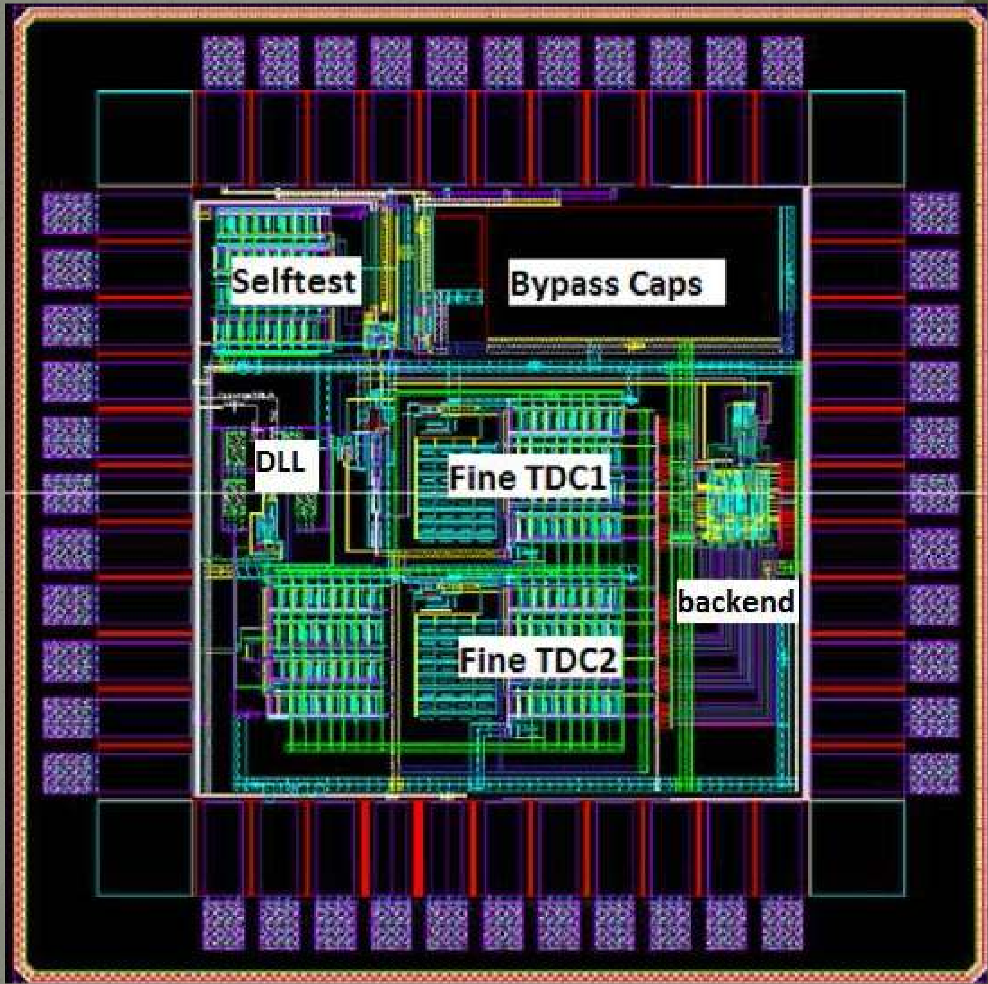
RPCDAQ module – the workhorse

- Unshaped, digitized, LVDS RPC signals from 128 strips (64x + 64y)
- 16 analog RPC signals, each signal is a summed or multiplexed output of 8 RPC amplified signals.
- Global trigger
- TDC calibration signals
- TCP/IP connection to backend for command and data transfer

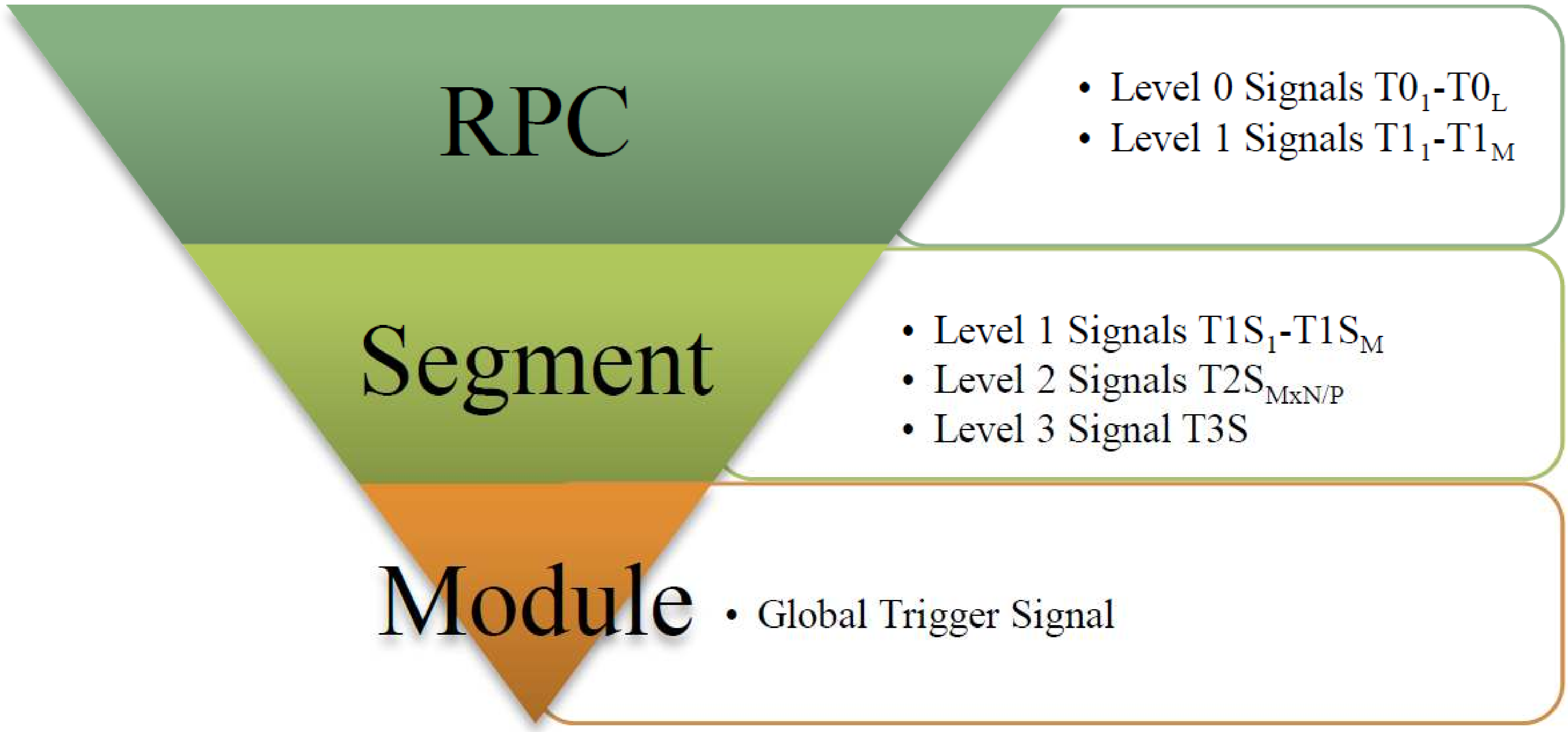


ASIC based TDC device

- Principle
  - Two fine TDCs to measure start/stop distance to clock edge (T_1, T_2)
  - Coarse TDC to count the number of clocks between start and stop (T_3)
  - TDC output = $T_3+T_1-T_2$
- Specifications
  - Currently a single-hit TDC, can be adapted to multi-hit
  - 20 bit parallel output
  - Clock period, T_c = 4ns
  - Fine TDC interval, $T_c/32$ = 125ps
  - Fine TDC output: 5 bits
  - Coarse TDC interval: $2^{15} * T_c$ = 131.072μs
  - Coarse TDC output: 15 bits



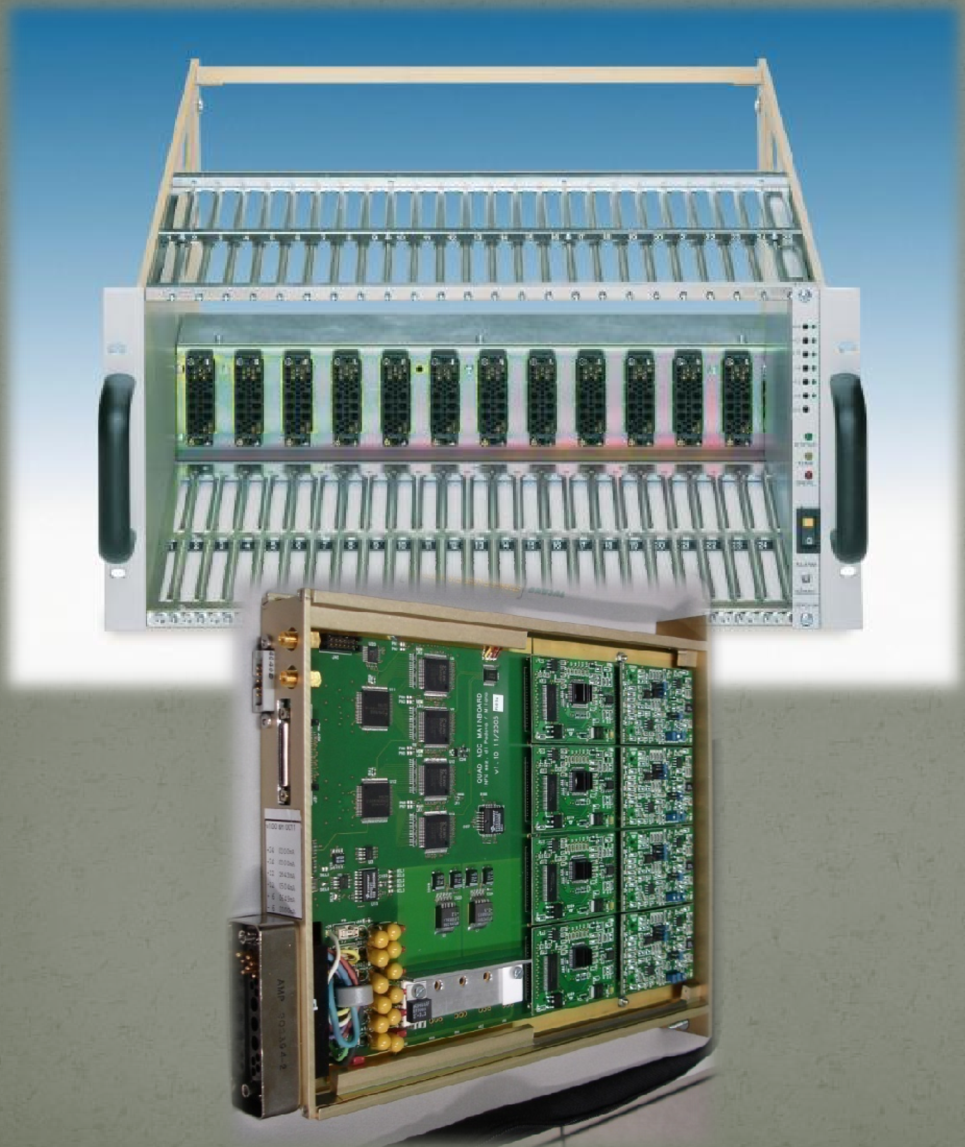
ICAL Trigger Scheme

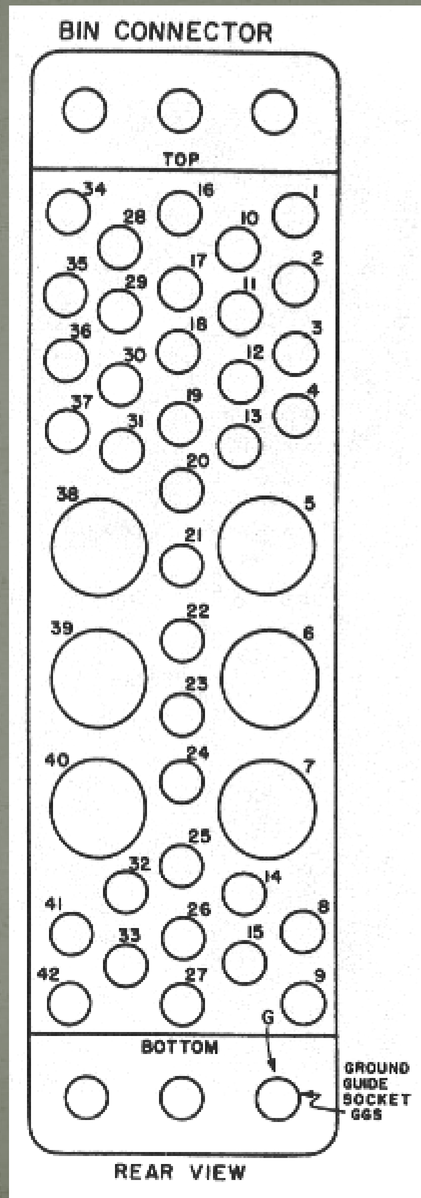


Introduction to NIM

- The NIM (Nuclear Instrumentation Methods) standard established in 1964 for the nuclear and high energy physics communities. The goal of NIM was to promote a system that allows for interchangeability of modules.
- Standard NIM modules are required to have a height of 8.75", width in multiples of 1.35". Modules with a width of 1.35" are referred to as single width modules and modules with a width of 2.7" are double width modules, etc. The NIM crate, or NIM bin, is designed for mounting in EIA 19" racks, providing slots for 12 single-width modules. The power supply, which is in general, detachable from the NIM bin, is required to deliver voltages of +6 V, -6 V, +12 V, -12 V, +24 V, and -24 V.
- The NIM standard also specifies three sets of logic levels.
  - In fast-negative logic, usually referred to as NIM logic, logic levels are defined by current ranges. Since the standard also requires 50 ohm input/out impedances, these current ranges correspond to voltages of 0 V and -0.8 V for logic 0 and 1 respectively. Fast-negative logic circuitry can provide NIM signal with rise times of order 1 nsec.
  - Slow-positive logic, is rarely used in fast-pulse electronics due to the slow rise times involved.
  - Specifications for ECL (emitter-coupled logic) voltage levels and interconnections have been added to the NIM subsequently.

NIM crate and power supplies

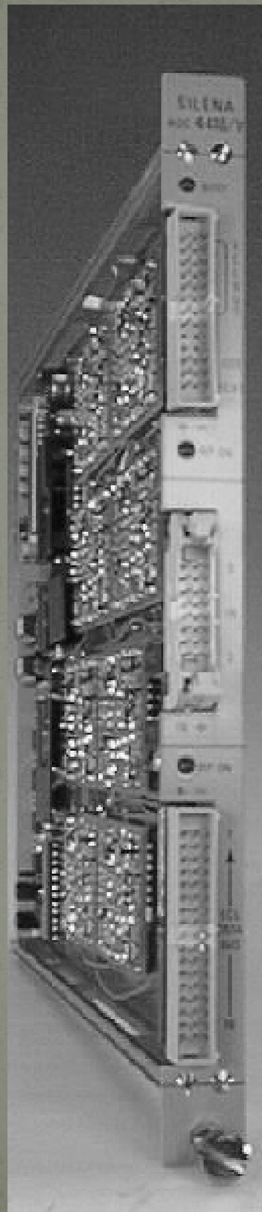


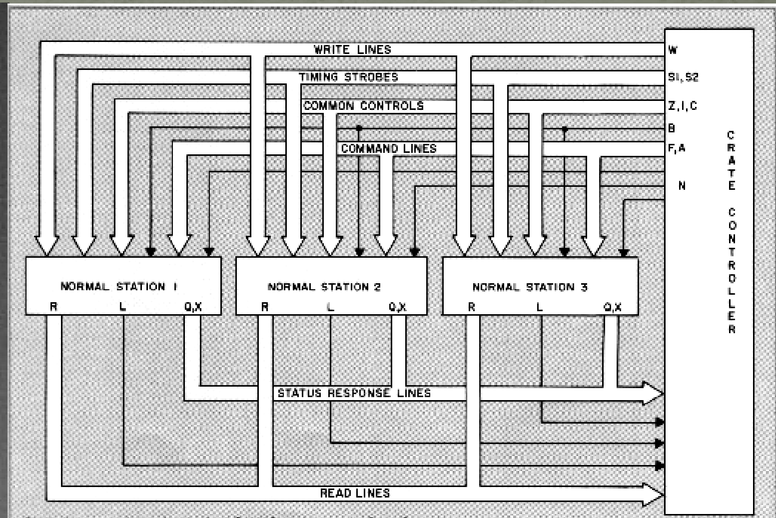


PIN	FUNCTION
1	RESERVED
2	RESERVED
3	BIN GATE
4	RESERVED
5	
6	
7	
8	+200 V D.C.
9	SPARE
* 10	+6 V
* 11	-6 V
12	RESERVED
13	SPARE
14	SPARE
15	RESERVED
* 16	+12 V
* 17	-12 V
18	SPARE
19	RESERVED
20	SPARE
21	SPARE
22	RESERVED
23	RESERVED
24	RESERVED
25	RESERVED
26	SPARE
27	SPARE
* 28	+24 V
* 29	-24 V
30	SPARE
31	SPARE
32	SPARE
33	117 V A.C. (HOT)
* 34	POWER RETURN GND
* 35	RESET
36	GATE
37	SPARE
38	
39	
40	
* 41	117 V A.C. (NEUTRAL)
* 42	HIGH QUALITY GND
G	GROUND GUIDE PIN

** Must be bussed to all bin connectors GPIB through PG12B.*

CAMAC hardware and signals

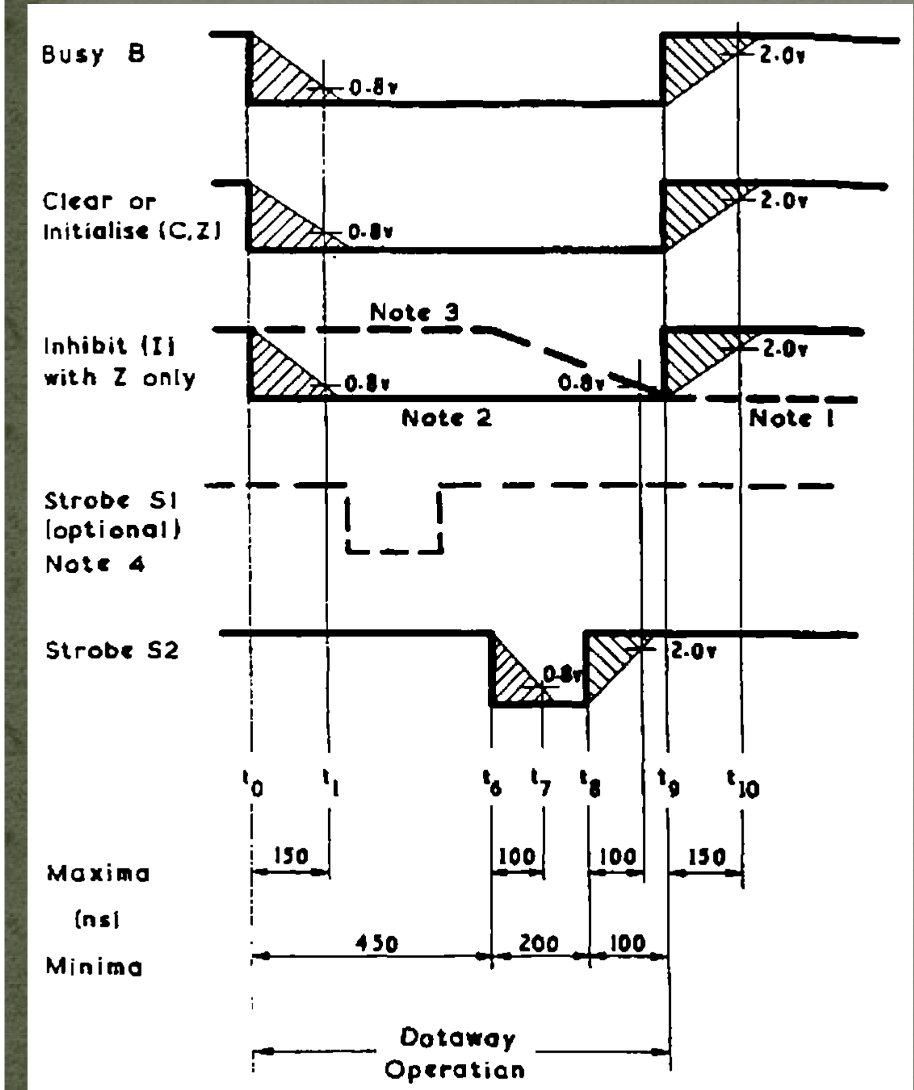


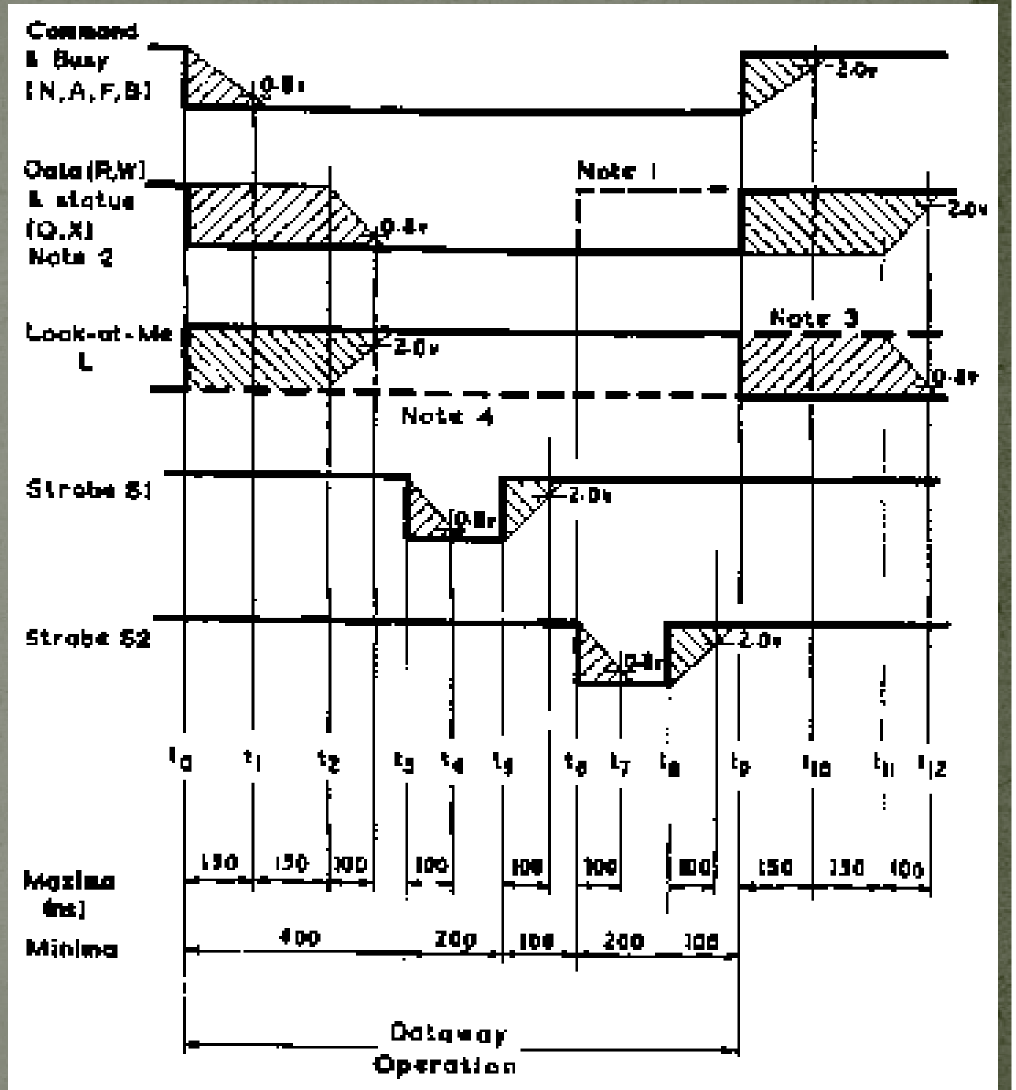


Block diagram and signal paths for 3 CAMAC modules and a Crate Controller.

TITLE	DESIGNATION	CON-TACTS	USE AT A MODULE
Command			
Station Number	N	1	Selects the module (individual line from control station).
Sub-Address	A1, 2, 4, 8	4	Selects a section of the module.
Function	F1, 2, 4, 8, 16	5	Defines the function to be performed in the module.
Timing			
Strobe 1	S1	1	Controls first phase of operation. (Dataway signals may change.)
Strobe 2	S2	1	Controls second phase. (Dataway signals may change.)
Data			
Write	W1-W24	24	Bring information to the module.
Read	R1-R24	24	Take information from the module.
Status			
Look-at-Me	L	1	Indicates request for service (individual line to control station).
Busy	B	1	Indicates that a Dataway operation is in progress.
Response	Q	1	Indicates status of feature selected by command.
Command Accepted	X	1	Indicates that module is able to perform action required by the command.
Common Controls			Operate on all stations connected to them, no command required.
Initialize	Z	1	Sets module to a defined state. (accompanied by S2 and B).
Inhibit	I	1	Disables features for duration of signal.
Clear	C	1	Clears registers (accompanied by S2 and B).
Non-Standard Connections			
Free bus-lines	P1, P2	2	For specified uses.
Patch Contacts	P3-P5	3	For unspecified interconnections. No Dataway lines.
Mandatory Power Lines			
+24 V DC	+24	1	
+6 V DC	+6	1	
-6 V DC	-6	1	
-24 V DC	-24	1	
0 V	0	2	Power return.
Additional Power Lines			Lines are reserved for the following power supplies.
+12 V DC	+12	1	Low current for indicators, etc.
-12 V DC	-12	1	
Clean Earth	E	1	Reference for circuits requiring clean earth.
Reserved Y1, Y2	2		Reserved for future allocation.

CAMAC dataway timing charts





Computer Automated Measurement and Control

CAMAC system development

System layers

CAMAC Hardware

CAMAC controller and PC interface

Serial, Parallel, GPIB, USB and Ethernet interfaces

Driver software

Operating System specific

Application program

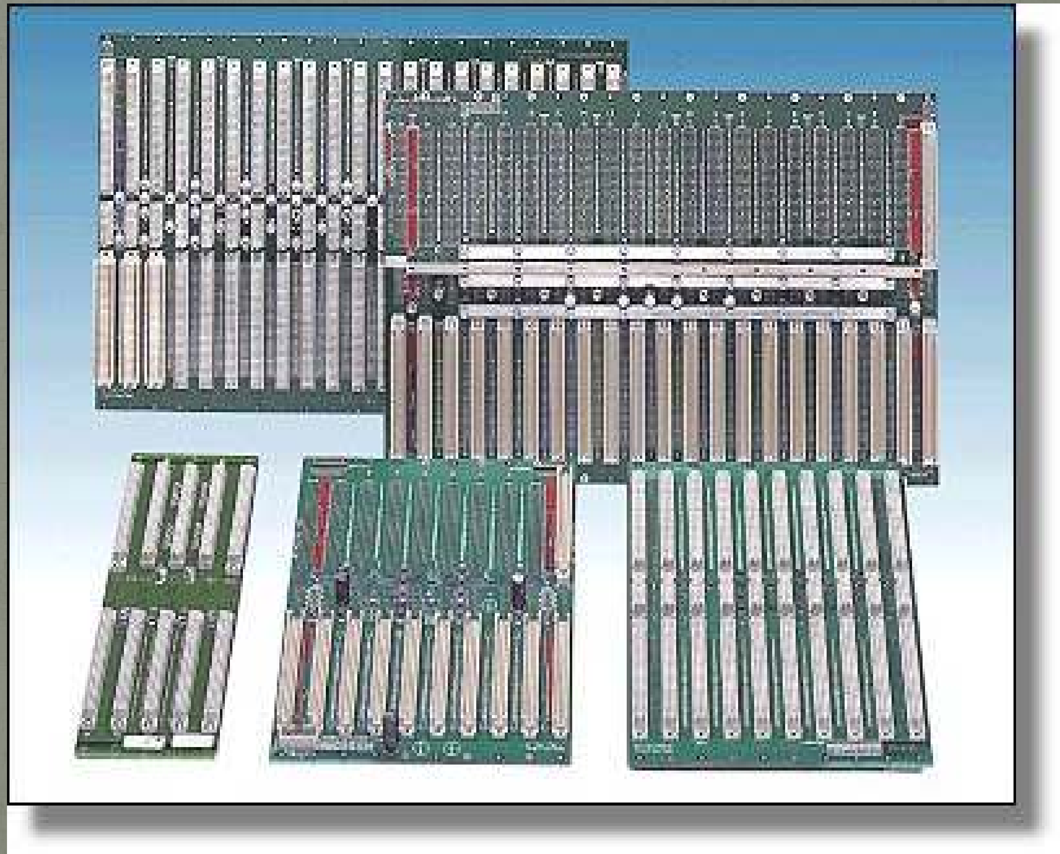
DAQ system specific

Software library

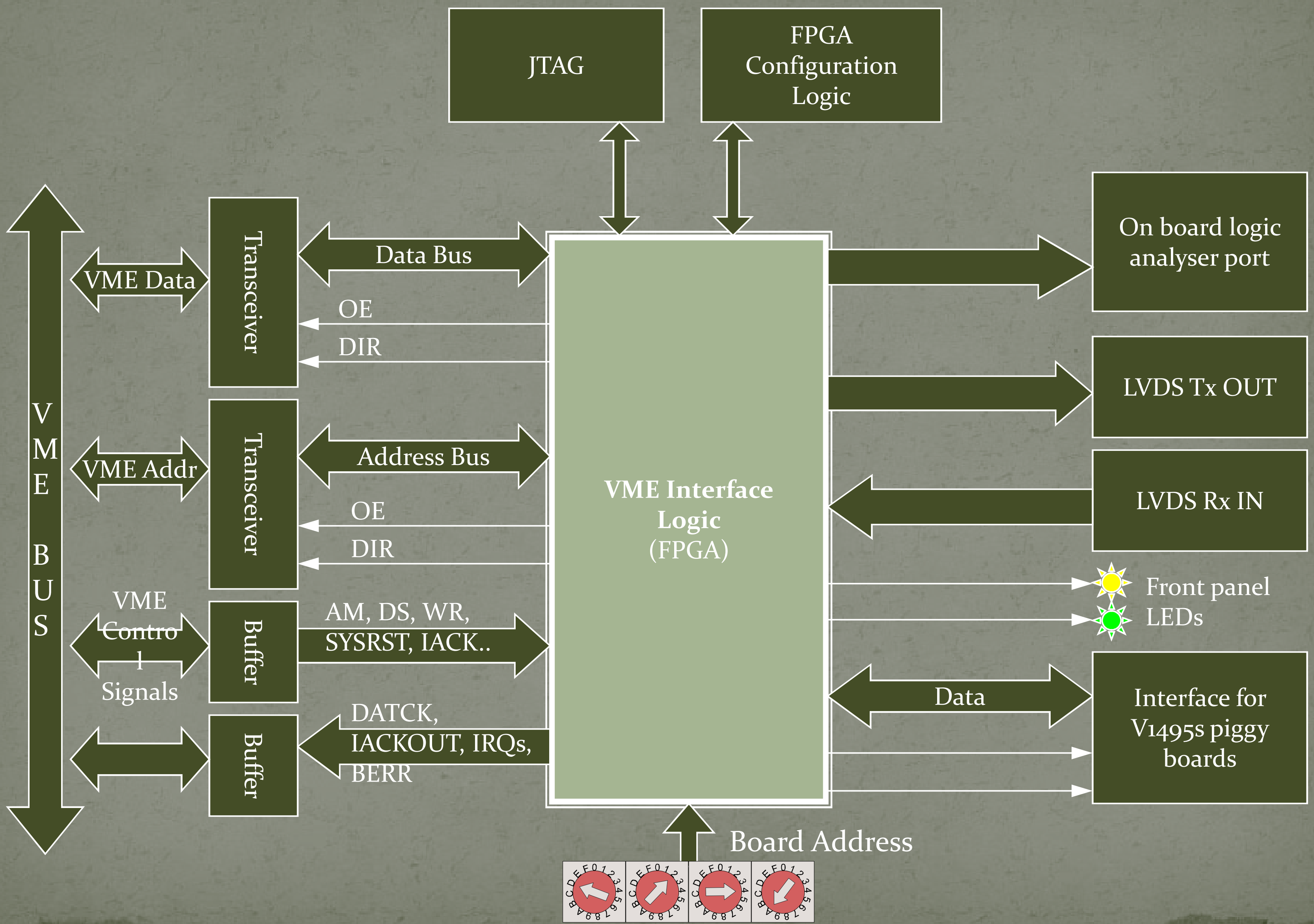
Programming Language specific

VME system hardware components

- ❖ "VERSA-module Europe"
- ❖ A modern fast, high density, modular, scientific instrumentation standard.
- ❖ Bandwidth up to 40MBytes/s (compare with 1MByes/s of CAMAC)



Custom VME Module



Elimination of noise - differential signalling

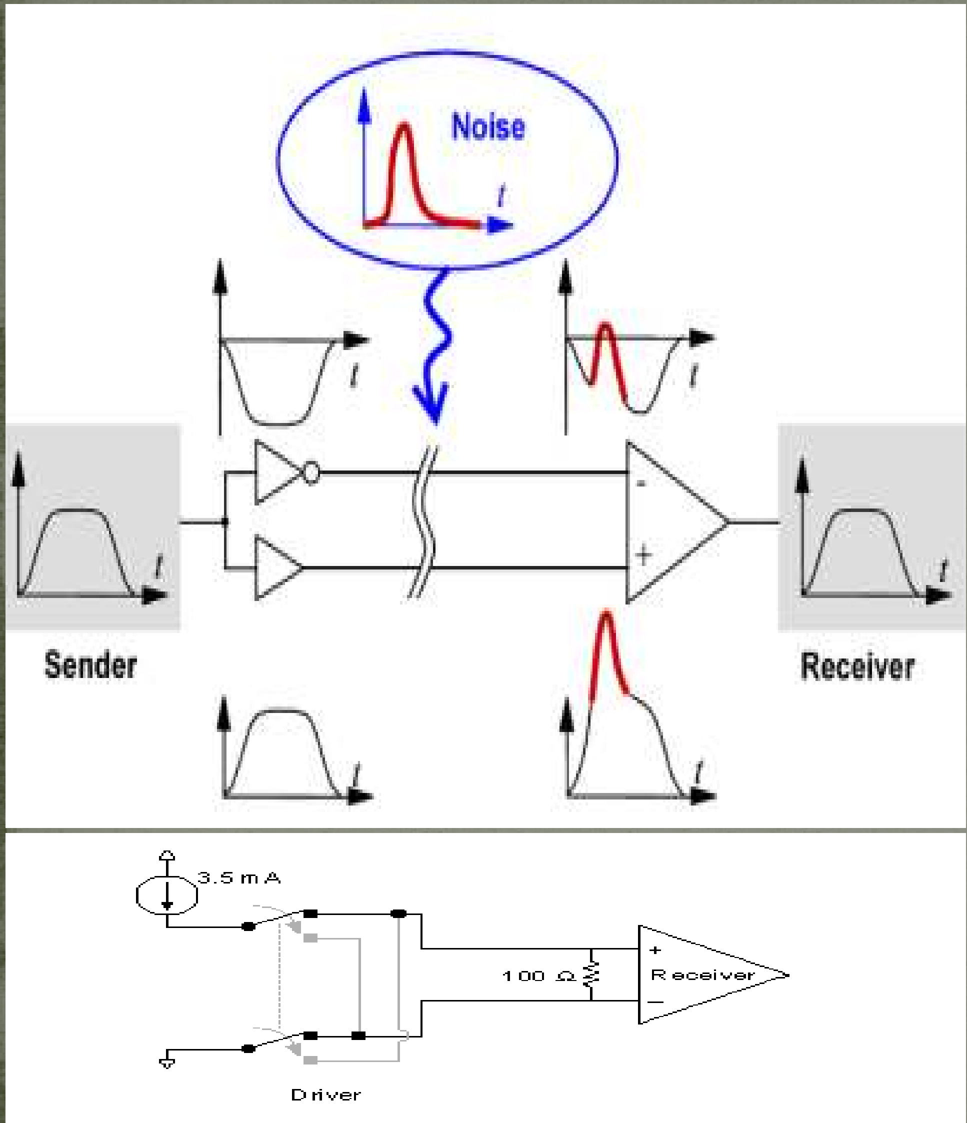


Figure 1. LVDS Driver and Receiver

In differential signaling, the transmitter translates the single input signal into a pair of outputs that are driven 180° out of phase. Since external interference tend to affect both the wires together, the receiver recovers the signal as the difference in the voltages on the two lines thus improving immunity to such problems. This transmission scheme provides large common-mode rejection and noise immunity to a data transmission system that a single-ended system referenced only to ground cannot provide.

Advantages of LVDS

- Ability to reject common-mode noise
  - When the two lines of a differential pair run adjacent and in close proximity to one another, environmental noise, such as EMI (electromagnetic interference), is induced upon each line in approximately equal amounts. Because the signal is read as the difference between two voltages, any noise common to both lines of the differential pair is subtracted out at the receiver. The ability to reject common-mode noise in this manner makes LVDS less sensitive to environmental noise and reduces the risk of noise related problems, such as crosstalk from neighboring lines.
- Reduced amount of noise emission
  - When the two adjacent lines of a differential pair transmit data, current flows in equal and opposite directions, creating equal and opposite electromagnetic fields that cancel one another. The strength of these fields is proportional to the flow of current through the lines. Thus the lower current flow in an LVDS transmission line produces a weaker electromagnetic field than other technologies.
- Flexibility around their power supply
  - LVDS offers designers flexibility around their power supply solution, working equally well at 5V, 3.3V and lower.

References and acknowledgements

- Paul Horowitz & Winfield Hill, The Art of Electronics, Cambridge University Press (1980)
- C.F.G.Delaney, Electronics for the Physicist with Applications, John Wiley & Sons (1980)
- W.R.Leo, Techniques for Nuclear and Particles Physics Experiments, Narosa (1987)
- G.F. Knoll, Radiation detection and measurement, John Wiley & Sons (2000)
- Anant Agarwal & Jeffrey H. Lang, Foundations of Analog and Digital Electronic Circuits, Morgan Kaufmann (2006)
- Albert Paul Malvino, Electronic Principles, Tata McGraw-Hill (2007)
- Stefaan Tavernier, Experimental Techniques in Nuclear and Particle Physics, Springer (2010)
- Stephan Henzler, Time-to-Digital Converters, Springer (2010)

- P.W.Nicholson, G.G.Eichholz & J.W.Poston, E.Fenyves & O.Haiman, L.B.Robinson, G.Hall, M.C.S.Williams, JÖrgen Christiansen, Stefan Ritt
- ALICE, ATLAS, CMS and INO collaborations

Thank you

For your attention.
Lecture slides are available on my web page:
http://www.tifr.res.in/~bsn/other.html