Memory look-up table based trigger module*

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1 Introduction to trigger systems

All modern experiments and detectors require some form of trigger to initiate or veto (or clear) the data acquisition system. Requirements for trigger systems include high speed, need to interrogate many detectors and to correlate the information from each detector element. Trigger systems are usually implemented using layered structures.

Multiple triggers are a composite of several successive triggers, each of increasing restrictivity. The combination allows complex and selective triggers with much lower dead time than a comparable single level trigger. Each level of trigger provides a filter for the next level so somewhat slower but sophisticated triggers can be employed.

The first level trigger modules are designed to be part of a system that provides triggers based on the high input rates and simple and fast hardware logic. These modules receive inputs directly from the detectors after required signal conditioning. Logic registers and summing amplifiers are examples of these modules. For more complex trigger conditions, the first level trigger decision must gate subsequent trigger activities and processing to achieve a practical rate.

Subsequent level(s) provide higher level triggers based on more sophisticated but slow logic based upon the results of actual detector measurements and event parameter estimates. Examples are track finding through a sequence of detector elements, energy calibration, peak energy determination, centroid finding and

*Lecture notes for the first SERC School on Experimental High Energy Physics held at T.I.F.R, Bombay during January 1995 momentum and rapidity calculations. These triggers are often implemented on computer systems employing complex algorithms such as those based on Artificial Intelligence and Neural Network techniques.

2 Look-up table based trigger modules

A trigger module generates an exactly timed output signal whenever the time overlap of input signals satisfies a pre-selected coincidence requirement. Even though the traditional hardware AND(NAND) or OR(NOR) logic circuit based trigger modules may be used in the small experiments, they lack flexibility and versatility in their functions while handling large number of detector channels.

In contrast, look-up table based modules offer many advantages in addition to overcoming the drawbacks mentioned above when used in lower level of trigger systems. Look-up tables are usually implemented in memory chips which are commonly used in microprocessor and computer systems. Detector inputs based on which the trigger decision has to be taken are fed on the address lines to the chip, where as the output trigger patterns are indicated on its data lines. Look-up tables are generated using simple programs, essentially constructing the output patterns for every combination of input signals applying trigger criteria on that combination. Refer to Fig.2 for the concept of look-up table generation for Function #1 from the following table.

The look-up tables are then down loaded onto the chips. In case of ROM (Read Only Memory) chips, they are loaded using special hardware programmers. In case of RAM (Random Access Memory) and likes, the tables are usually down loaded from the data acquisition system hosts at the time of a run start or as and when changes are required in the trigger criteria. Once loaded with the look-up tables and appropriate signal lines are connected to the memory chips, they produce the programmed trigger patterns as and when the required set of detector channels produce signals in them satisfying those patterns. In other words, the status of detector channels connected to the address lines of the chip, form a unique address into the chip where the corresponding trigger pattern is already loaded. A logically enabled chip then outputs these patterns on its data lines.

Major advantage of this technique is evident from the fact that in order to make the changes in the trigger function, it is just enough if the tables implementing the changes are down loaded afresh. It is also easily possible to build complex systems by maintaining the same hardware interconnecting structure among the signals and operating them with look-up tables implementing different trigger functions.

3 Description of the circuit

A simple model circuit is designed to study the basic concepts of look-up table based trigger systems. Heart of this circuit of course is an EPROM (Erasable Programmable Read Only Memory) chip, 2732 mounted in a ZIF (Zero Insertion Force) socket which allows easy removal and insertion of the memory chip. It is of 4096 X 8-bit capacity, thus has 12 address lines (A_0-A_{11}) and 8 data lines (D_0-D_7). It also has two other pins for enabling the chip itself and the outputs. In this circuit, both these lines are always logically enabled.

Eight lines of a DIP switch set are connected to the address lines A_0-A_7 of the EPROM, simulating the actual signal inputs. Four lines of another DIP switch set are connected to the address lines A_8-A_{11}. These lines implement different trigger functions on the same data fed by the 8-line DIP switch. The following functions are implemented on this circuit for demonstration purpose.

Function		Trigger criteria
Deci	Bin	
0	0000	Veto. Disable trigger.
1	0001	Indicate number of active inputs. Output is in binary format.
2	0010	Trigger on 3 or more active inputs. Trigger status indicated by 8th (GREEN) LED.
3	0011	Trigger on 3 or more consecutive active inputs. Trigger status indicated by 8th (GREEN) LED.
4	0100	Indicate number of active inputs by the corresponding output line, i.e n-th fold indicated by n-th LED.
5	0101	Trigger on at least one 4-fold coincidence from two sections of input lines; 1-4 and 5-8. Trigger status indicated by 8th (GREEN) LED.

The data bus of the EPROM is driven by 74LS240, to the output bus of which a bank of 8 LEDs are connected. The output trigger patterns are indicated by the LEDs. The circuit board takes in +12 volts as its required power supply voltage, from which VCC (+5V) is derived using a 3-terminal regulator chip, 7805.

It is important to note that both the data inputs fed with the help of DIP switches as well as the trigger patterns indicated by the LEDs are all represented in the binary (radix 2) format.

4 Studies and discussions

As mentioned already, this circuit is meant only to study the concept of look-up table, hence doesn't employ any live input signals from the actual detectors. The idea essentially is to study the trigger patterns for various signal and function inputs given by the DIP switches. It is interesting to discuss how this building block may be used to design more complex trigger systems. One concept which one will not be able to study by this rather simplified circuit is the timing of input and output signals and the effect of memory chip's transmission delay on the system design. It is worth spending some time on these issues though.

A simple program is used to generate the look-up table implementing the functions mentioned in the above table. which is down loaded into the EPROM. One can study this program and practice writing such routines for implementing some of the common trigger functions. Finally, characteristics of some of the alternate devices which also may be used in these type of trigger module also can be discussed.