Basic Electronics course for the INO Graduate Training programme

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Autumn 2012 Time Table

Time (hrs)	Monday	Tuesday	Wednesday	Thursday	Friday
0930-1100	Particle Physics GM AG-69	Exp. Meth. II BSN, AS D-423	Exp. Meth. I VN D-423	Exp. Meth. II BSN, AS D-423	Exp.Meth. I VN D-423
1130-1300				Particle Physics GM AG-69	

Course Outline-1

- *Basic detector characteristics and output*
  - *Charge, current and voltage*
  - *Signal types: DC or pulse (and pulse shapes)*
- *Passive components*
  - *Resistors, capacitors, inductors,* impedance *and transformers*
  - *Integrators, differentiators,* LCR resonant circuits
- Generation and measurement of
  - Voltage, current, time, frequency
  - Measuring resistance, temperature, pressure, magnetic field and light
- *Basic semiconductor device physics*
  - *P-N junction, Diodes, I-V curve*
- *Rectifiers, DC power supplies, regulators, DC-DC converters*
- *Transistor characteristics*
  - *Transistor circuits:* emitter follower*, push-pull amplifier*
  - *Low noise devices: FET, JFET, MOSFET*

Course Outline-2

- *Operational amplifiers*
  - *Principle of Negative feedback*
  - *Differential amplifier*
  - *Applications: differentiator, integrator, amplifiers, summing amplifier, oscillators, comparators*
- Noise in detectors and electronics
  - Measurement and reduction of noise
  - Grounding and shielding
- *Digital electronics*
  - *Why digital?*
  - *Logic states, gates (OR, NOT, AND, NAND, NOR, XOR)*
  - Implementing arbitrary truth tables, Karnaugh maps
  - *Flip-flops, latches, registers, memories (RAM, ROMs, FIFO etc.)*
  - *Multiplexers, decoders, mono-stable multi-vibrators, counters*
- *Logic families*
  - *TTL, CMOS, LVDS*
- *Co-axial cables*
  - *Signal transmission and loss*
  - *Impedance matching*
  - *Noise and distortion*

Course Outline-3

- Commonly used front end electronics
  - *Preamplifiers, shaping amplifiers*
  - *Fast and slow coincidence,* logic & linear gates, logic & linear FIFO, *delay line*
  - *Discriminators: leading edge, constant fraction*
  - *Coincidence circuits*
  - Single channel analyser, multi-channel analyser

- ADC, DAC and TDC
  - *Performance parameters*
  - *ADC functions: Charge versus peak sensing*
  - *ADC types: Wilkinson, successive approximation, flash*
  - DAC and applications
  - *TDC: Principles, classical types, FPGA, ASIC*

- Some advanced topics
  - *Programmable logic: CPLD, FPGA*
  - Application Specific Integrated Circuits (ASICs)

- PC interfacing protocols and standards
  - Serial (RS-232, USB, SPI), parallel (Centronix, PCI)
  - *Modular instrumentation standards: NIM, CAMAC, VME*

Some info on the course

- Good news! The course will be taught at introductory rather than advanced level.
- You will be *possibly* be prepared to setup and run nuclear and high energy physics experiments.
- No. of class room hours = 30 hours (approx.), i.e. 20 x 1.5 hours
- Class days and hours: Tuesdays and Thursdays, 9:30am to 11am
- Class room: D-423
- Teaching method: PPT projection + blackboard
- A few additional guest lectures on specific topics are planned.

- Assessment:
  - Four assignments = 20 marks
  - Mid semester exam = 25 marks
  - End semester exam = 40 marks
  - Case-study work = 15 marks

Some references

- Stefaan Tavernier, Experimental Techniques in Nuclear and Particle Physics, Springer (2010).
- G.F. Knoll, Radiation detection and measurement, John Wiley & Sons (2000).
- W.R.Leo, Techniques for Nuclear and Particles Physics Experiments, Narosa (1987)
- Anant Agarwal & Jeffrey H. Lang, Foundations of Analog and Digital Electronic Circuits, Morgan Kaufmann (2006)
- Paul Horowitz & Winfield Hill, The Art of Electronics, Cambridge University Press (1980)
- Albert Paul Malvino, Electronic Principles, Tata McGraw-Hill (2007)

Thankful to these authors. A lot of material and figures from the above mentioned books will be used in this course.

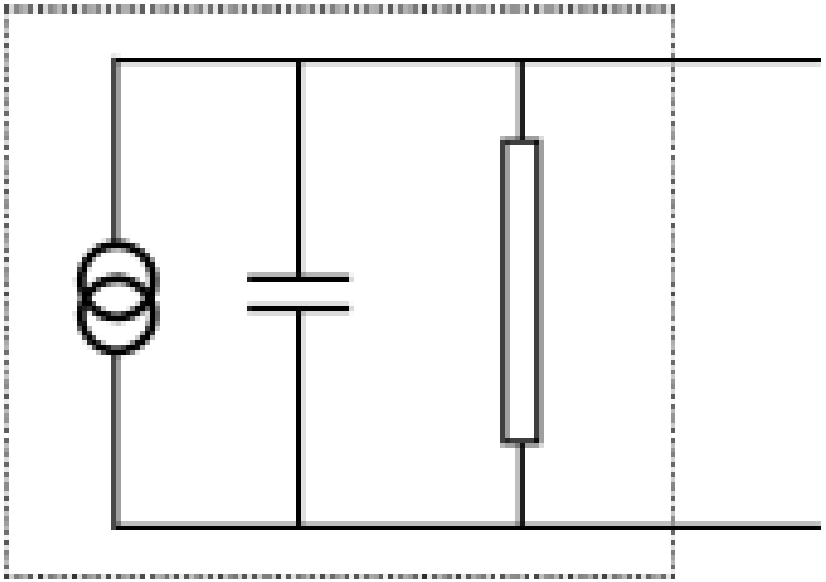
August 16, 2012

LECTURE-1

Basic detector characteristics and output

- Detection of ionising radiation in the end nearly always comes down to detecting some small electrical signal.
- Dealing with such small signals is one of the main challenges in designing detectors for nuclear physics and particle physics.

- From the electrical point of view, a detector is a current source with a large internal resistance and a small capacitance.
- In the absence of any ionising radiation there is a small current, which is called the dark current or leakage current.

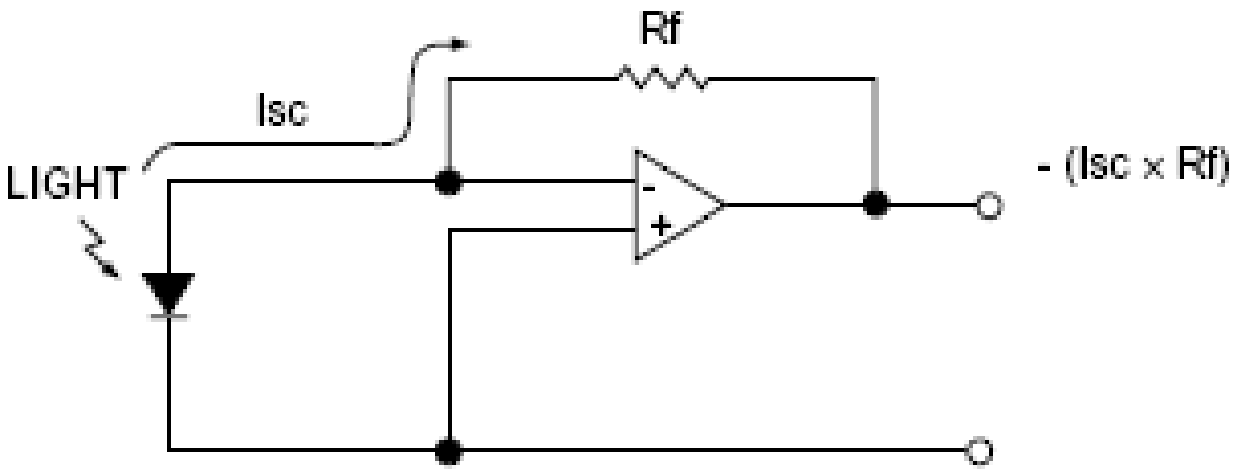


Modes for measuring detector signals

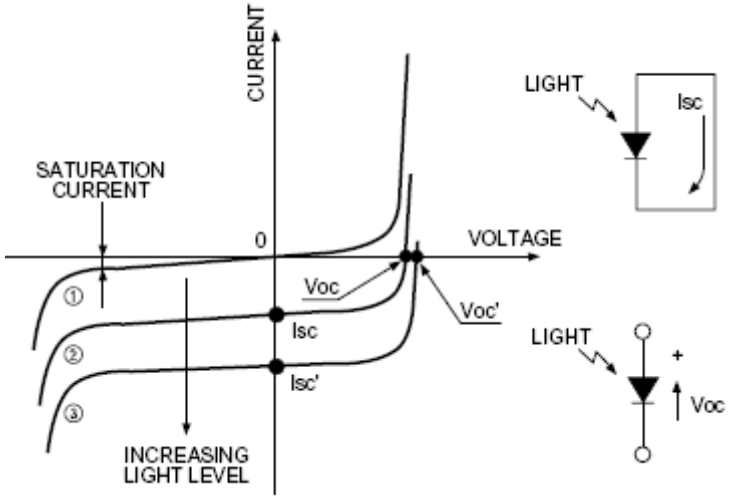
- Current mode
  - Measures the total current of the detector and ignores the pulse nature of the signal.
  - Does not allow advantage to be taken of the timing and amplitude information present in the signal.

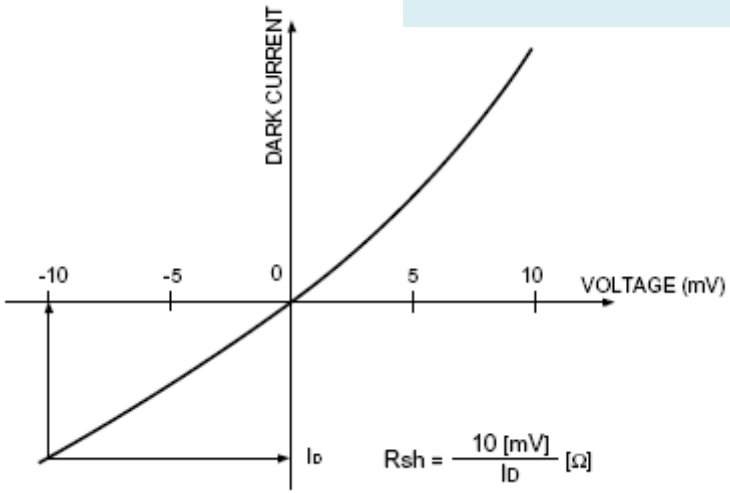
- Pulse mode.
  - Observes and counts the individual pulses generated by the particles.
  - Gives superior performance but cannot be used if the rate is too large.

Current mode

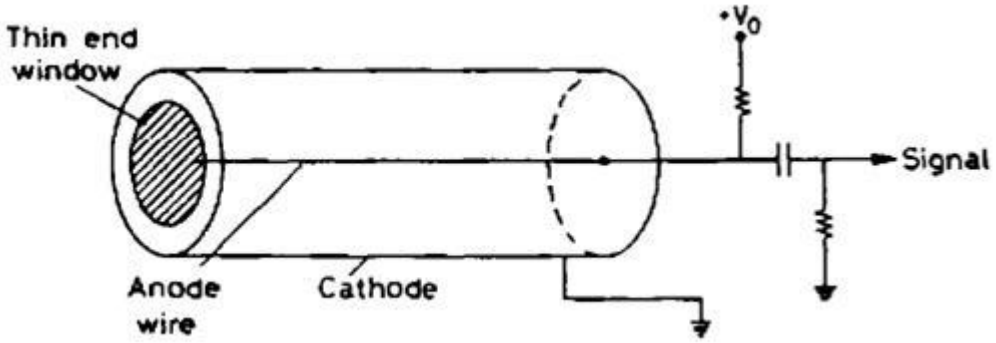


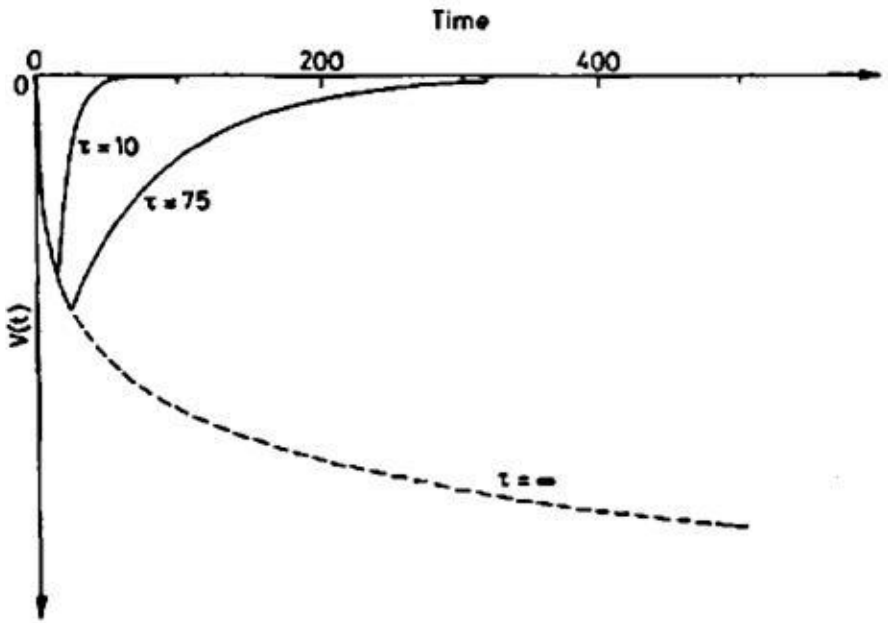
If we set the open loop gain of the operational amplifier as A, the characteristics of the feedback circuit allows the equivalent input resistance to be which is several orders of magnitude smaller than Rf. Thus this circuit enables ideal Isc measurement over a wide range.





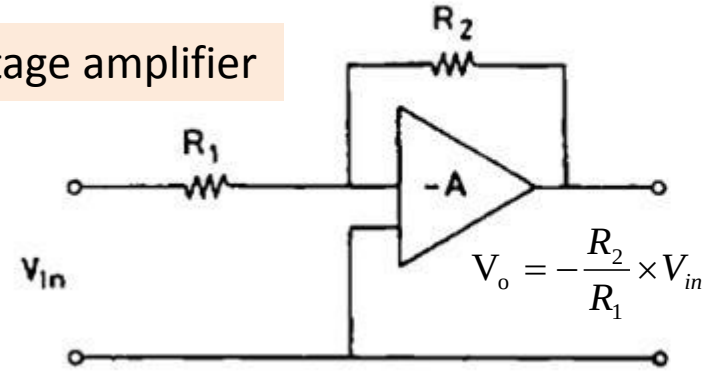
An example of pulse mode



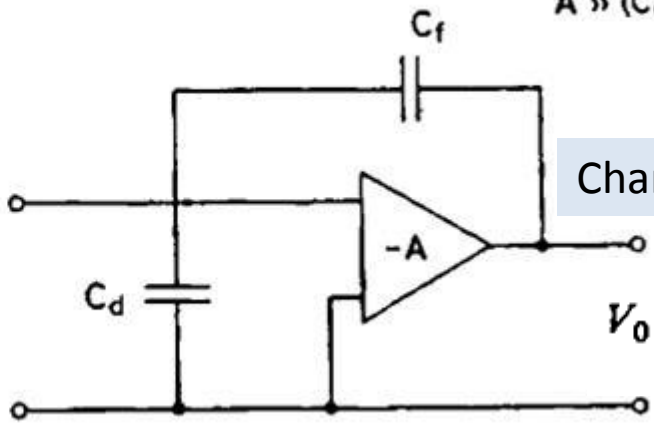


$A \gg (C_d + C_f)/C_f$

Voltage amplifier



$$V_o = -\frac{R_2}{R_1} \times V_{in}$$



Charge amplifier

$$V_0 \simeq -\frac{Q}{C_f}$$

Pulse mode

- Amplitude of the pulses is proportional to the initial charge signal and the arrival time of the pulse is some fixed time after the physical event.
- By using appropriate thresholds, one can select and count only those pulses that one wants to count.
- Often the 'good events' are characterised by
  - some specific signal amplitude
  - simultaneous presence of two (or more) signals in different detectors.
  - absence of some other signal.
- In the pulse mode, one can register a pulse height spectrum and such a spectrum contains a large amount of useful information.

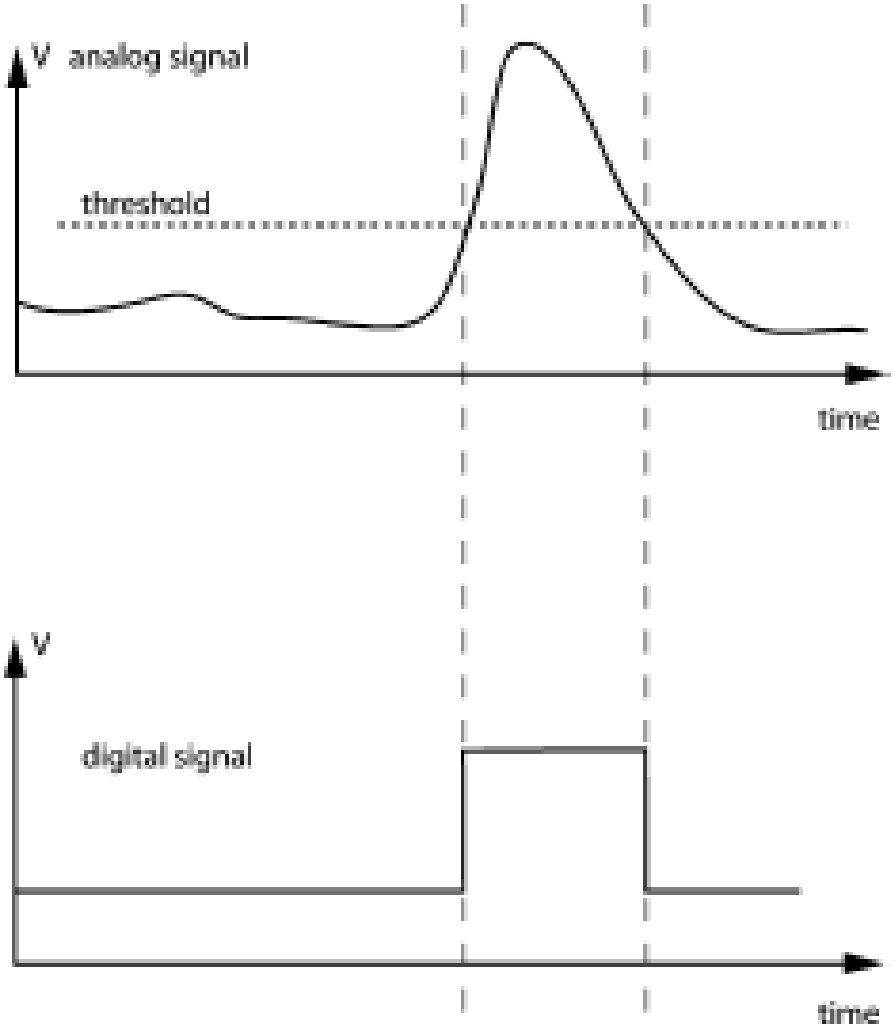
August 21, 2012

LECTURE-2

Pulse counting

A discrimination circuit has an analog input signal and a digital output signal. If the input signal exceeds some fixed threshold, a digital output signal is generated.

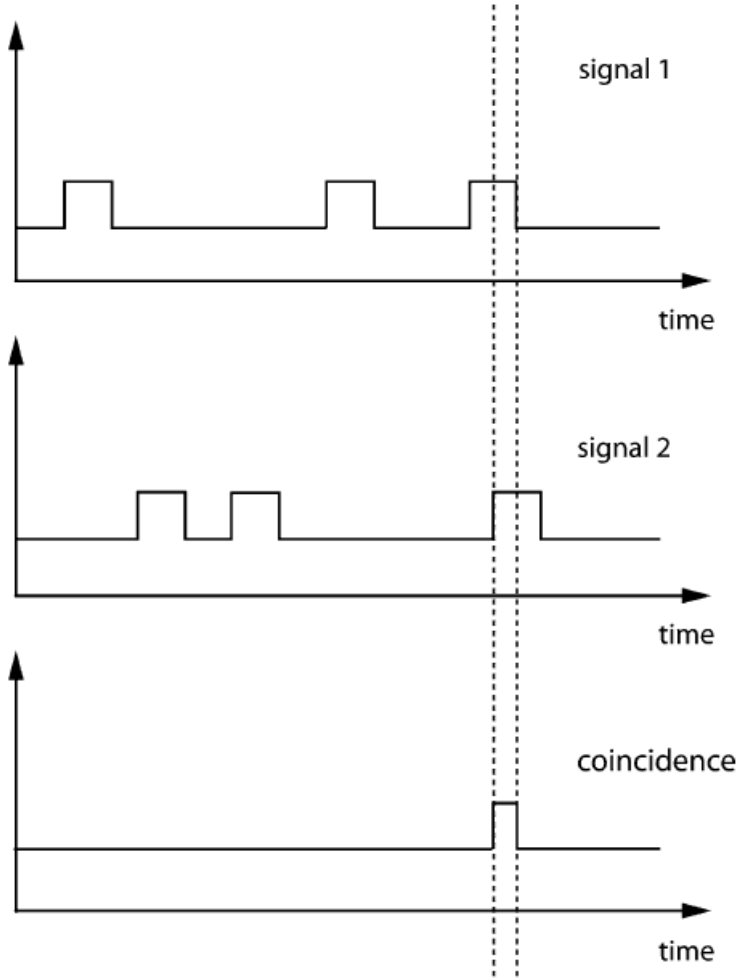
- In this process, the setup could be inefficient.
- Sometimes a real event in the detector does not produce a pulse that is large enough to produce a signal exceeding the threshold.
- Or a suitable signal was produced, but the electronics did not recognise the pulse because it was arriving at the same time as some other event.
- This last effect is referred to as dead time.



Coincidence of signals

- To see if an event occurred simultaneously with some other event, the electronics will look for the simultaneous presence of two logical signals within some time Window.
- In coincidence counting, one should be aware of the possibility to have random coincidences.
- These are occurrences of a coincidence caused by two unrelated events arriving by chance at the same time.
- The rate of random coincidences between two signals is proportional to the rate of each type of signal times the duration of the coincidence window.

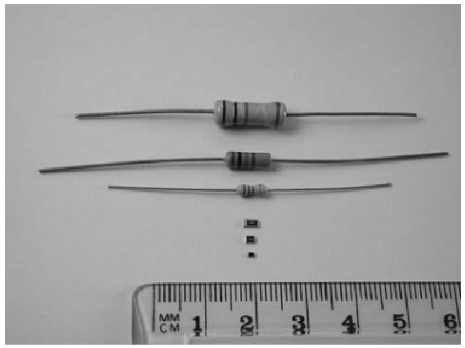
$$\frac{dN_{random}}{dt} = \frac{dN_1}{dt} \times \frac{dN_2}{dt} \times \Delta t$$

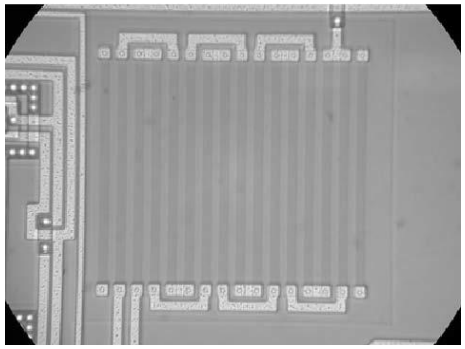


Triad of passive linear elements

- Resistors
- Capacitors
- Inductors

Resistors



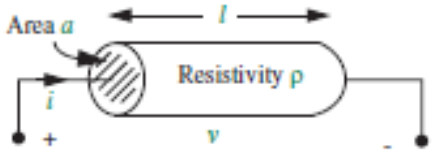


At the bottom, Silicon-chromium thin-film resistors, each with 6 µm width and 217.5 µm length, and nominal resistance 50 kΩ

Nichrome wire used in toasters and electric stoves and planar layers of poly-silicon in highly complex computer chips, to small rods of carbon particles encased in Bakelite commonly found in electronic equipment ...

Voltage measured across the terminals of a resistor is linearly proportional to the current flowing through the resistor. The constant of proportionality is called the *resistance*

$v = iR$ (Ohm's Law)



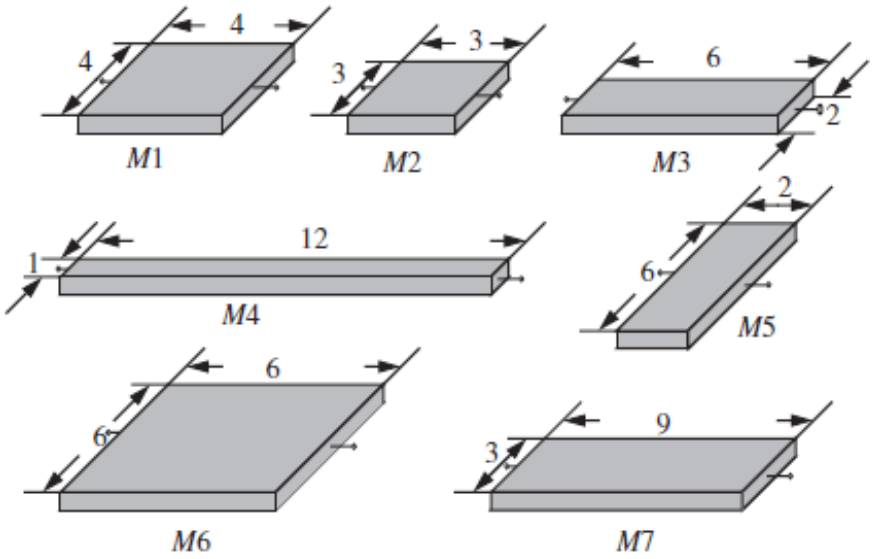
$$R = \frac{\rho l}{a}$$

Resistance of a cuboid shaped resistor with length *l, width w,* and height *h is given by* $R = \rho l/wh$

Resistivities of various materials

Material	ρ (Ω•m) at 20 °C	σ (S/m) at 20 °C	Temperature coefficient[note 1] (K^{-1})	Reference
Silver	1.59×10^{-8}	6.30×10^{7}	0.0038	[4][5]
Copper	1.68×10^{-8}	5.96×10^{7}	0.0039	[5]
Annealed copper[note 2]	1.72×10^{-8}	5.80×10^{7}		[*citation needed*]
Gold[note 3]	2.44×10^{-8}	4.10×10^{7}	0.0034	[4]
Aluminium[note 4]	2.82×10^{-8}	3.5×10^{7}	0.0039	[4]
Calcium	3.36×10^{-8}	2.98×10^{7}	0.0041	
Tungsten	5.60×10^{-8}	1.79×10^{7}	0.0045	[4]
Zinc	5.90×10^{-8}	1.69×10^{7}	0.0037	[6]
Nickel	6.99×10^{-8}	1.43×10^{7}	0.006	
Lithium	9.28×10^{-8}	1.08×10^{7}	0.006	
Iron	1.0×10^{-7}	1.00×10^{7}	0.005	[4]
Platinum	1.06×10^{-7}	9.43×10^{6}	0.00392	[4]
Tin	1.09×10^{-7}	9.17×10^{6}	0.0045	
Carbon steel (1010)	1.43×10^{-7}	6.99×10^{6}		[7]
Lead	2.2×10^{-7}	4.55×10^{6}	0.0039	[4]
Titanium	4.20×10^{-7}	2.38×10^{6}	X	
Grain oriented electrical steel	4.60×10^{-7}	2.17×10^{6}		[8]
Manganin	4.82×10^{-7}	2.07×10^{6}	0.000002	[9]
Constantan	4.9×10^{-7}	2.04×10^{6}	0.000008	[10]
Stainless steel[note 5]	6.9×10^{-7}	1.45×10^{6}		[11]
Mercury	9.8×10^{-7}	1.02×10^{6}	0.0009	[9]
Nichrome[note 6]	1.10×10^{-6}	9.09×10^{5}	0.0004	[4]
GaAs	5×10^{-7} to 10×10^{-3}	5×10^{-8} to 10^{3}		[12]
Carbon (amorphous)	5×10^{-4} to 8×10^{-4}	1.25 to 2×10^{3}	−0.0005	[4][13]
Carbon (graphite)[note 7]	$2.5e\times10^{-6}$ to 5.0×10^{-6} //basal plane 3.0×10^{-3} ⊥basal plane	2 to 3×10^{5} //basal plane 3.3×10^{2} ⊥basal plane		[14]
Carbon (diamond)[note 8]	1×10^{12}	$\sim10^{-13}$		[15]
Germanium[note 8]	4.6×10^{-1}	2.17	−0.048	[4][5]
Sea water[note 9]	2×10^{-1}	4.8		[16]
Drinking water[note 10]	2×10^{1} to 2×10^{3}	5×10^{-4} to 5×10^{-2}		[*citation needed*]
Silicon[note 8]	6.40×10^{2}	1.56×10^{-3}	−0.075	[4]
Deionized water[note 11]	1.8×10^{5}	5.5×10^{-6}		[17]
Glass	10×10^{10} to 10×10^{14}	10^{-11} to 10^{-15}	?	[4][5]
Hard rubber	1×10^{13}	10^{-14}	?	[4]
Sulfur	1×10^{15}	10^{-16}	?	[4]
Air	1.3×10^{16} to 3.3×10^{16}	3×10^{-15} to 8×10^{-15}		[18]
Paraffin	1×10^{17}	10^{-18}	?	
Fused quartz	7.5×10^{17}	1.3×10^{-18}	?	[4]
PET	10×10^{20}	10^{-21}	?	
Teflon	10×10^{22} to 10×10^{24}	10^{-25} to 10^{-23}	?	

Resistance of planar materials



Suppose resistance of a planar material of unit length and unit width, W is Ro, then

Ro = ρ1/H

Resistance of a cuboid shaped material with length L, width W, height H, and resistivity ρ is

R = ρL/WH

Substituting Ro = ρ/H, we get

R = Ro(L/W)

Because all square pieces made out of a given material have the same resistance (provided, of course, the pieces have the same thickness), we often characterize the resistivity of planar material of a given thickness with

$$R_{\square} = R_o, \tag{1.10}$$

where R_o is the resistance of a piece of the same material with unit length and width. Pronounced "R square," $R_{\square}$ is the resistance of a square piece of material.

Process shrinks

$$\frac{R_1}{R_2} = \frac{\rho L_1/(W_1 H)}{\rho L_2/(W_2 H)} = \frac{L_1/W_1}{L_2/W_2}.$$

Let the resistance values after the process shrink be R_1' and R_2'. Since each dimension shrinks by the fraction α, each new dimension will be α times the original value. Thus, for example, the length L_1 will change to αL_1. Using Equation 1.7, the ratio of the new resistance values is given by

$$\frac{R_1'}{R_2'} = \frac{\rho' \alpha L_1/(\alpha W_1 \alpha H)}{\rho' \alpha L_2/(\alpha W_2 \alpha H)} = \frac{L_1/W_1}{L_2/W_2}$$

In other words, the ratio of the resistance values is unchanged by the process shrink.

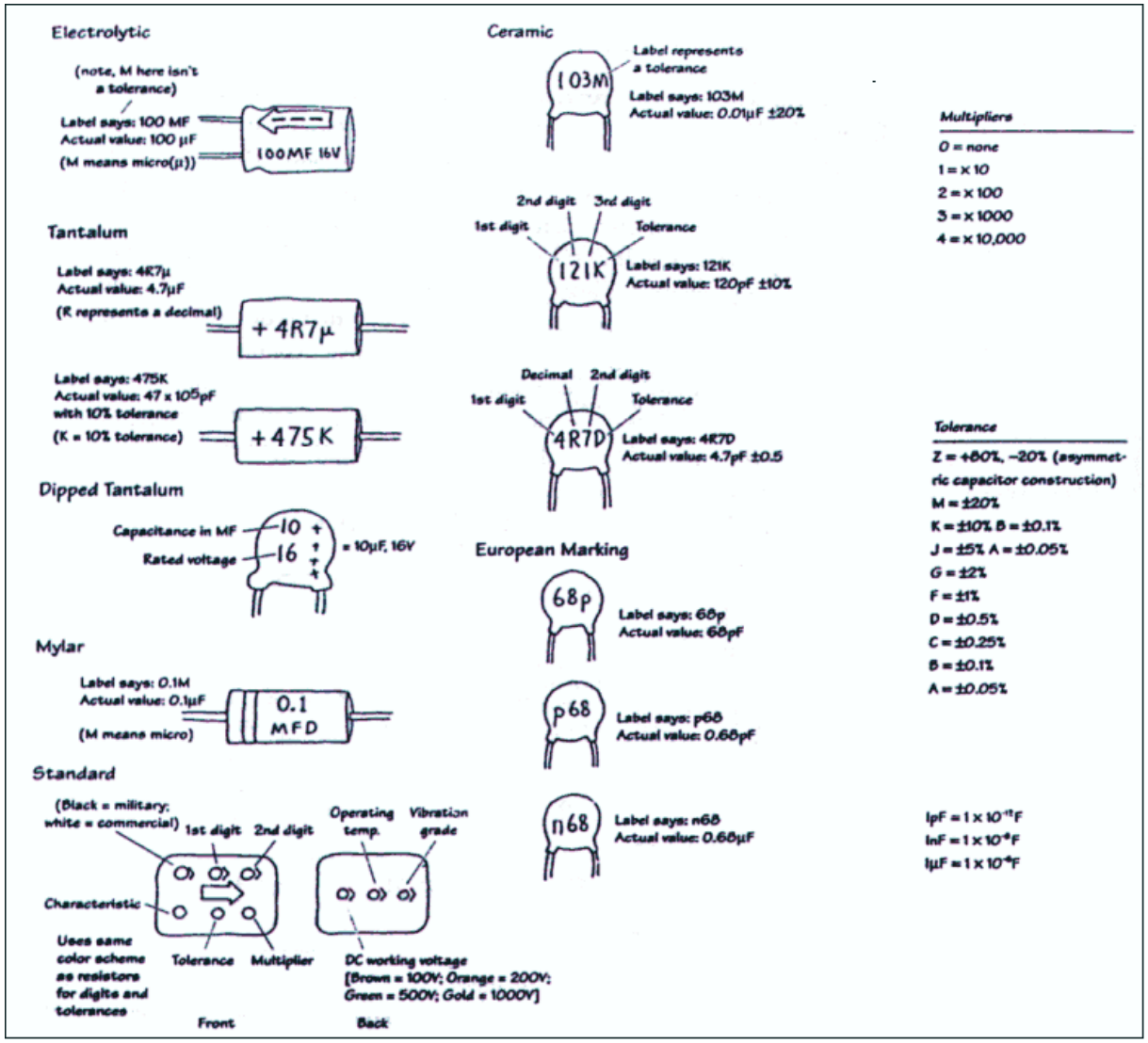
The ratio property of planar resistance — that is that the ratio of the resistances of rectangular pieces of material with a given thickness and resistivity is independent of the actual values of the length and the width provided the ratio of the length and the width is fixed — enables us to perform process shrinks (for example, from a 0.25-µm process to a 0.18-µm process) without needing to change the chip layout. Process shrinks are performed by scaling the dimensions of the chip and its components by the same factor, thereby resulting in a smaller chip. The chip is designed such that relevant

Please read Anant Agarwal

Capacitors

- Frequency dependent resistors
- Waveform generation, filtering, blocking and bypass
- Energy storage, resonant circuits
- Integrators and differentiators
- Capacitors can not dissipate power, Why?

Capacitors



$$Q = CV$$

$$I = C\frac{dV}{dt}$$

August 23, 2012

LECTURE-3

Inductors

- Along with capacitors used to built filters – separate desired signals from background.
- Capacitors, for practical reasons, are closer to ideal in their behavior than inductors. In addition, it is easier to place capacitors in integrated circuits, than it is to use inductors. Therefore, we see capacitors being used far more often than we see inductors being used.
- Still, there are some applications where inductors simply must be used. Transformers are a case in point.
- An inductor obeys the expression

$$v_L = L_X \frac{di_L}{dt}$$

where v_L is the voltage across the inductor, and i_L is the current through the inductor, and L_X is called the inductance.

Transformers

- Two closely coupled coils – primary and secondary
- Voltage multiplication proportional to the turns ratio of the transformer
- Current correspondingly reduced
- Transformers are quite efficient
- Two important functions
  - Change the ac line voltage to a useful value
  - Isolate the electronic device from actual power line
- Transformers for audio and RF (tuned transformers if only narrow range of frequencies present)
- Transformers for RF use special core materials for minimising code losses.

Impedance and reactance

Differentiators

A basic *CR* differentiator network is diagrammed in Fig. 16.9. From the circuit equations, the input voltage E_{in} and output voltage E_{out} are related by

$$E_{in} = \frac{Q}{C} + E_{out} \tag{16.3}$$

where Q represents the charge stored across the capacitor. Now, differentiating with respect to time,

$$\frac{dE_{in}}{dt} = \frac{1}{C}\frac{dQ}{dt} + \frac{dE_{out}}{dt} \tag{16.4}$$

$$\frac{dE_{in}}{dt} = \frac{1}{C}i + \frac{dE_{out}}{dt} \tag{16.5}$$

Noting that $E_{out} = iR$ and setting $RC = \tau$, we obtain

$$E_{out} + \tau\frac{dE_{out}}{dt} = \tau\frac{dE_{in}}{dt} \tag{16.6}$$

Now, if we make RC sufficiently small, we can neglect the second term on the left and

$$E_{out} \cong \tau\frac{dE_{in}}{dt} \tag{16.7}$$

Thus, in the limit of small time constant τ, the network acts to produce an output E_{out} that is proportional to the time derivative of the input waveform E_{in}—hence the name *differentiator.* In order to meet these conditions, the time constant should be small compared with the duration of the pulse to be differentiated.

In the opposite extreme of large time constant, the first term on the left of Eq. (16.6) can be neglected and we have

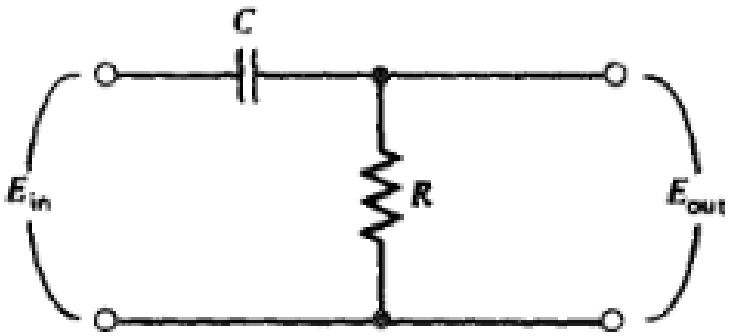
$$\tau\frac{dE_{out}}{dt} \cong \tau\frac{dE_{in}}{dt} \tag{16.8}$$

and setting the constant of integration equal to zero

$$E_{out} \cong E_{in} \tag{16.9}$$

Therefore, if the conditions for differentiation are not met, the network will tend to pass the waveform without alteration.

Differentiators are used for detecting leading edges and training edges in pulse circuits.



Make sure that R is “not too small”, thus loading the input

(a) *Sinusoidal* E_{in}
For

$$E_{in} = E_i \sin 2\pi ft \tag{16.10}$$

it can be shown that

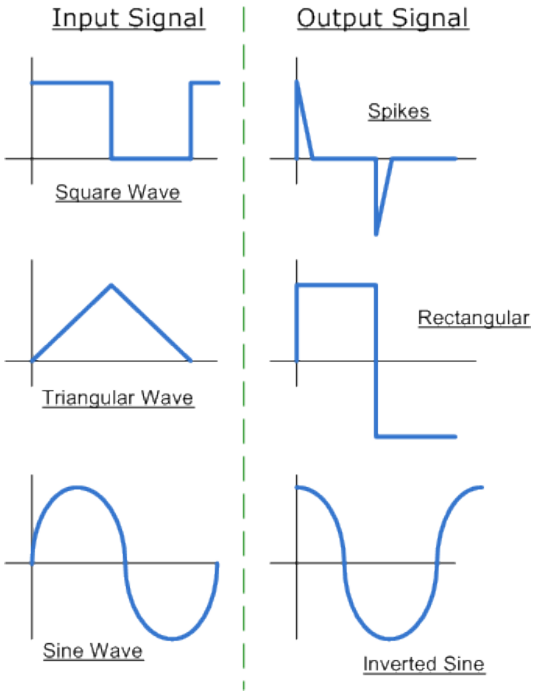
$$\frac{E_{out}}{E_i} = |A| \sin(2\pi ft + \theta) \tag{16.11}$$

where

$$|A| = \frac{1}{[1 + (f_1/f)^2]^{1/2}} \qquad \theta = \tan^{-1}\left(\frac{f_1}{f}\right)$$

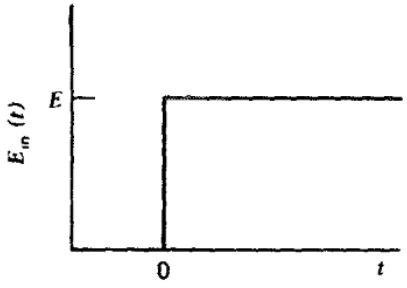
$$f_1 \equiv \frac{1}{2\pi\tau}$$

For high-frequency inputs, $f \gg f_1$, and $|A| \cong 1$. Hence, high frequencies are passed to the output with little attenuation, and we have a *high-pass filter.* Low frequencies are attenuated, because for $f \ll f_1$, $|A| \cong 0$. In the limit of $f = 0$ (constant voltage), no signal is transmitted and the network serves to block dc voltages because of the capacitor that is in series with the signal.



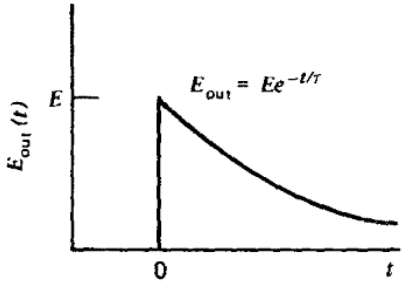
(b) *Step Voltage Input*
For

$$E_{in} = \begin{cases} E & (t \geq 0) \\ 0 & (t < 0) \end{cases}$$



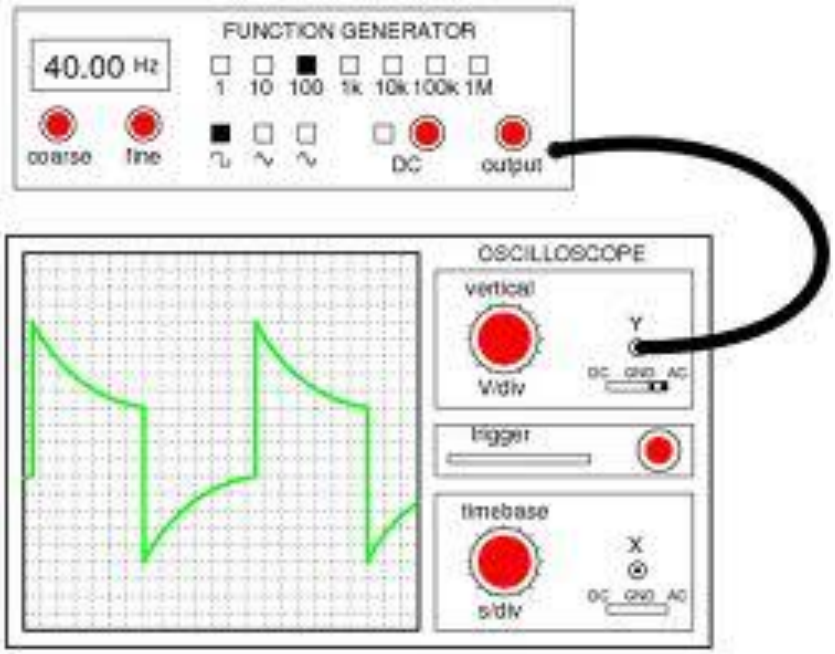
the output is

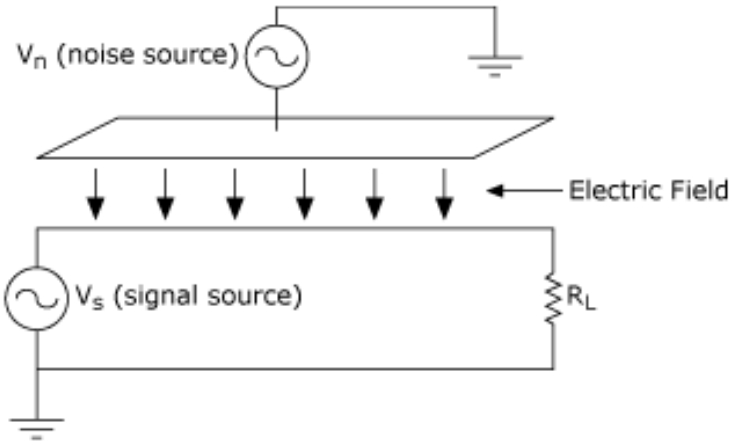
$$E_{out} = Ee^{-t/\tau}$$



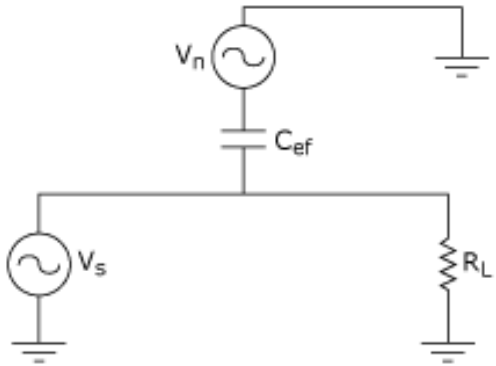
This case approximately represents the shaping of a fast-rising signal pulse with a long tail by a single *CR* differentiator. Note that the fast leading edge of the step is *not* differentiated because τ is not small compared with its rise time. The leading edge is therefore simply passed through, and the shaping consists of "differentiating away" the long tail. The amplitude E is not affected provided τ does not become small compared with the finite rise time of the actual signal pulse.

Unintentional capacitive coupling





a. Physical Representation



b. Equivalent Circuit

When configured as shown in Fig. 16.10, a passive RC network can also serve as an integrator. The circuit equation is now

$$E_{in} = iR + E_{out} \tag{16.13}$$

The current i also represents the rate of charging or discharging of the capacitor.

$$i = \frac{dQ}{dt} = C\frac{dV_c}{dt} \tag{16.14}$$

or

$$i = C\frac{dE_{out}}{dt} \tag{16.15}$$

Now combining Eqs. (16.13) and (16.15) and setting $RC = \tau$, we obtain

$$E_{in} = \tau\frac{dE_{out}}{dt} + E_{out} \tag{16.16}$$

Rearranging, we have

$$\frac{dE_{out}}{dt} + \frac{1}{\tau}E_{out} = \frac{1}{\tau}E_{in} \tag{16.17}$$

Now, if RC is sufficiently large, only the first term on the left is significant, and

$$\frac{dE_{out}}{dt} \cong \frac{1}{\tau}E_{in}$$

or

$$E_{out} \cong \frac{1}{\tau}\int E_{in}\,dt \tag{16.18}$$

Hence, the name *integrator*. The network will integrate provided the time constant τ is large compared with the time duration of the input pulse.

In the opposite extreme of small time constant only the second term on the left of Eq. (16.17) is significant, and therefore

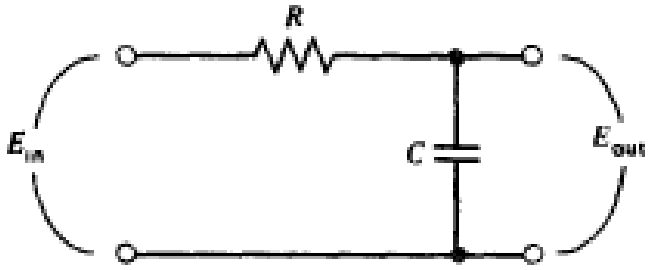
$$\frac{1}{\tau}E_{out} \cong \frac{1}{\tau}E_{in}$$

or

$$E_{out} \cong E_{in} \tag{16.19}$$

Thus, if the conditions for integration are not met, the network tends to pass the waveform without change.

Integrators



Integrators find use in analog computation, control systems, feedback, analog/digital conversion and waveform generation.

Again we apply Eq. (16.17) to some specific input waveforms.

(a) *Sinusoidal* E_{in}

For

$$E_{in} = E_i \sin 2\pi ft$$

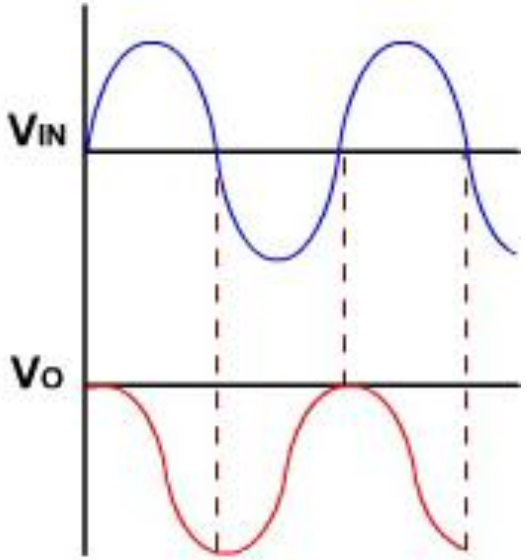
the solution is

$$\frac{E_{out}}{E_i} = |A| \sin(2\pi ft + \theta) \qquad (16.20)$$

where

$$|A| = \frac{1}{[1 + (f/f_2)^2]^{1/2}} \qquad \theta = -\tan^{-1}\left(\frac{f}{f_2}\right)$$

$$f_2 \equiv \frac{1}{2\pi\tau}$$



Again, we examine the extremes of frequency response. If

$$f \gg f_2, \quad \text{then} \quad |A| \cong 0$$

and if

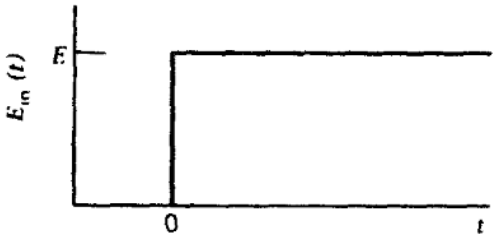
$$f \ll f_2, \quad \text{then} \quad |A| \cong 1$$

Therefore, the network blocks high frequencies, passes low frequencies without attenuation, and is thus a low-pass filter.

(b) *Step Voltage Input*

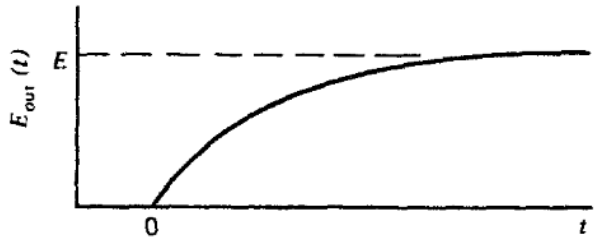
For

$$E_{in} = \begin{cases} E & (t \geq 0) \\ 0 & (t < 0) \end{cases}$$



the output is

$$E_{out} = E(1 - e^{-t/\tau})$$



This response is also plotted in Fig. 16.10. Recall that the circuit performs as an integrator in the limit of large τ. The mathematical integral of the step input should be a linearly increasing ramp. The actual response starts out as a linear ramp, but over a sufficiently long time scale the circuit time constant is no longer large by comparison, and the integration begins to fail. The output voltage then approaches the input step as a limit.

A simple application of integrator

September 3, 2012

LECTURE-4

Lab course

- RPC fabrication and characterisation
- Muon life time
- Atmospheric muon flux monitoring using RPC stack in C217

Devices in which a controlled flow of electrons can be obtained are the basic building blocks of all the electronic circuits.

Solid-state semiconductor electronics
(Since ~1930's)

- Some solid state semiconductors and their junctions offer the possibility of controlling the number and direction of flow of charge carriers through them.

- Simple excitations like light, heat or small applied voltage etc. can change the number of mobile charges in semiconductors.

- Supply and flow of charge carriers in the semiconductors are within the solid itself.

- Advantages: Small, low voltage, low power, long life, high reliability

Metals, semiconductors and insulators

- Current flow due to the applied field

$$\mathbf{j} = \mathbf{E}/\rho$$

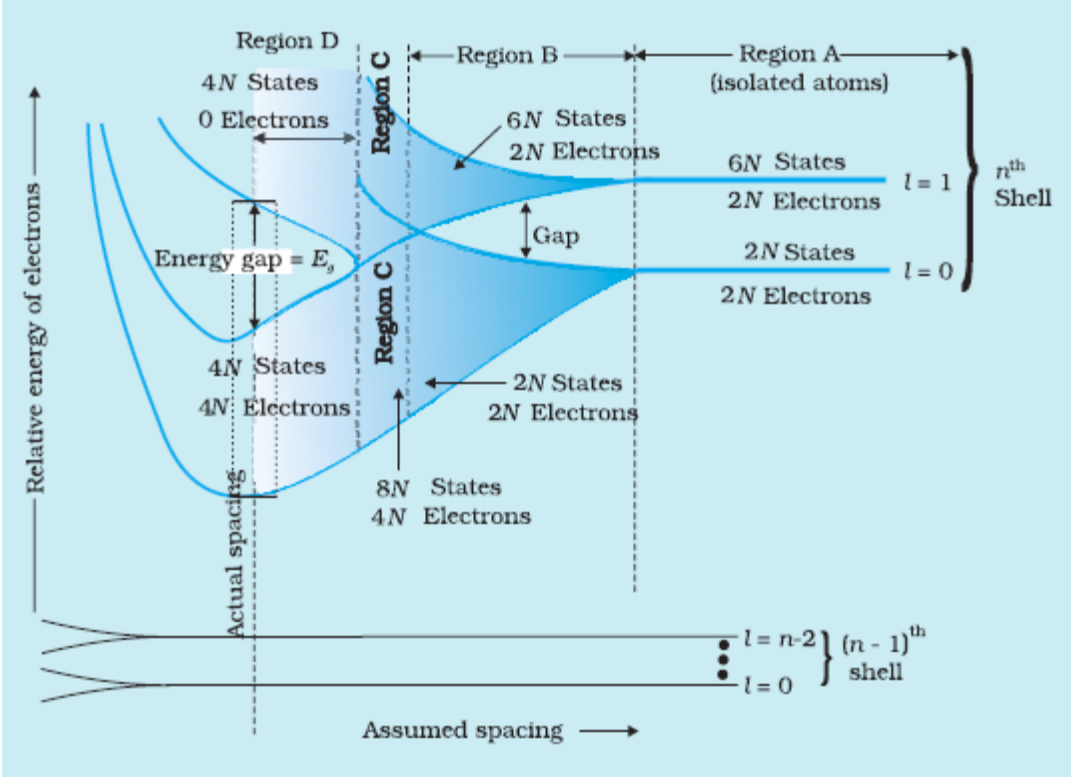
where **j** is the current density, **E** is the field applied and ρ is the resistivity.

Classification based on resistivity

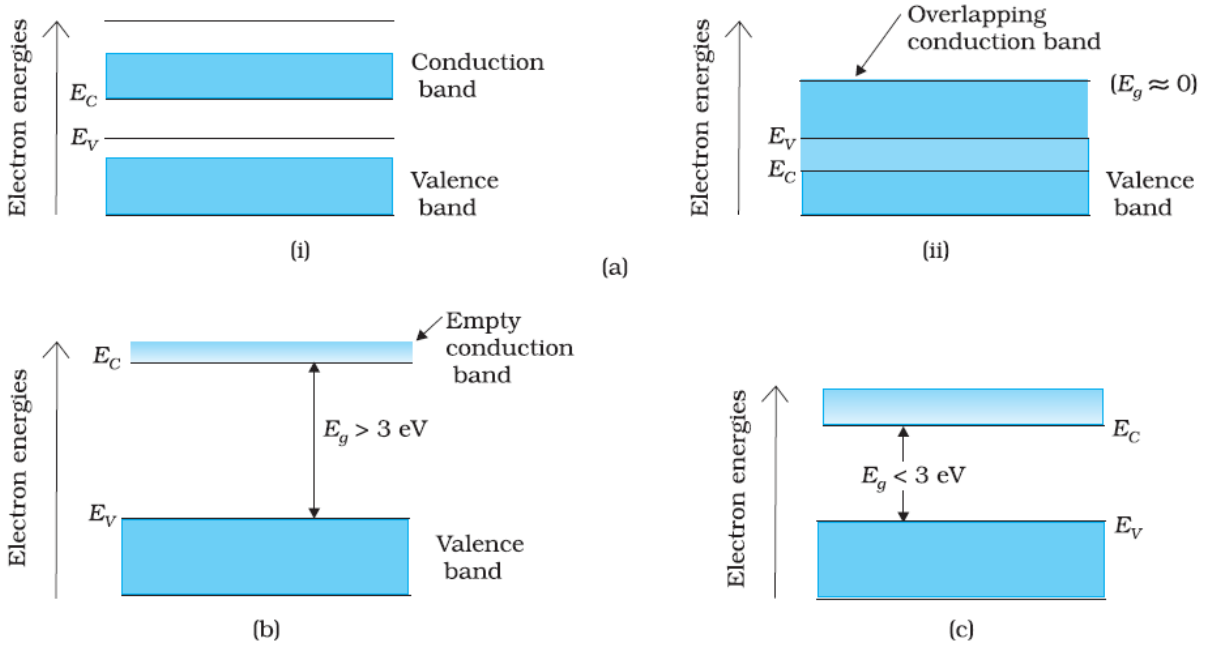
- Metals
  - $\rho = 10^{-2}$ to 10^{-8} Ω-m
  - ρ is fairly independent of **E**
  - $\rho \alpha T$
- Semiconductors
  - $\rho = 10^{-5}$ to 10^{6} Ω-m
  - $\rho \alpha 1/T$
- Insulators
  - $\rho = 10^{11}$ to 10^{19} Ω-m

Band gap theory

- Inside crystal each electron has different energy level; decided by the orbit in which it revolves
- Energy levels with continuous energy variation → Energy bands
- Valence energy band and conduction energy band
- The gap between top of valence band and bottom of conduction band is called the Energy gap E_g



Classification based on energy bands



- Conductors
  - Conduction band partially full and valence band is partially empty. Electrons from lower bands can move up
  - Conduction and valence bands overlap
- Insulators
  - E_g high (~6eV); No electrons in the conduction band
- Semiconductors
  - E_g low (~1eV); Electrons can acquire enough energy to cross from valence to conduction band

p-n junction

- A clear understanding of the junction behaviour is important to analyse the working of other semiconductor devices.

- How a junction is formed and how the junction behaves under the influence of external applied voltage (also called *bias*).

How does a p-n junction formed?

- By adding precisely a small quantity of impurity, part of the p-Si wafer can be converted into n-Si. The wafer now contains p-region and n-region and a metallurgical junction between p-, and n- regions.

- Two important processes occur during the formation of a p-n junction: *diffusion* and *drift*.

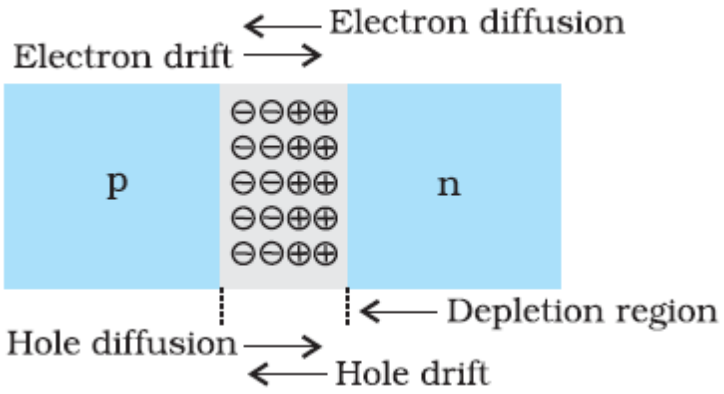
- Due to the concentration gradient across p-, and n- sides, holes diffuse from p-side to n-side (p → n) and electrons diffuse from n-side to p-side (n → p). This motion of charge carries gives rise to *diffusion current* across the junction.

- As the electrons continue to diffuse from n → p, a layer of positive charge (or positive space-charge region) on n-side of the junction is developed. Similarly negative charge is developed on p-side.

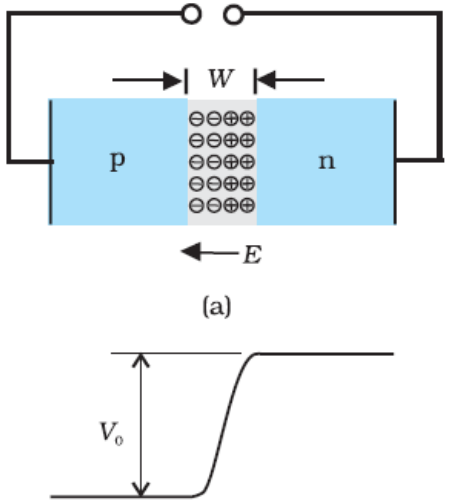
- This space-charge region on either side of the junction together is known as *depletion region*. The thickness of depletion region is of the order of one-tenth of a micron.

- An electric field directed from positive charge towards negative charge develops. Due to this field, an electron on p-side of the junction moves to n-side and a hole on n-side of the junction moves to p-side. The motion of charge carriers due to the electric field is called drift. Thus a *drift current*, which is opposite in direction to the diffusion current starts.

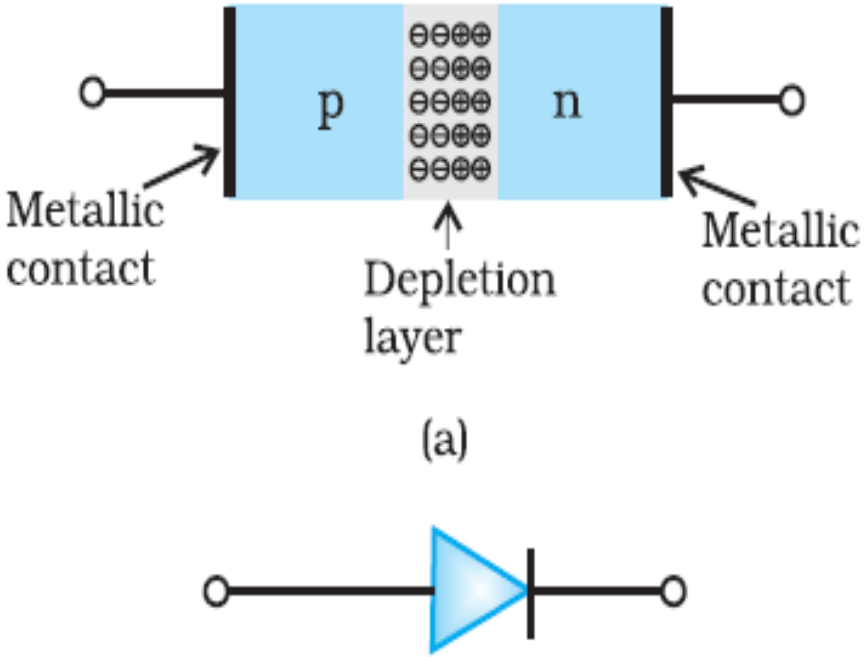
❖Initially, diffusion current is large and drift current is small. As the diffusion process continues, the space-charge regions on either side of the junction extend, thus increasing the electric field strength and hence drift current. This process continues until the diffusion current equals the drift current. Thus a p-n junction is formed. In a p-n junction under equilibrium there is *no net* current.



❖ The loss of electrons from the n-region and the gain of electrons by the p-region cause a difference of potential across the junction of the two regions. The polarity of this potential is such as to oppose further flow of carriers so that a condition of equilibrium exists. Since this potential tends to prevent the movement of electron from the n region into the p region, it is often called a *barrier potential*.

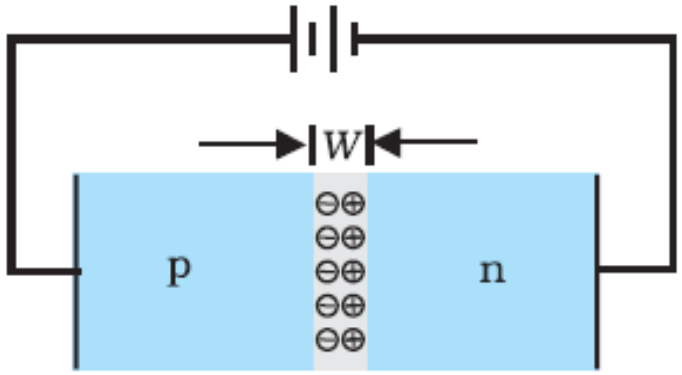


Semiconductor diode

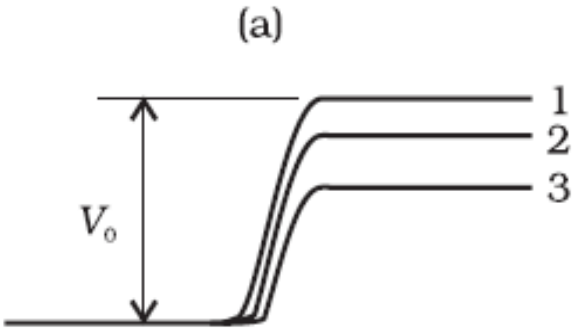


Forward bias

- The applied voltage mostly drops across the depletion region and the voltage drop across the p-side and n-side of the junction is negligible.



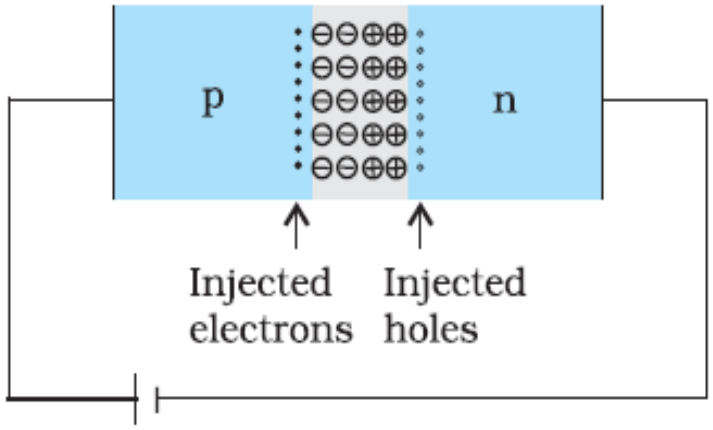
- The direction of the applied voltage (V) is opposite to the built-in potential V_0. The effective barrier height under forward bias is (V_0–V). Current through the diode increases with applied voltage.



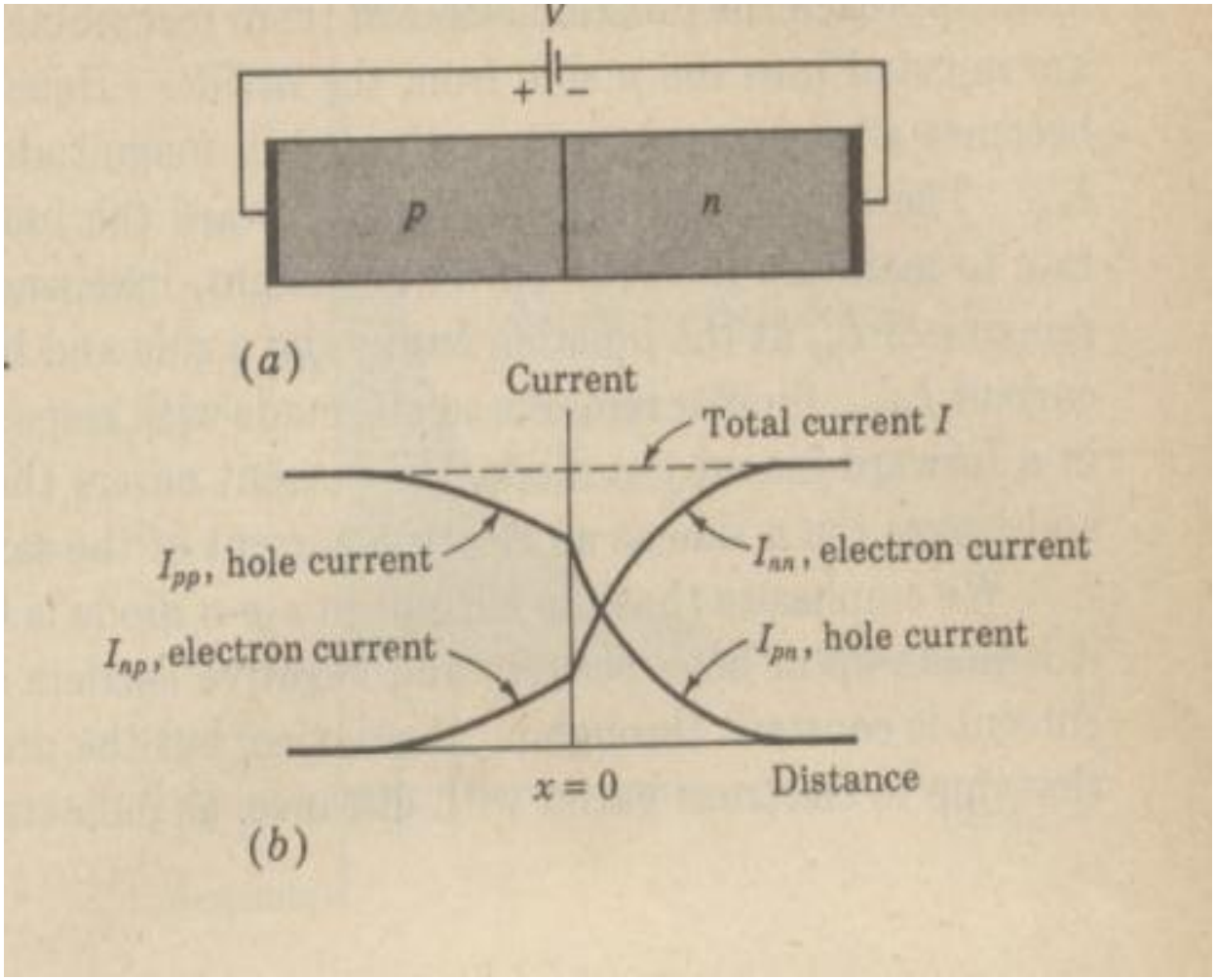
❖Due to the applied voltage, electrons from n-side cross the depletion region and reach p-side (where they are minority carries). Similarly, holes from p-side cross the junction and reach the n-side (where they are minority carries). This process under forward bias is known as *minority carrier injection.*

❖At the junction boundary, on each side, the minority carrier concentration increases significantly compared to the locations far from the junction. Due to this concentration gradient, the injected electrons on p-side diffuse from the junction edge of p-side to the other end of p-side. Likewise, the injected holes on n-side diffuse from the junction edge of n-side to the other end of n-side. This motion of charged carriers on either side gives rise to current.

❖The total diode forward current is sum of hole diffusion current and conventional current due to electron diffusion. The magnitude of this current is usually in mA.



Current components in a p-n diode

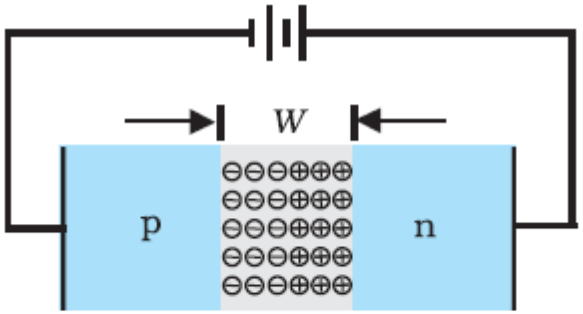


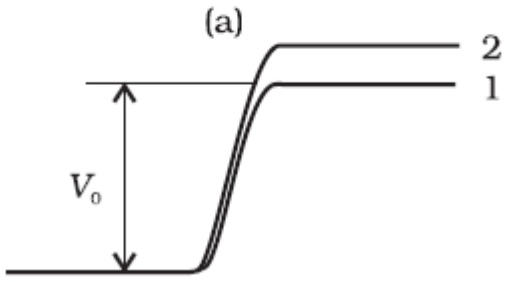
Reverse bias

- The applied voltage mostly drops across the depletion region. The direction of applied voltage is same as the direction of barrier potential.

- As a result, the barrier height increases and the depletion region widens due to the change in the electric field. The effective barrier height under reverse bias is ($V_0 + V$).

- This suppresses the flow of electrons from n→ p and holes from p→ n. Thus, diffusion current, decreases enormously compared to the diode under forward bias.





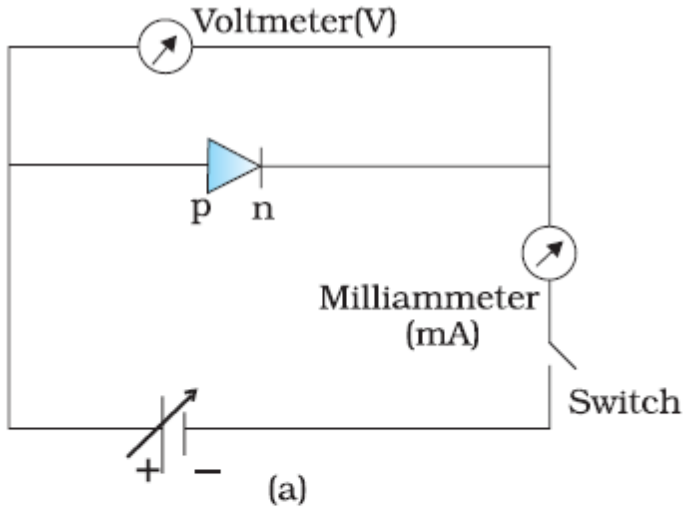
- The electric field direction of the junction is such that if electrons on p-side or holes on n-side in their random motion come close to the junction, they will be swept to its majority zone. This drift of carriers gives rise to current. The drift current is of the order of a few μA. This is quite low because it is due to the motion of carriers from their minority side to their majority side across the junction. The drift current is also there under forward bias but it is negligible (μA) when compared with current due to injected carriers which is usually in mA.

- The diode reverse current is not very much dependent on the applied voltage. Even a small voltage is sufficient to sweep the minority carriers from one side of the junction to the other side of the junction. The current is not limited by the magnitude of the applied voltage but is limited due to the concentration of the minority carrier on either side of the junction.

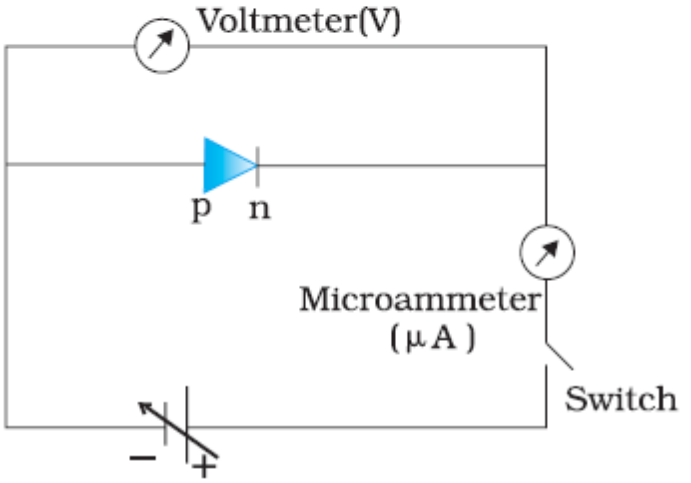
- The current under reverse bias is essentially voltage independent upto a critical reverse bias voltage, known as breakdown voltage (V_{br}). When $V = V_{br}$, the diode reverse current increases sharply. Even a slight increase in the bias voltage causes large change in the current. If the reverse current is not limited by an external circuit below the rated value (specified by the manufacturer) the p-n junction will get destroyed due to overheating. This can happen even for the diode under forward bias, if the forward current exceeds the rated value.

V-I characteristics of a diode

- In forward bias measurement, we use a milli-ammeter since the expected current is large while a micro-ammeter is used in reverse bias to measure the current.



(a)



(b)

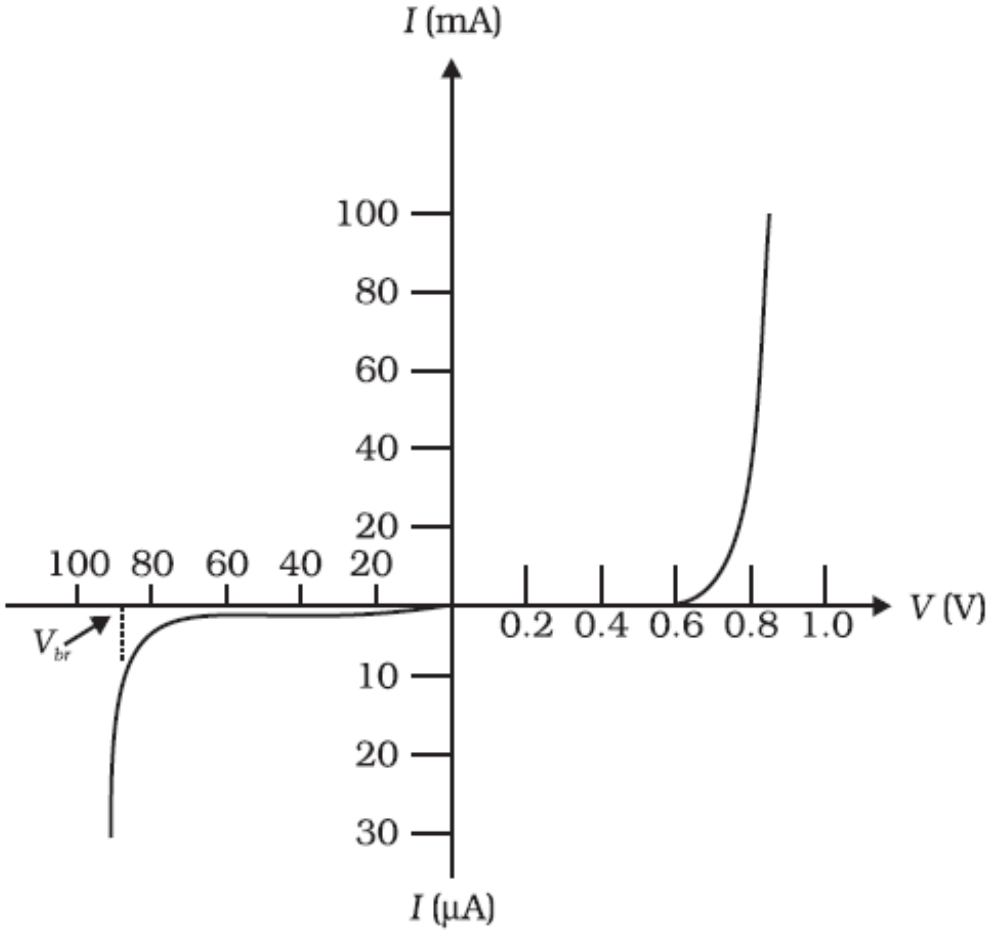
$$I = I_0\left(\epsilon^{\frac{V}{\eta V_T}} - 1\right)$$

I_0 is the saturation current, V_T is the thermal voltage, η is the *ideality factor*, also known as the *quality factor* or sometimes *emission coefficient* (1 for Ge and 2 for Si)), I = Diode current, V is the voltage across the diode

$$V_T = \frac{T}{11{,}600}$$ (26mV at room temperature)

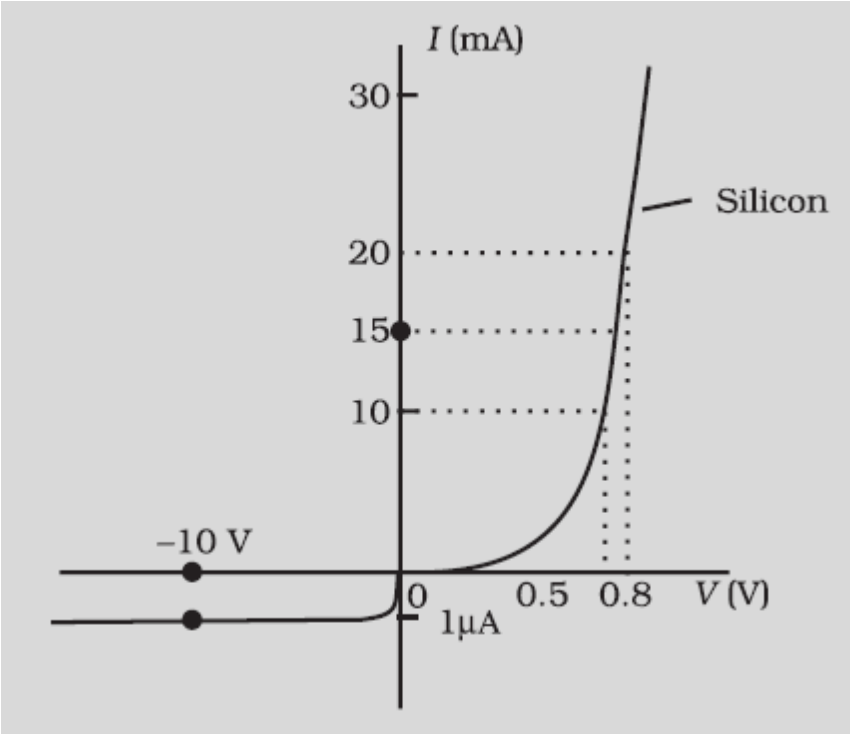
Threshold voltage or cut-in voltage (~0.2V for germanium diode and ~0.7 V for silicon diode).

For the diode in reverse bias, the current is very small (~µA) and almost remains constant with change in bias. It is called *reverse saturation current (I_0)*. However, for special cases, at very high reverse bias (break down voltage), the current suddenly increases. The general purpose diodes are not used beyond the reverse saturation current region.



Dynamic resistance of a diode

- p-n junction diode primarily allows the flow of current only in one direction (forward bias). The forward bias resistance is low as compared to the reverse bias resistance. This property is used for rectification of ac voltages.

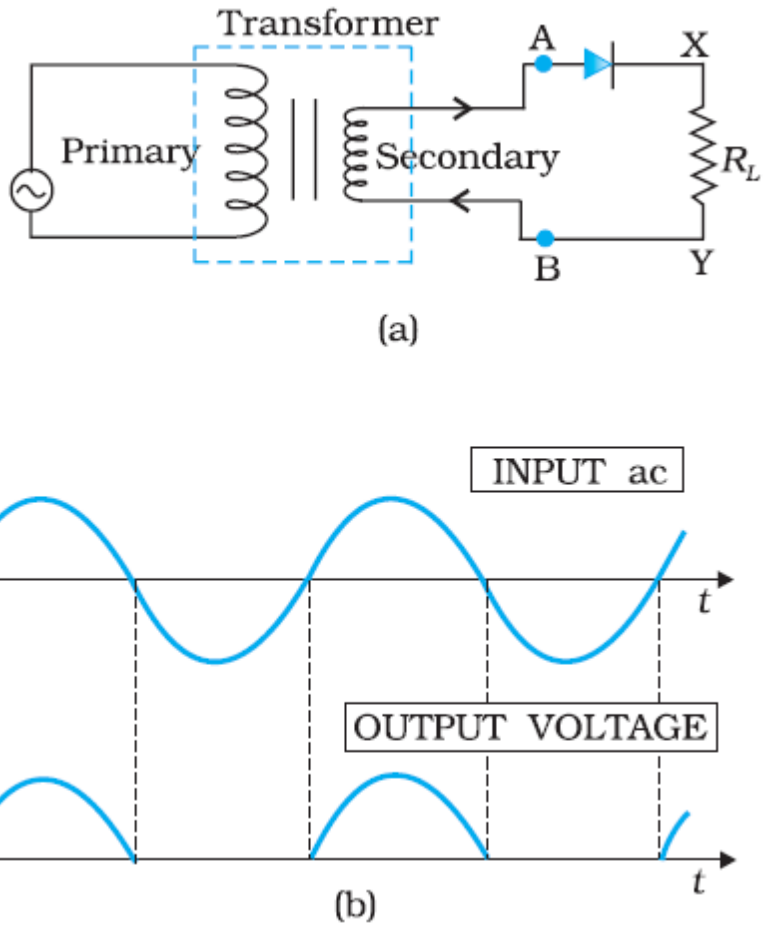


Dynamic resistance of a diode = $\frac{\text{Small change in voltage}}{\text{Small change in current}}$

Diode as a rectifier

- The reverse saturation current of a diode is negligible and can be considered equal to zero for practical purposes.

- The reverse breakdown voltage of the diode must be sufficiently higher than the peak ac voltage at the secondary of the transformer to protect the diode from reverse breakdown.



Parameters for HWR

Input sinusoidal waveform → Average value = 0

We will idealise of diode characteristics.

$v_i = V_m \sin\omega t$

$i = I_m \text{Sin}\omega t$ where $0 \le \omega t \le \pi$

$i = 0$ where $\pi \le \omega t \le 2\pi$

$I_m = V_m / (R_f + R_L)$

$I_{dc} = I_m / \pi$

$I_{rms} = I_m / 2$

$V_{dc} = -I_m * R_L / \pi$

Peak inverse voltage = Peak transformer secondary voltage

% regulation = $100 * (V_{\text{no load}} - V_{\text{full load}}) / V_{\text{full load}}$

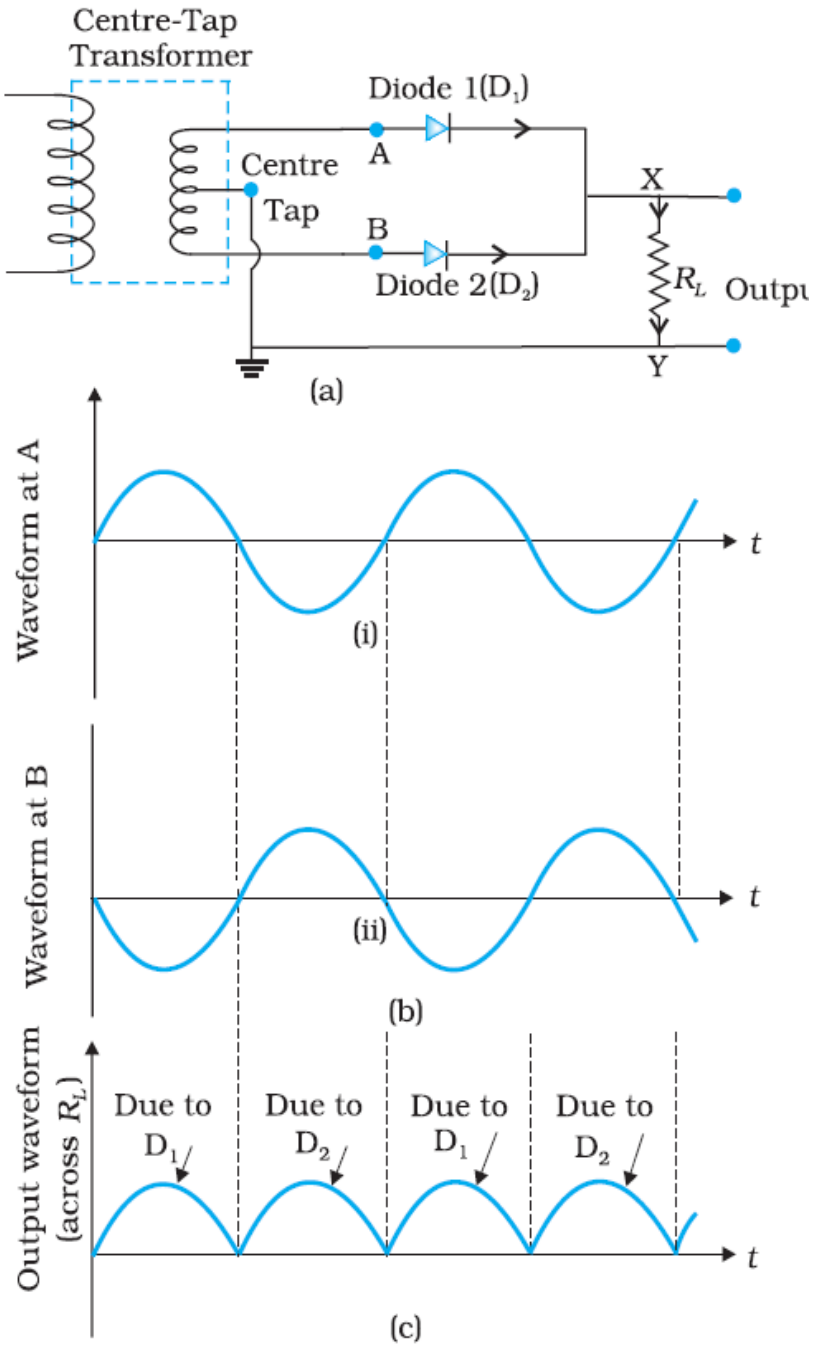
$V_{dc} = V_m / \pi - I_{dc} * R_f$

Ripple factor = rms value /average value

$r = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = 1.21$

Full-wave rectifier

- For a full-wave rectifier the secondary of the transformer is provided with a centre tapping and so it is called *centre-tap transformer*.



Parameters for FWR

$I_{dc} = 2I_m / \pi$

$I_{rms} = \frac{I_m}{\sqrt{2}}$

$V_{dc} = -I_m * R_L / \pi$

Peak inverse voltage = 2 * Max transformer voltage

% regulation = $100 * (V_{no\ load} - V_{full\ load}) / V_{full\ load}$

$V_{dc} = 2V_m / \pi - I_{dc} * R_f$

Ripple factor = rms value /average value

$r = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = 0.482$

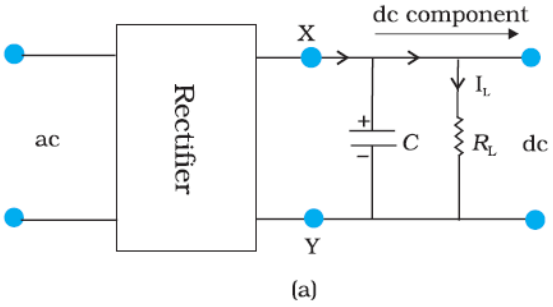
Filters

- The rectified voltage is in the form of pulses of the shape of half sinusoids. Though it is unidirectional it does not have a steady value.

- To get steady dc output from the pulsating voltage normally a capacitor is connected across the output terminals (parallel to the load R_L). Since these additional circuits appear to *filter* out the *ac ripple* and give a *pure dc* voltage, so they are called filters.

- When the voltage across the capacitor is rising, it gets charged. If there is no external load, it remains charged to the peak voltage of the rectified output. When there is a load, it gets discharged through the load and the voltage across it begins to fall. In the next half-cycle of rectified output it again gets charged to the peak value.

- The rate of fall of the voltage across the capacitor depends upon the *time constant* ($1/R_LC$).



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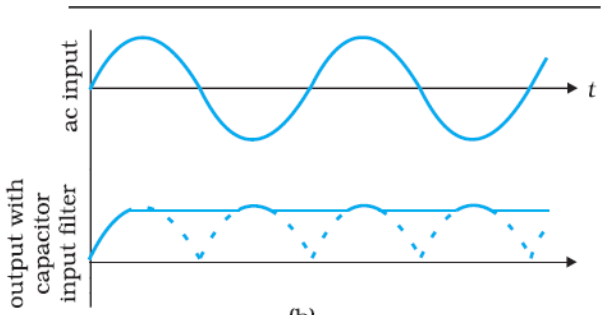
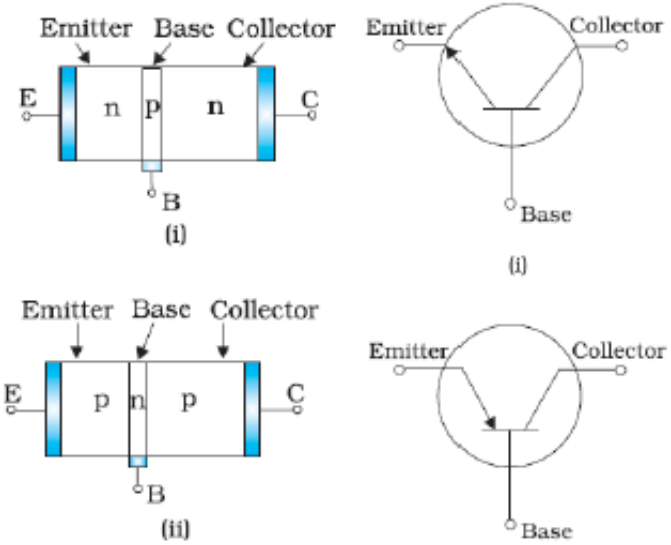


(b)

September 6, 2012

LECTURE-5

Transistors



All the three segments of a transistor have different thickness and their doping levels are also different.
Arrowhead shows the direction of conventional current in the transistor.

- *Emitter*: Moderate size and heavily doped. Supplies a large number of majority carriers for the current flow through the transistor.
- *Base*: Very thin and lightly doped.
- *Collector*: Collects a major portion of the majority carriers supplied by the emitter. Moderately doped and larger in size as compared to the emitter.

Transistor configurations

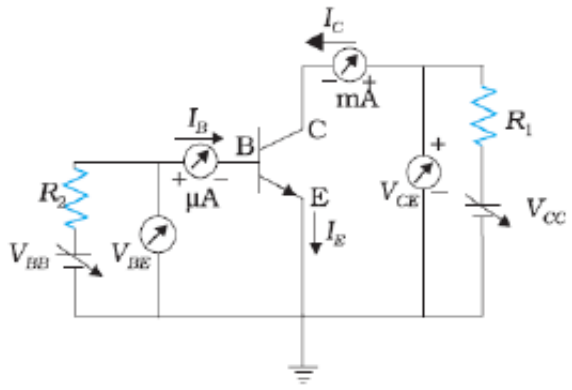
- In a transistor, only three terminals are available, viz., *Emitter* (E), *Base* (B) and *Collector* (C).

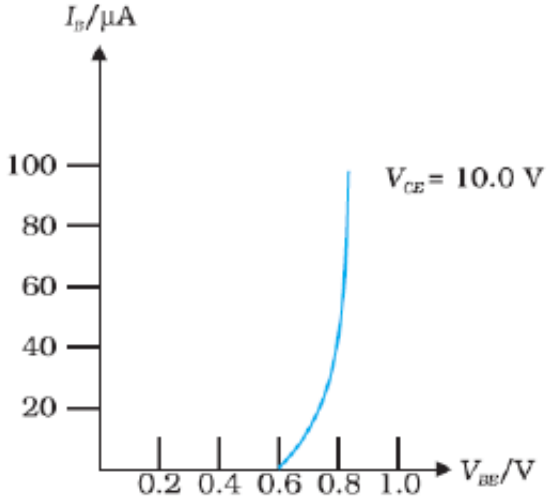
- Therefore, in a circuit the input/output connections have to be such that one of these (E, B or C) is common to both the input and the output.

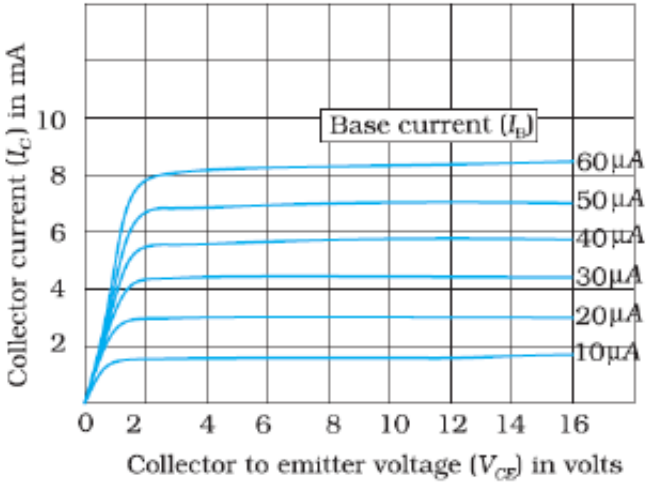
- Accordingly, the transistor can be *connected* in any of the following three configurations:

    1. *Common Emitter (CE)*
    2. *Common Base (CB)*
    3. *Common Collector (CC)*

CE transistor characteristics

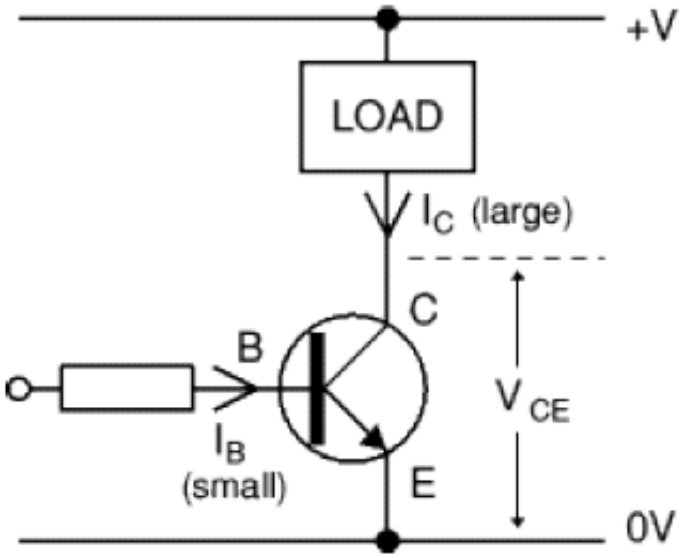






$$r_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE}} \qquad r_o = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B} \qquad \beta_{ac} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}}$$

Transistor as a switch



- When a transistor is used as a switch it must be either **OFF** or **fully ON**.
- In the fully ON state the voltage V_{CE} across the transistor is almost zero and the transistor is said to be **saturated** because it cannot pass any more collector current Ic.
- The output device switched by the transistor is usually called the 'load'.

The power developed in a switching transistor is very small:

- In the **OFF** state: power = Ic × V_{CE}, but Ic = 0, so the power is zero.
- In the **full ON** state: power = Ic × V_{CE}, but V_{CE} = 0 (almost), so the power is very small.

This means that the transistor should not become hot in use and you do not need to consider its maximum power rating.

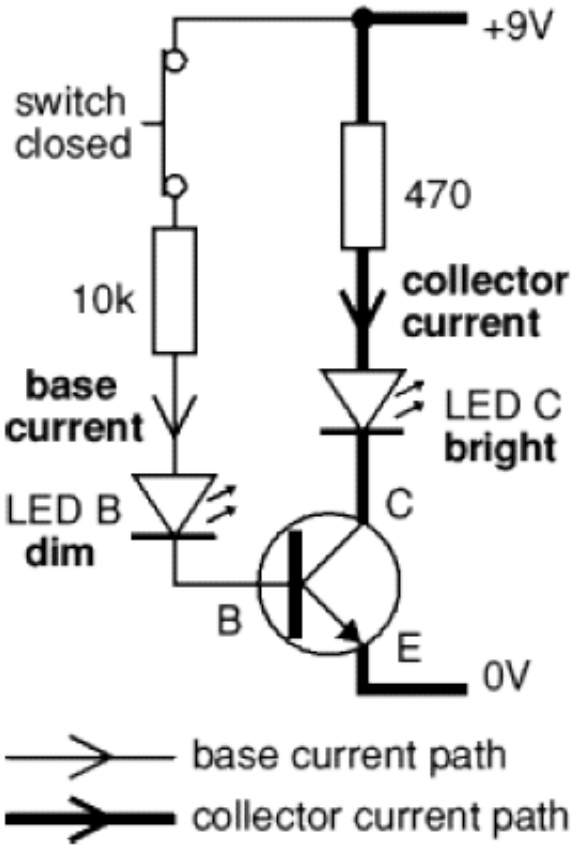
Transistor currents

The diagram shows the two current paths through a transistor.

The small **base current** controls the larger **collector current**.

When the switch is closed a small current flows into the base (B) of the transistor. It is just enough to make LED B glow dimly. The transistor amplifies this small current to allow a larger current to flow through from its collector (C) to its emitter (E). This collector current is large enough to make LED C light brightly.

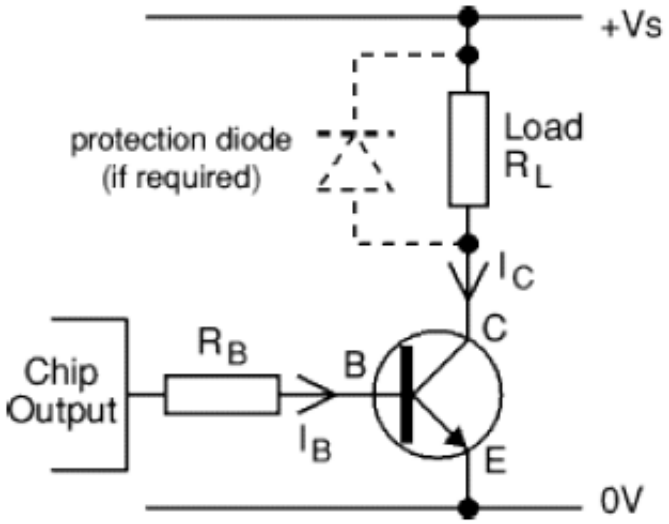
When the switch is open no base current flows, so the transistor switches off the collector current. Both LEDs are off.



A transistor amplifies current and can be used as a switch.

This arrangement where the emitter (E) is in the controlling circuit (base current) and in the controlled circuit (collector current) is called **common emitter mode**. It is the most widely used arrangement for transistors.

Designing a NPN transistor switch



1. Load is ON when IC output is HIGH.
2. The transistor's maximum collector current I_c(max) must be greater than the load current I_c.

   Load current $_{Ic}$ = Supply voltage($_{Vs}$) / Load resistance($_{RL}$)

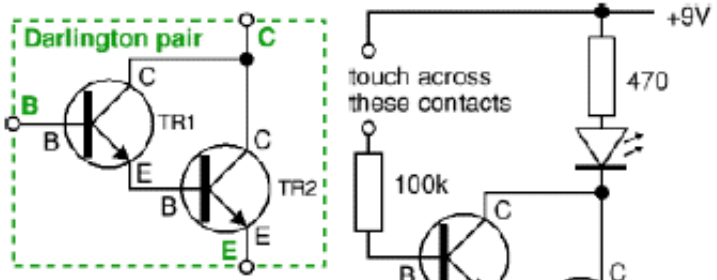
3. The transistor's minimum current gain h_{FE}(min) must be at least five times the load current I_c divided by the maximum output current from the IC.

$_{hFE}$(min) > 5 * Load current($_{Ic}$)/ maximum IC current

4. A resistor R_B is required to limit the current flowing into the base of the transistor and prevent it being damaged. However, R_B must be sufficiently low to ensure that the transistor is thoroughly saturated to prevent it overheating, this is particularly important if the transistor is switching a large current (> 100mA). A safe rule is to make the base current I_B about five times larger than the value which should just saturate the transistor.

   $R_B = V_c * h_{FE} / (5 * I_c)$, where V_c is the IC supply voltage

Darlington pair

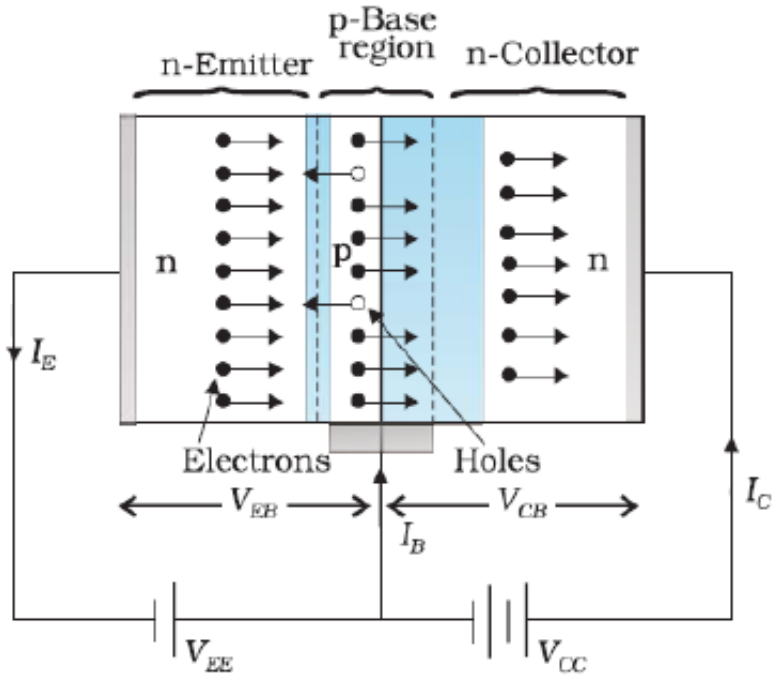


Darlington pair current gain, $h_{FE} = h_{FE1} \times h_{FE2}$
(h_{FE1} and h_{FE2} are the gains of the individual transistors)

Only a tiny base current is required to make the pair switch on.

A Darlington pair behaves like a single transistor with a very high current gain. It has three leads (**B**, **C** and **E**) which are equivalent to the leads of a standard individual transistor. To turn on there must be 0.7V across both the base-emitter junctions, which are connected in series inside the Darlington pair, therefore it requires 1.4V to turn on.

A Darlington pair is sufficiently sensitive to respond to the small current passed by your skin and it can be used to make a **touch-switch**. The 100kΩ resistor protects the transistors if the contacts are linked with a piece of wire.



Transistor as amplifier

The heavily doped emitter has a high concentration of majority carriers, which will be electrons in an n-p-n transistor. These majority carriers enter the base region in large numbers.

The base is thin and lightly doped. So the majority carriers there would be few. In a n-p-n transistor the majority carriers in the base are holes since base is of p-type semiconductor.

The large number of electrons entering the base from the emitter swamps the small number of holes there. As the base collector-junction is reverse biased, these electrons, which appear as minority carriers at the junction, can easily cross the junction and enter the collector.

The electrons in the base could move either towards the base terminal to combine with the holes entering from outside or cross the junction to enter into the collector and reach the collector terminal.

The base is made thin so that most of the electrons find themselves near the reverse-biased base-collector junction and so cross the junction instead of moving to the base terminal.

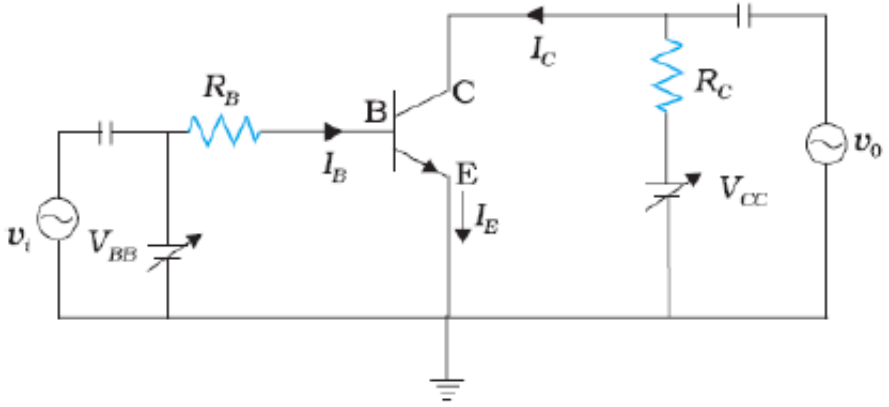
If we represent the hole current and the electron current crossing the forward biased junction by I_h and I_e respectively then the total current in a forward biased diode is the sum $I_h + I_e$.

We see that the emitter current $I_E = I_h + I_e$ but the base current $I_B << I_h + I_e$.

The current entering into the emitter from outside is equal to the emitter current I_E. Similarly the current emerging from the base terminal is I_B and that from collector terminal is I_C.

$$I_E = I_C + I_B, \text{ or } I_C \cong I_E$$

CE transistor amplifier



Biasing of the transistor:

- Fix its operating point somewhere in the middle of its active region.
- We fix the value of V_{BB} corresponding to a point in the middle of the linear part of the transfer curve.
- Then the dc base current I_B would be constant and corresponding collector current I_C will also be constant.
- The dc voltage $V_{CE} = V_{CC} - I_C R_C$ would also remain constant.
- The operating values of V_{CE} and I_B determine the operating point of the amplifier.

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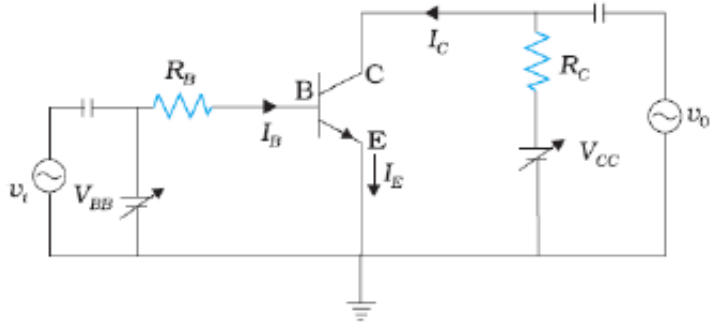
- If a small sinusoidal voltage with amplitude v_s is superposed on the dc base bias by connecting the source of that signal in series with the V_{BB} supply, then the base current will have sinusoidal variations superimposed on the value of I_B.

- As a consequence, the collector current also will have sinusoidal variations superimposed on the value of I_C, producing in turn corresponding change in the value of V_O.

- We can measure the ac variations across the input and output terminals by blocking the dc voltages by large capacitors.



In general, amplifiers are used to amplify alternating signals. Now let us superimpose an ac input signal *vi* (to be amplified) on the bias V_{BB} (dc). The output is taken between the collector and the ground.

First assume that $v_i = 0$.

Then applying Kirchhoff's law to the output loop, we get

$$V_{cc} = V_{CE} + I_c R_L$$

Likewise, the input loop gives

$$V_{BB} = V_{BE} + I_B R_B$$

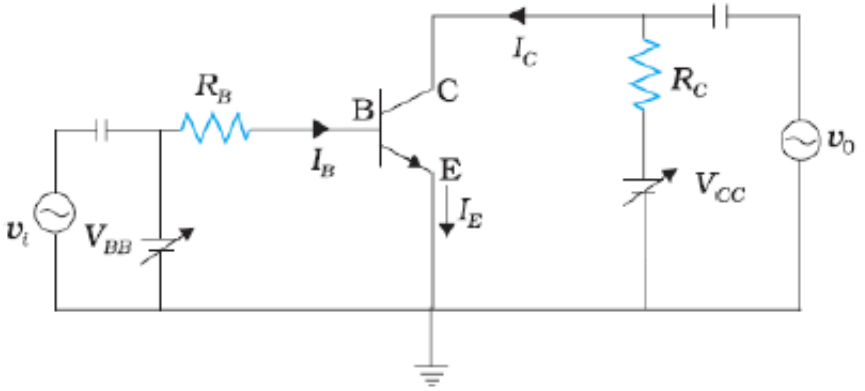
When v_i is not zero, we get

$$V_{BB} + v_i = V_{BE} + I_B R_B + \Delta I_B (R_B + r_i)$$

$$v_i = \Delta I_B (R_B + r_i) = r \Delta I_B$$

The change in I_B causes a change in I_c.

We define a parameter β_{ac},



$\beta_{ac} = \Delta I_C / \Delta I_B = I_C / I_B$

which is also known as the *ac current gain*.

Usually βac is close to βdc in the linear region of the output characteristics.

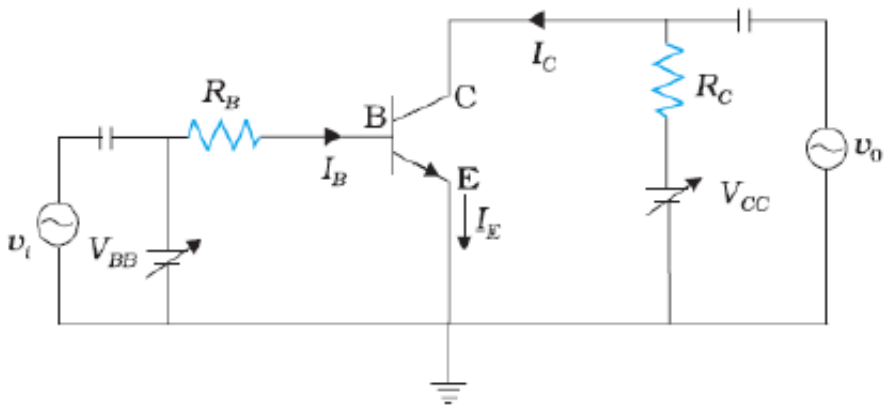
The change in I_c due to a change in I_B causes a change in V_{CE} and the voltage drop across the resistor R_L because V_{CC} is fixed.

These changes can be given as

$\Delta V_{CC} = \Delta V_{CE} + R_L \Delta I_C = 0$

or $\Delta V_{CE} = -R_L \Delta I_C$

The change in V_{CE} is the output voltage v_0.



$v_0 = \Delta V_{CE} = -\beta_{ac} R_L \Delta I_B$

The voltage gain of the amplifier is

$A_v = v_0 / v_i = \Delta V_{CE} / r\Delta I_B = -\beta_{ac} R_L / r$

The negative sign represents that output voltage is opposite with phase with the input voltage.

Field-Effect Transistors (FETs)

- Work by controlling a current with an electric field produced by an applied voltage
- Compare this that of bipolar transistor where base current is used
- Hence, control electrode (gate) draws virtually no current, only leakage current
- Results in high input impedance ~$10^{14}\Omega$; essential in many applications

Advantages:

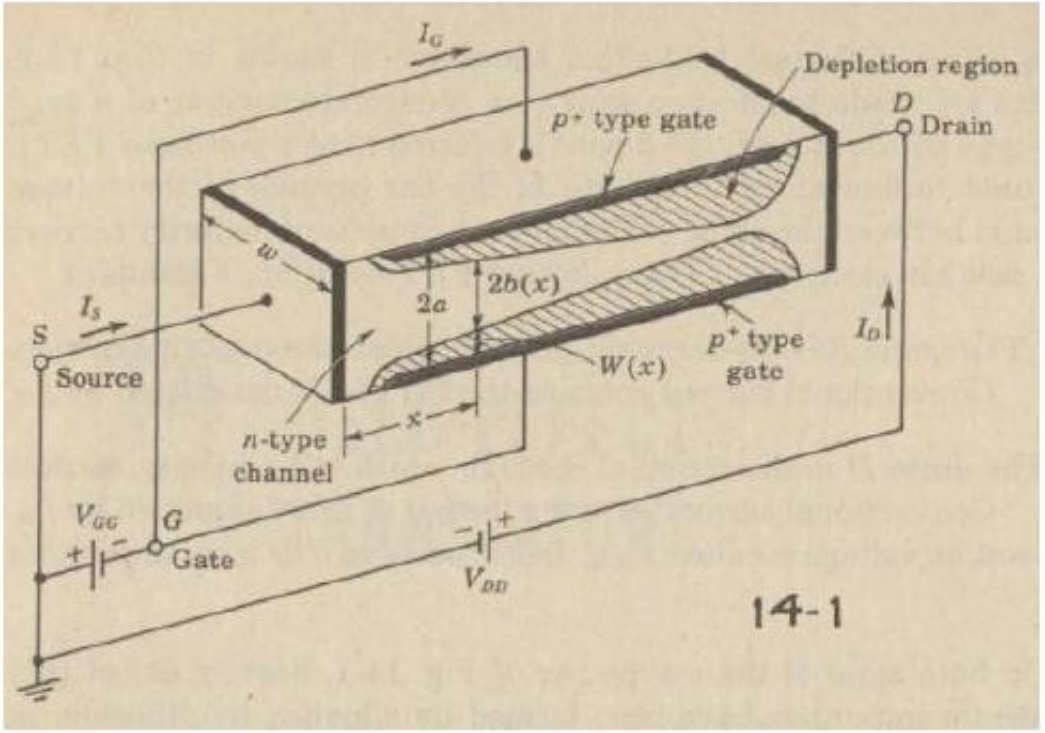
- Operation depends on flow of majority carriers only, a unipolar device like vacuum tube. Conventional transistor is a bipolar device
- Relatively immune to radiation
- High input impedance
- Less noisy than a tube or a bipolar transistor
- No offset current at zero drain current
- Thermal stability
- Small area devices

Main applications

- Linear and logic switches
- Amplifiers
- Voltage controlled resistors
- Current sources
- Useful for building LSI circuits
- High current FET devices
- Signal choppers

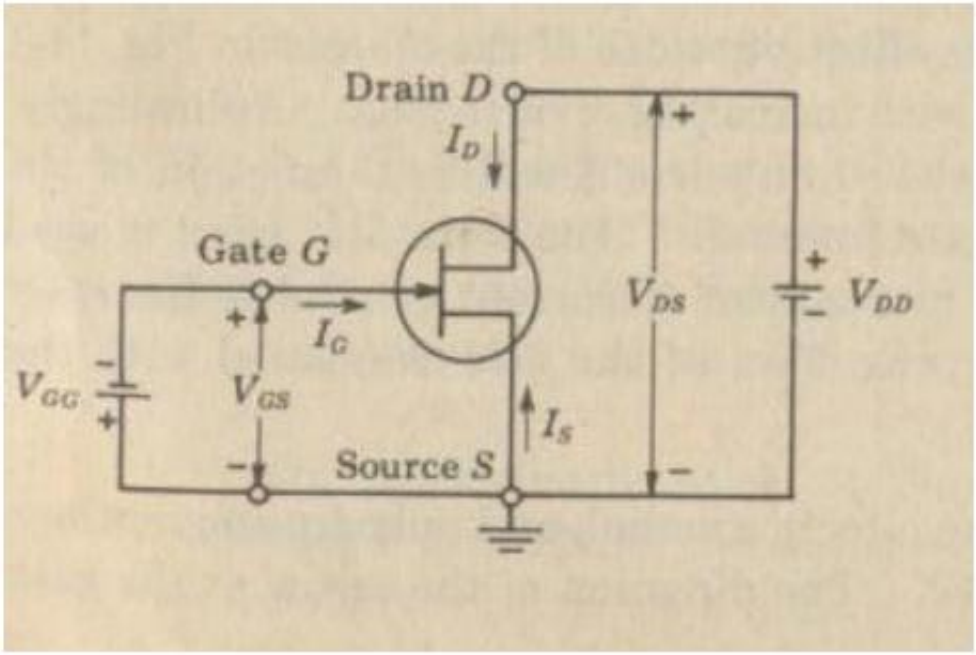
FET standard notations

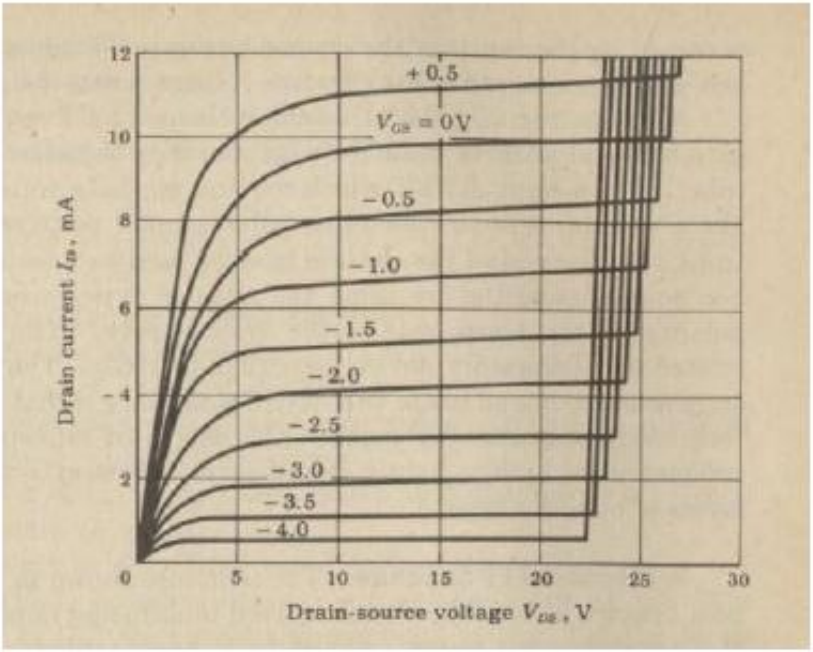
n-channel FET for example
Ohmic contacts are made to the ends of a n-type semiconductor bar.
Current is flown along the bar due to the supply between the ends.



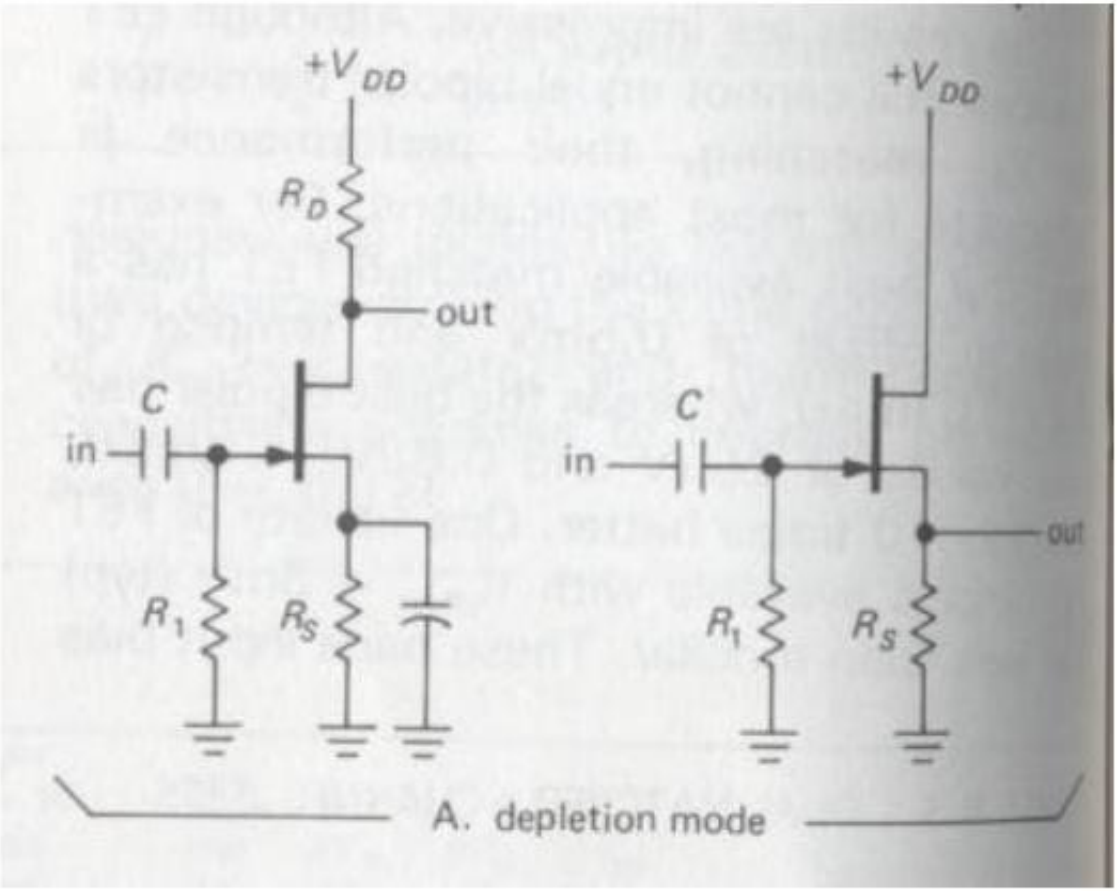
- Source (S): Terminal through which the majority carriers enter the bar. Current is I_S.
- Drain (D): Terminal through which the majority carriers leave the bar. Current is I_D. The drain-to-source voltage is called V_{DS} and is positive if D is more positive than S.
- Gate (G): On both sides of the n-type bar, heavily doped (p^+) regions of acceptor impurities formed, creating p-n junctions. Gate-source voltage is V_{GS}, applied to reverse bias the p-n junction. Gate current is I_G.
- Channel: n-type material between the two gate regions is the channel through which the majority carriers move from source to drain.

FET characteristics

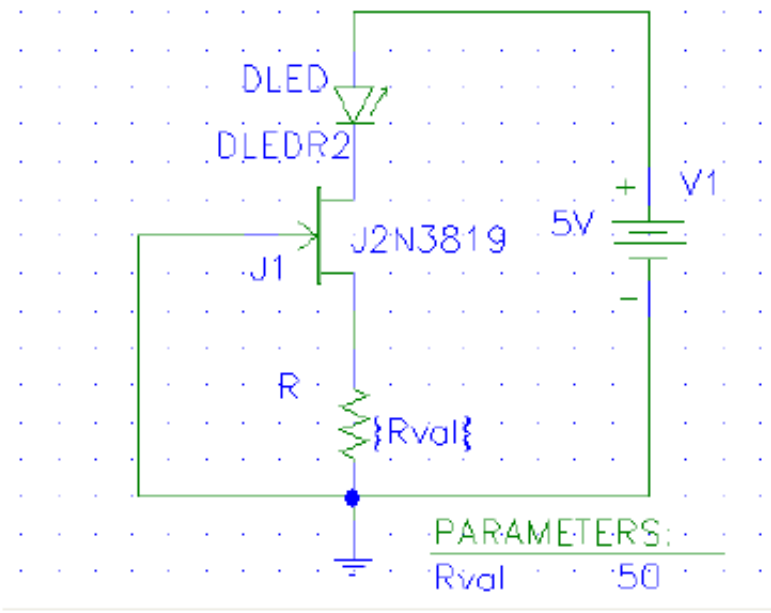




FET amplifiers



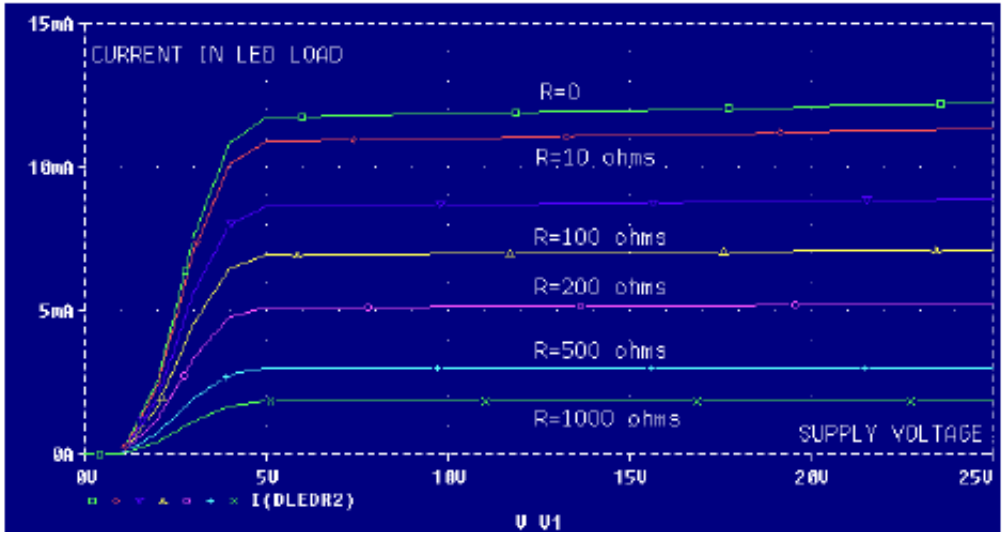
JFET current sources



The LED works most consistently if the current passing through it can be maintained constant, even if the supply voltage changes - for example, as the battery discharges.

The source resistor R determines the gate source voltage through the relationship $V_{GS} = -V_{S0} = -I_D R$

This allows a range of currents to be achieved, since the operating conditions of the JFET can be chosen by selecting the value of R, which determines the relative values of I_D and V_{GS} .



Had we used a resistor on its own to try and control the current through the LED, the current would have been strongly dependent on V1 for all values.

Metal-Oxide-Silicon (MOS) devices

- Principle of MOS Field Effect Transistor transistor operation

  Metal (poly) gate on oxide between source and drain

  Source and drain implants of opposite type to substrate.

  Gate is biased to **invert** channel below oxide

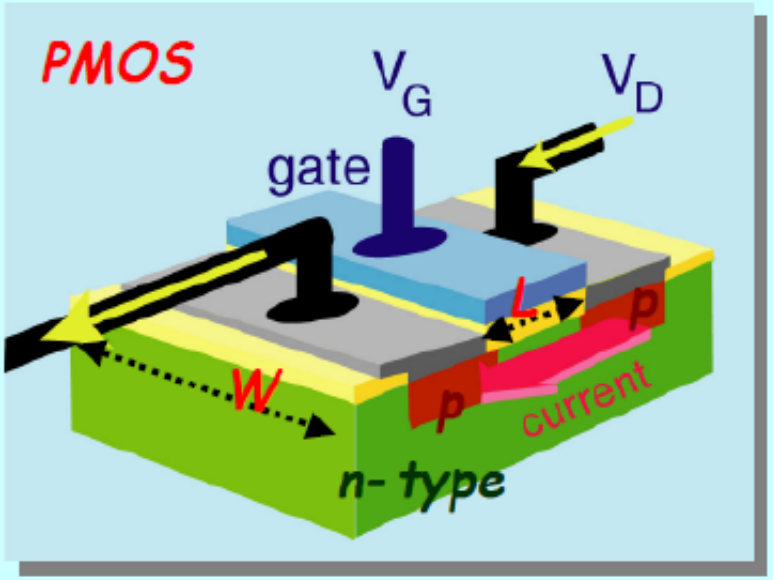
  apply voltage bias to gate, which...

  gives field across oxide

  modulates current in conducting channel

  transistor can be used as

  switch (digital) or amplifier (analogue)



The 'metal' in the name MOSFET is now often a misnomer because the previously metal gate material is now often a layer of polysilicon. Aluminium had been the gate material until the mid 1970s, when polysilicon became dominant, due to its capability to form self-aligned gates. Metallic gates are regaining popularity, since it is difficult to increase the speed of operation of transistors without metal gates. Likewise, the 'oxide' in the name can be a misnomer, as different dielectric materials are used with the aim of obtaining strong channels with applied smaller voltages.

MOS Field Effect Transistor

- Operation - input signal is voltage on gate

  very high input impedance > $10^{12}\Omega$

- I-V behaviour nMOS

  $V_G > V_T$ to switch on, vary V_{DS}

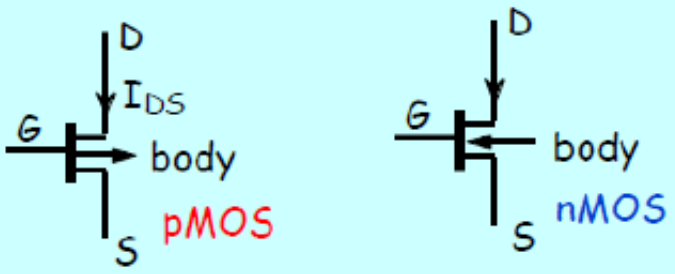
  linear region

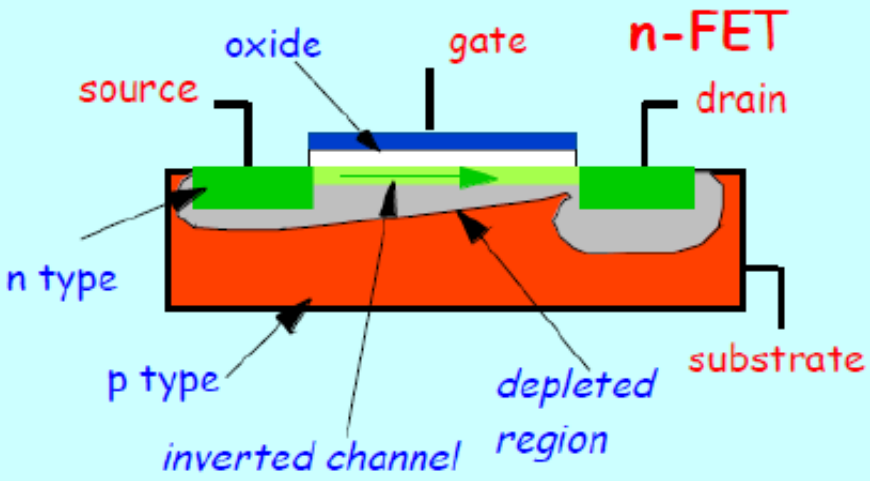
  $I_{DS} \sim (V_G - V_T)V_{DS}$

  saturation region

  channel "pinch off" near drain

  $I_{DS} \sim (V_G - V_T)^2$

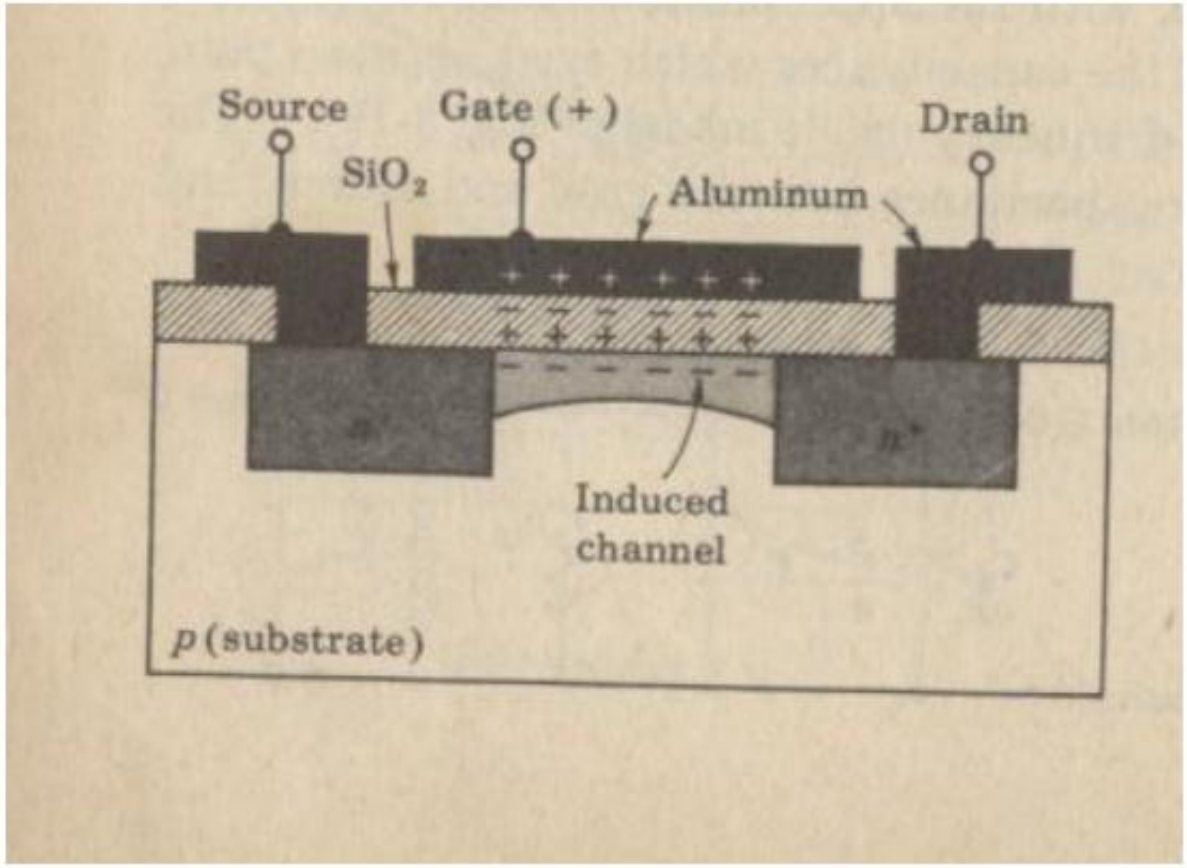




$\partial I_{DS}/\partial V_{GS} = i_{ds}/v_{gs} = g_m = (2\mu C_{ox} I_{DS} W/L)^{1/2}$ transconductance

defined by geometry & current only - important for IC design

Enhanced mode MOSFET

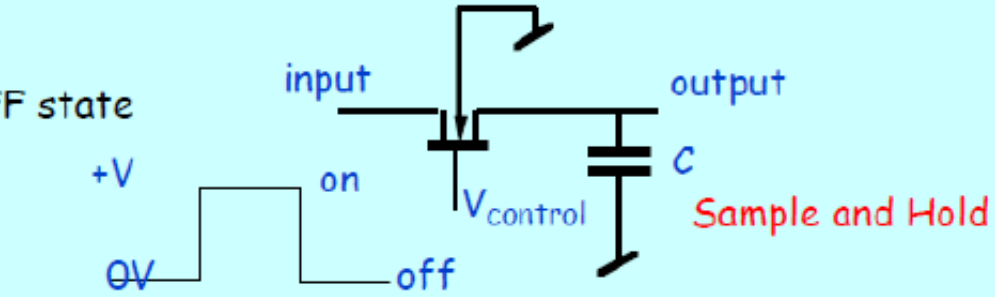


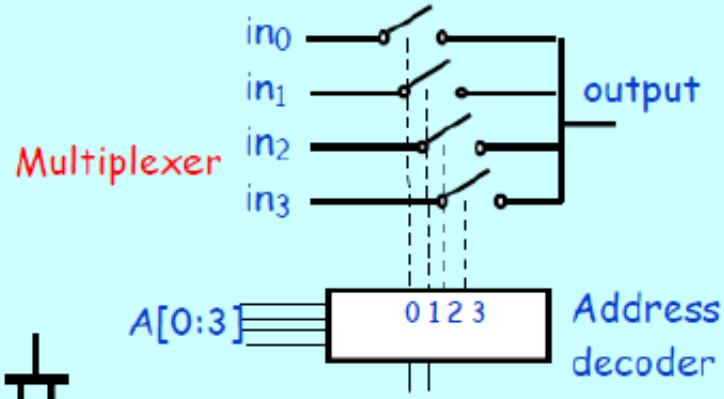
- When the gate voltage V_{GS} is below the threshold for making a conductive channel; there is little or no conduction between the terminals source and drain; the switch is off.
- When the gate is more positive, it attracts electrons, inducing an *n*-type conductive channel in the substrate below the oxide, which allows electrons to flow between the *n*-doped terminals; the switch is on.

Cut-off ($V_{GS} < V_{th}$), linear ($V_{GS} > V_{th}$ and $V_{DS} < (V_{GS} - V_{th})$) or saturation ($V_{GS} > V_{th}$ and $V_{DS} > (V_{GS} - V_{th})$) modes of operation

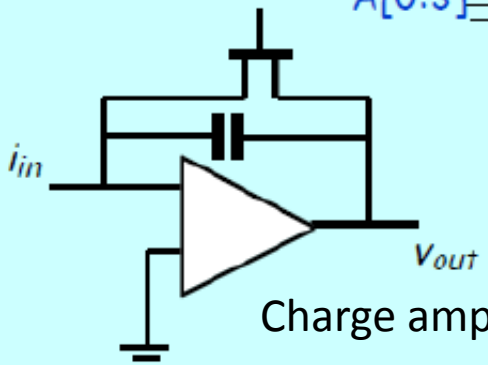
Simple MOSFET applications

- Voltage controlled switch
  - very high resistance in OFF state
  - R_{ON} ~ 5 - 100Ω
  - fast response ~nsec
  - bi-directional



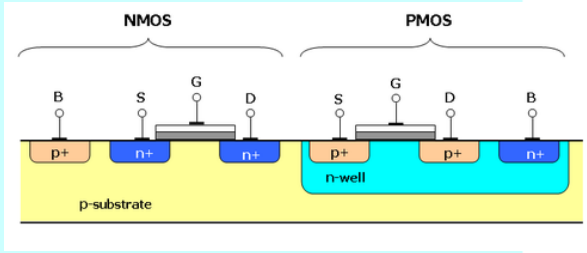


- Voltage controlled resistor
  - operate in linear region
  - $R_{DS} \sim 1/(V_G - V_T)$
  - convenient for IC design



Charge amplifier

CMOS = Complementary MOS



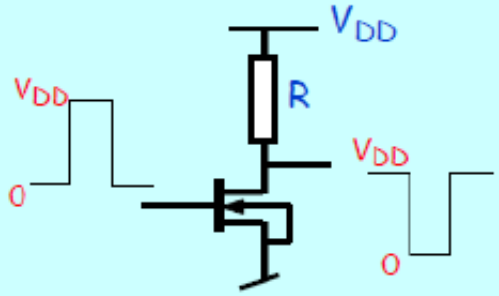
- Both pMOS and nMOS transistors on same wafer

  by putting p-type "wells" into n-type wafer (or vice-versa)

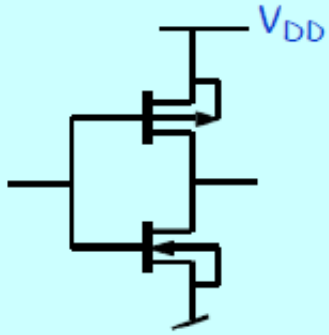
  build nMOS transistors in locally p-type region

- Why?

NMOS inverter



CMOS inverter



NMOS consumes power in low state

CMOS version consumes power only when switching

basis of almost all modern logic

In IC technologies, accurate resistors are harder to make than C and transistors

CMOS – for low power applications

- The MOSFET is used in digital complementary metal–oxide–semiconductor (CMOS) logic, which uses p- and n-channel MOSFETs as building blocks.
- Overheating is a major concern in integrated circuits since ever more transistors are packed into ever smaller chips.
- CMOS logic reduces power consumption because no current flows (ideally), and thus no power is consumed, except when the inputs to logic gates are being switched.
- CMOS accomplishes this current reduction by complementing every nMOSFET with a pMOSFET and connecting both gates and both drains together.
- A high voltage on the gates will cause the nMOSFET to conduct and the pMOSFET not to conduct and a low voltage on the gates causes the reverse.
- During the switching time as the voltage goes from one state to another, both MOSFETs will conduct briefly.
- This arrangement greatly reduces power consumption and heat generation.

Power MOSFETs

Enhancement-mode MOSFETs capable of handling high voltages and currents are now available.

Typical parameters are:

- V_{DS} = 400V
- I_D = 20Amps
- R_{DS} (ON) = 0.055Ω

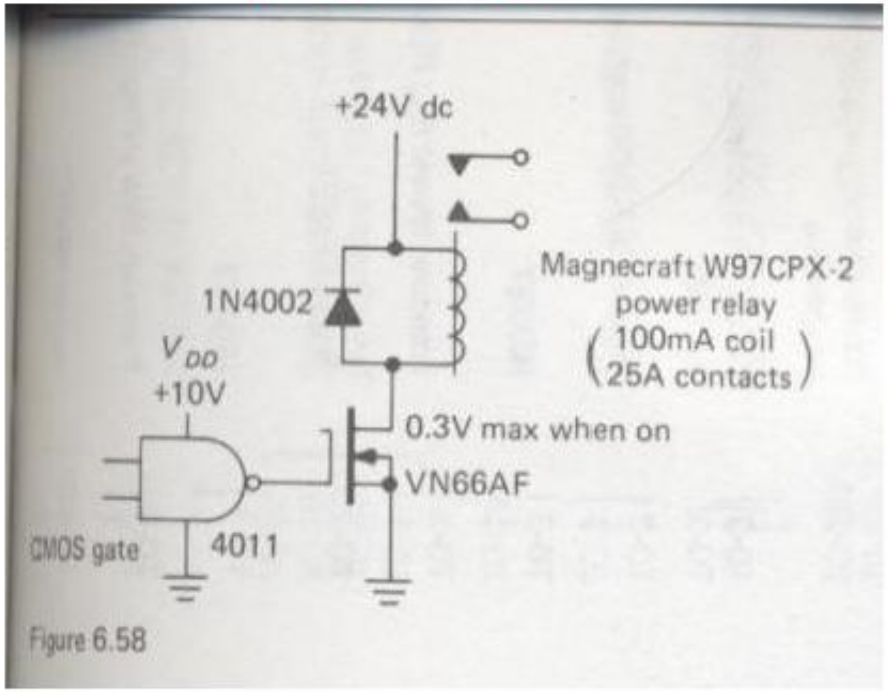


Figure 6.58

Some more advantages over bipolar transistors:

- High input impedance
- Absence of thermal runaway, $I_D \alpha 1 / T$.
- MOSFETs can be paralleled without the current-equalizing resistors
- Excellent choice for the saturated switch
- On MOSFET behaves like a small resistance

Disadvantages

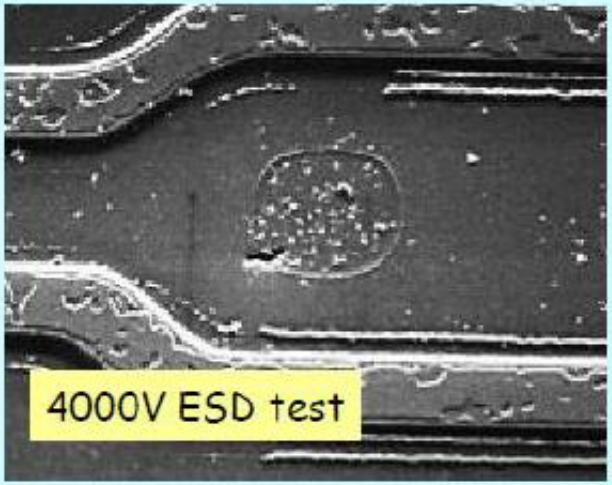
- On Resistance
  - Although small, it contributes to RC time in fast switches
- Capacitance
  - Inevitable capacitances between nodes, important for high speed circuits
- Relevance to op-amps
  - FET amplifiers have much higher input impedance and draw much lower currents
- Latch-up
  - Under certain conditions, parasitic bipolar transistors formed
  - MOS circuits can go into high current states - destructive
- ESD
  - Care needed in handling
  - Static electricity developed in the body; shipping, inserting the chip
  - Protection networks can degrade performance
- Small gain-bandwidth product in comparison with bipolar transistor
- Glitches

  Gate to channel capacitively coupled

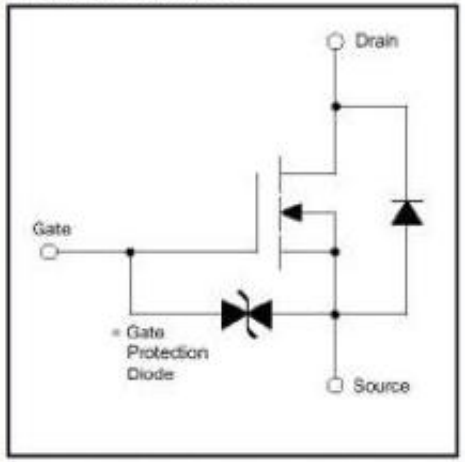
  Ex: Multiplexer during transitions of the input address

ElectroStatic Discharge

- MOS circuits are prone to damage from ESD
  - gate oxides are thin layers - few nm in advanced technologies
  - oxide breakdown field < 1000MV/m = 1V/nm
- Human body can easily charge to 30-40kV walking across carpet on a dry day
  - precautions:
  - circuits designed with protection diodes
  - stand on conductive pad and earth body with wrist strap



●Equivalent circuit



•A protection diode is included between the gate and the source terminals to protect the diode against static electricity when the product is in use. Use a protection circuit when the fixed voltages are exceeded.

September 18, 2012

LECTURE-7

General comments

- In control systems, feedback consists in comparing the output of the system with the desired output and making a correction accordingly.
- In amplifier circuits the output should be a multiple of the input, so in a feedback amplifier the input is compared with an attenuated version of the output.
- Negative feedback is the process of coupling the output in such a way as to cancel some of the input.
- Amplifier gain is reduced, but improves other characteristics:
  - Freedom from distortion
  - Linearity
  - Flatness of response
  - Predictability of gain
  - Improved input and output impedances
- As more FB is used, the resultant amplifier characteristics become less dependent on the characteristics of the open-loop amplifier and finally depend only on the properties of the FB network itself.
- Positive FB, oscillator ➔ Compensation

Advantages of feedback

- Why sacrifice gain?

even if amplifier gain is defined

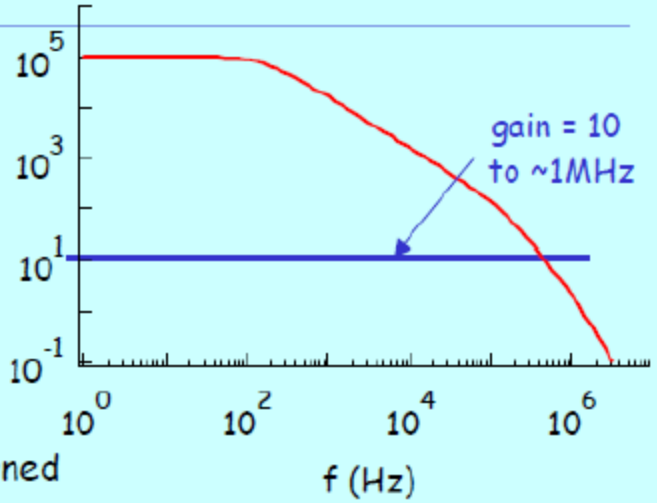
component gain is not a reliable quantity

gain in feedback circuits fixed by components

can choose precision

negative feedback improves performance

stability, linearity, distortion



some components approaching ideal can be designed

eg current sources with very high output impedance

real gain depends on frequency

designing for lower closed loop gain extends f range where gain is uniform

- up to some limit

frequency dependent feedback can be used

simplifies some designs

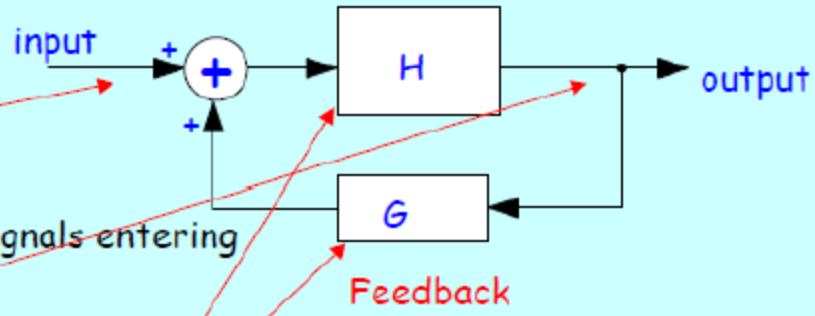
positive feedback has uses - eg oscillators

Negative feedback amplifier may become unstable and break into oscillations

System block diagrams

- Introduction to...

- Points to note
  - summing node
    - output from node = sum of signals entering
    - note signs at entry
  - pick-off node
    - all outgoing signals = incoming signal
  - functional blocks & directions of signals
    - usually label with transfer function of block



don't always distinguish summing nodes from others in diagrams - but only if it's very clear

- What kind of system?
  - electronic - but also mechanical, acoustic, optical,..

- How to manipulate?
  - label with signals, then follow rules

Feedback

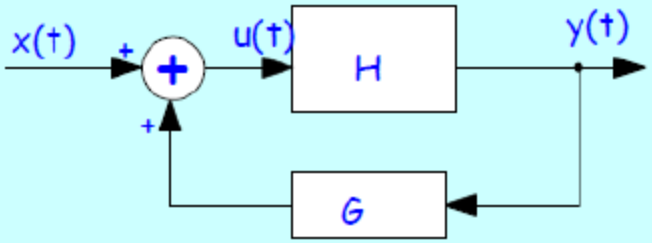
- After summing node

  $u(t) = x(t) + Gy(t)$

- At output

  $y(t)$, but also $Hu(t)$

  so $y(t) = H[x(t) + Gy(t)]$



$H_{system} = y(t)/x(t) = H/(1 - GH)$

- Why is this useful?

  suppose $H \gg 1$ then $H_{system} = -1/G$ ie. system transfer function independent of H

  eg $0 < G < 1$ system provides constant amplification

  G = feedback fraction

- Problems -

  perhaps $G \to 1/H$ $H_{system} \Rightarrow \infty$ unstable - positive feedback

  system will always be stable with negative feedback

H_{system} = Closed loop gain, H=Open loop gain, GH = Loop gain, 1-GH is return difference

Feedback network = Beta network

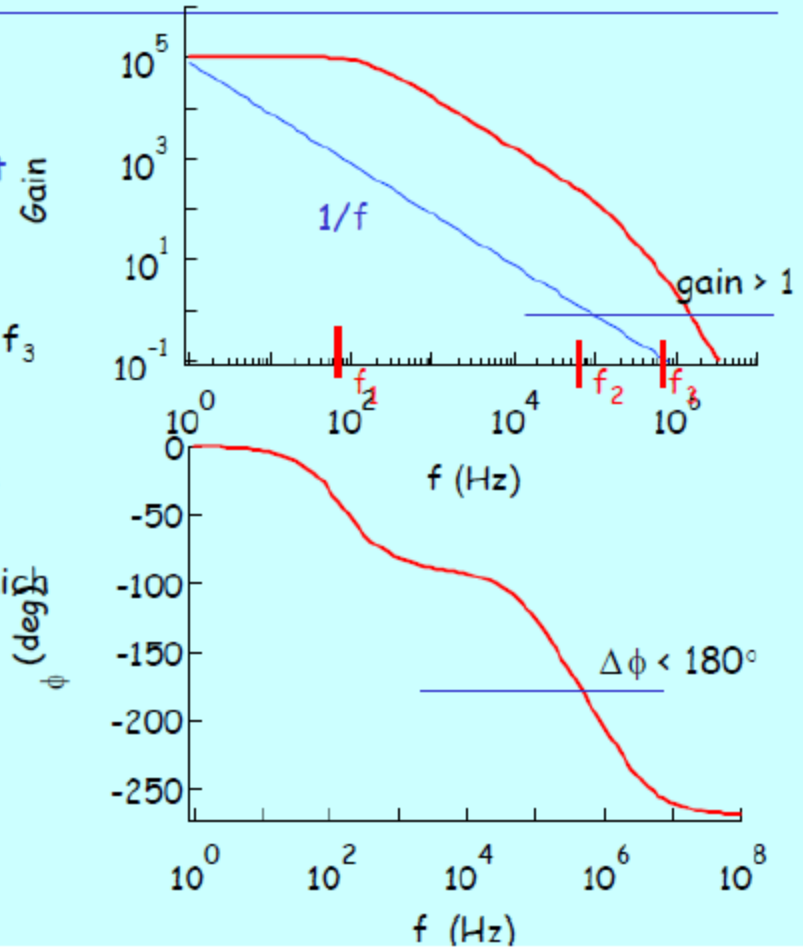
Ideal amplifier characteristics

1. Voltage
2. Current
3. Transconductance
4. Transresistance

Parameter	Voltage	Current	Transconductance	Transresistance
R_i	∞	0	0	0
R_o	0	∞	∞	0
Transfer characteristic	$V_o = A_v V_s$	$I_L = A_i I_s$	$I_L = G_m V_s$	$V_o = R_m I_s$

Op-amp frequency response

- Reason for falling gain with frequency
  - low pass filters in different stages
  - formed by natural capacitances present in circuit
- Poles
  - amplifier illustrated has poles at f_1, f_2, f_3
  - can give stability problems
  - if phase shift > 180° negative feedback becomes positive
  - must ensure gain < 1 at frequency at which phase shift > 180°
  - some op-amps have this built in
  - if not, reduce gain
  - if feedback network introduces phase changes, then this must be included in discussion



Why use differential amplifiers?

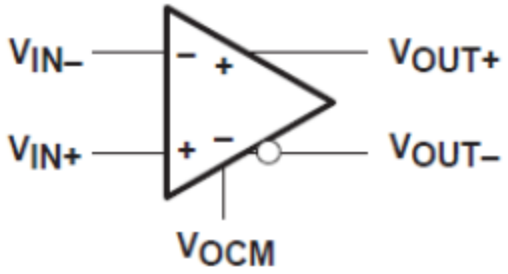
- Increased immunity to external noise
- Increased output voltage swing for a given voltage rail
- Ideal for low-voltage systems
- Integrated circuit is easier to use
- Reduced even-order harmonics

The term *balanced* is sometimes used to refer to differential-signal transmission. This conveys the idea of symmetry, which is very important in differential systems. The receiver has balanced inputs, the line has balanced characteristics and the driver has balanced outputs.

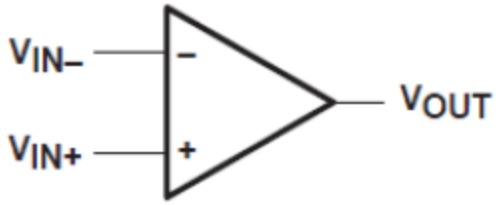
There are two methods commonly used to manipulate differential signals: electronic and transformer.

- Electronic methods have advantages, such as lower cost, small size and weight, and wide bandwidth.
- Transformers offer very good CMRR versus frequency, galvanic isolation, no power consumption (efficiencies near 100%), and immunity to very-hostile EMC environments.

Differential Amplifier vs Standard Operational Amplifier



Fully-Differential Amplifier



Standard Operational Amplifier

FULLY-DIFFERENTIAL AMPLIFIER

Differential in

Differential out

Output common-mode voltage set by Vocm

Multiple feedback paths

STANDARD OPERATIONAL AMPLIFIER

Differential in

Single-ended out

Output common-mode voltage is signal

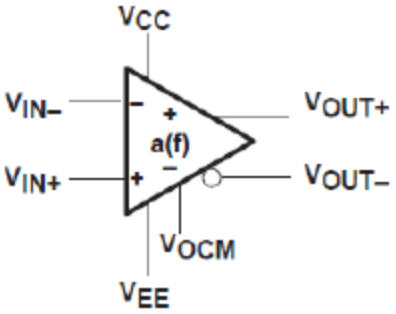
Single feedback path

Some definitions

The voltage difference between the plus and minus inputs is the input differential voltage, Vid. The average of the two input voltages is the input common-mode voltage, Vic.

The difference between the voltages at the plus and minus outputs is the output differential voltage, Vod. The output common-mode voltage, Voc, is the average of the two output voltages, and is controlled by the voltage at Vocm.

With a(f) as the frequency-dependant differential gain of the amplifier, then Vod = Vid × a(f).



Input voltage definition	**Vid = (Vin+) – (Vin–)**	$Vic = \frac{(Vin+) + (Vin-)}{2}$
Output voltage definition	**Vod = (Vout+) – (Vout–)**	$Voc = \frac{(Vout+) + (Vout-)}{2}$
Transfer function	**Vod = Vid × a(f)**	
Output common-mode voltage	**Voc = Vocm**	

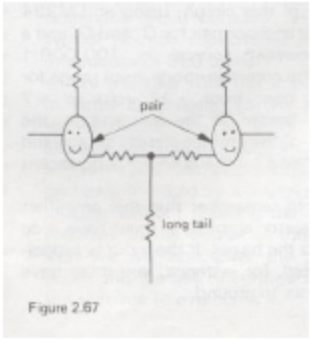
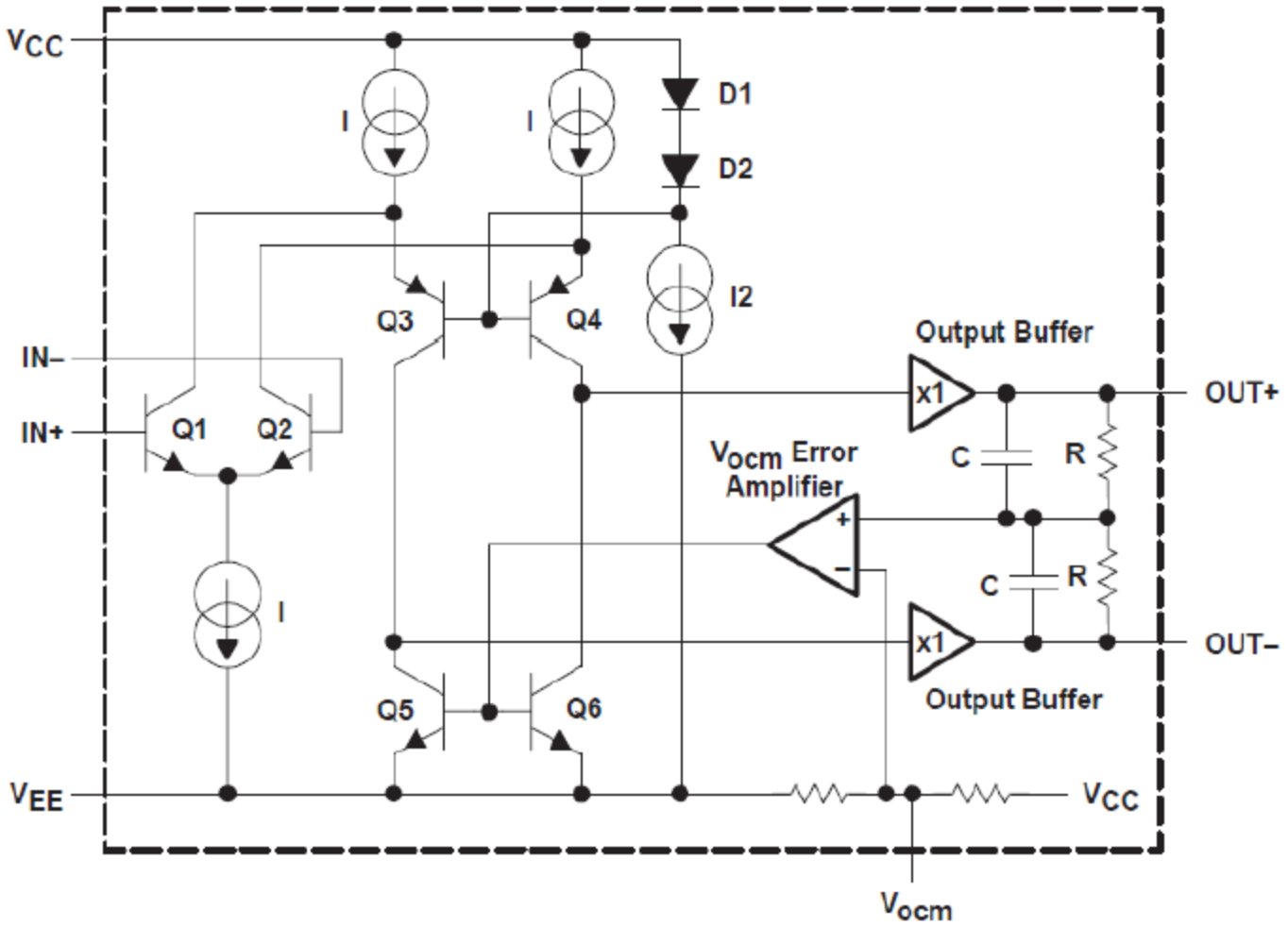
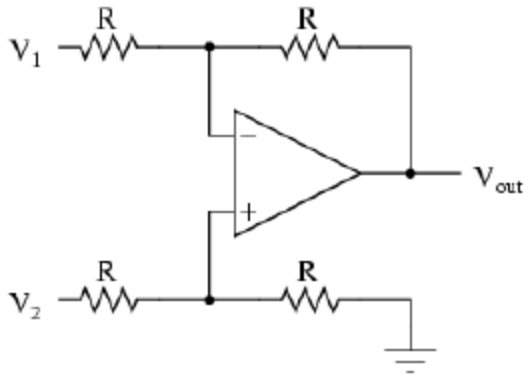


Figure 2.67

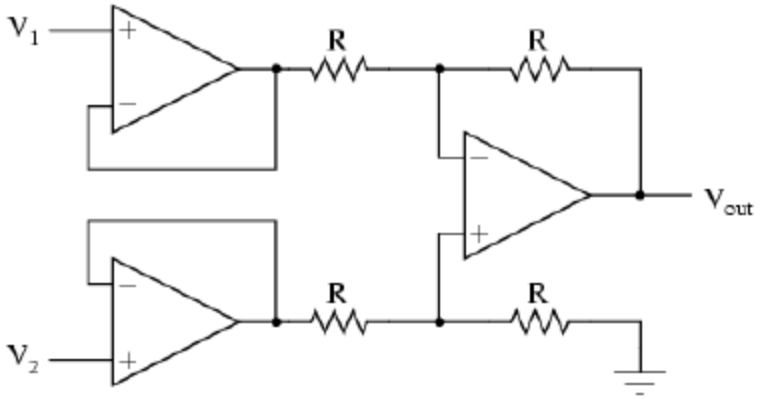
Simplified Differential Amplifier



Building a differential amplifier



$$V_{out} = V_2 - V_1$$



Signals

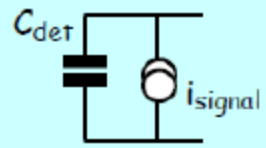
- Signal
  - generalised name for input into instrument system
- Might seem logical to consider signals before sensors but can now see
  - wide range of signal types are possible
    - *depend on sensor*
    - *depend on any further transformation - eg light to electrical*
- Most common types of signal
  - short, random pulses, usually current, amplitude carries information
    - *typical of radiation sensors*
  - trains of pulses, often current, usually binary
    - *typical of communication systems*
  - continuous, usually slowly varying, quantity - eg. current or voltage
    - *slow - typical of monitoring instruments*
    - *fast - eg cable TV, radio*
- terms like "slow", "fast" are very relative!

Sensor equivalent circuits

- Many of the sensors considered so far can be modelled as

  current source + associated capacitance

  typical values ~ few pF



  but can range from

  ~100fF semiconductor pixel

  ~10-20pF gas or Si microstrip, PM anode

  ~100pF large area diode

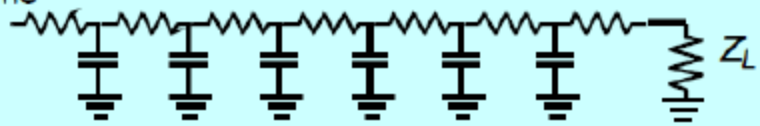
  ~μF wire chamber

  usually there is some resistance associated with the sensor, eg leads or metallisation but this has little effect on signal formation or amplification

- Notable exception: microstrips - gas or silicon

  the capacitance is distributed, along with the strip resistance

  forms a dissipative transmission line



Signal formation

- Issues in practical applications

duration

radiation: depends on transit time through sensor and details of charge induction process in external circuit

linearity

most radiation sensors characterised, or chosen for linearity
for commercial components can expect non-linearity, offset and possible saturation

reproducibility

eg. many signals are temperature dependent in magnitude - mobility of charges
other effects easily possible

ageing

sensor signals can change with time for many reasons
natural degradation of sensor, variation in operating conditions, radiation damage,...

- all these effects mean one should always be checking or calibrating measurements intended for accuracy as best one can

Typical signals

- Some examples

Signal source	Duration
Inorganic scintillator	$e^{-t/\tau}$ τ ~ few μs
Organic scintillator	$e^{-t/\tau}$ τ ~ few ns
Cerenkov	~ns
Gaseous	few ns - μs
Semiconductor	~10ns
Thermistors	continuous
Thermocouple	continuous
Laser	pulse train ~ps rise time or short pulses ~fs

- However, we will find later that speed of signal is not always sufficient to build fast responding systems

Amplifiers

- This is a large and important part of this course

  amplifiers are needed for many instruments

- inescapable in electronic instruments

  even if not used to boost signals, amplifiers are the basis of most important functional blocks

- in many circumstances amplification, in the sense of "boosting" signals, is vital

  signals to be measured or observed are often small

    defined by source - or object being observed

    and sensor - it is not usually easy to get large signals

  data have to be transferred over long distances without errors

    safest with "large" signals

Operational amplifier

- A good starting point for analogue electronics
  - will later consider devices and components used to build real amplifiers but the op-amp is a convenient idealisation
- building block
  - much electronics consists in recognising building blocks which perform specific functions
    - *a large circuit can appear quite complex but can often be reduced to much simpler functional elements*
- First questions to ask in analysing amplifying system
  - what quantity is being amplified? - eg. current, charge or voltage
  - what type of signals? eg. fast pulses or slow waveforms?
  - what is the input and output impedance? ie how should it be connected?
  - what is the gain?
- some more detailed information...
  - frequency response, linearity, noise level, ...

September 20, 2012

LECTURE-8

Operational amplifier approximation

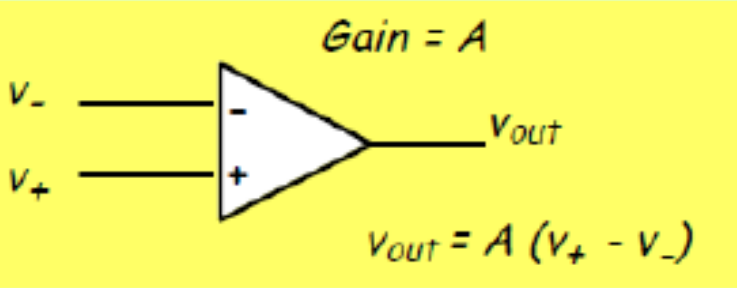
•very high gain **voltage** amplifier

gain = $A \rightarrow \infty$

infinite bandwidth

single output

dual, differential inputs, infinite impedance



amplifies difference in voltages between inputs

inputs are DC coupled

•Real op-amps almost invariably used with (negative) feedback

fraction of the output voltage fed back to the inverting input and subtracted from input signal.

***open loop** gain refers to amplifier gain **without** feedback*

***closed loop** … **with** feedback*

•Rules for calculation - (only hold with negative feedback)

(i) inputs approach same voltage ($v_+ = v_-$)

(ii) inputs draw no current

only possibility for stability

Inverting amplifier

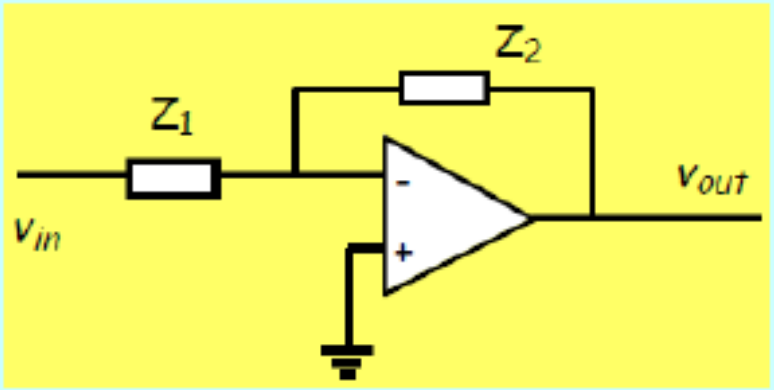
- Apply these rules

  $v_- = v_+ = 0$

- Consider current flow

  $(v_{in} - v_-)/(v_- - v_{out}) = Z_1/Z_2$

  $Gain_{closed\ loop} = v_{out}/v_{in} = -Z_2/Z_1$



NB +/- connections

- Inverting input is virtual ground

  held at 0V by rule (i)

- Input impedance

  source at input sees only Z_1 to ground

  so effective input impedance $\approx Z_1$

  usually low if aiming for - sometimes a disadvantage

Non-inverting amplifier

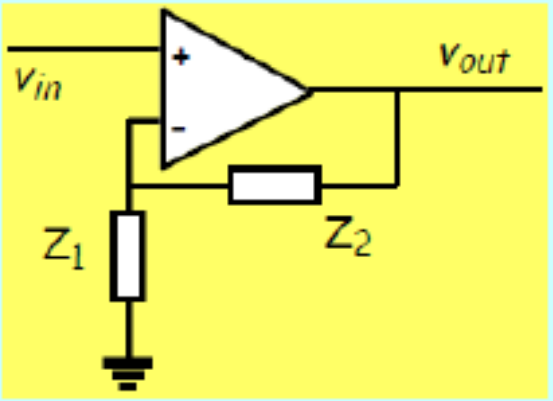
- Apply rules

  $v_{in} = v_+ = v_-$

- Voltage divider in feedback network

  $v_- = v_{out} Z_1/(Z_1 + Z_2)$

  $Gain_{closed\ loop} = v_{out}/v_{in} = 1 + Z_2/Z_1$



NB connections

- Input impedance

  source at input sees only input impedance of op-amp input = very high (∞)

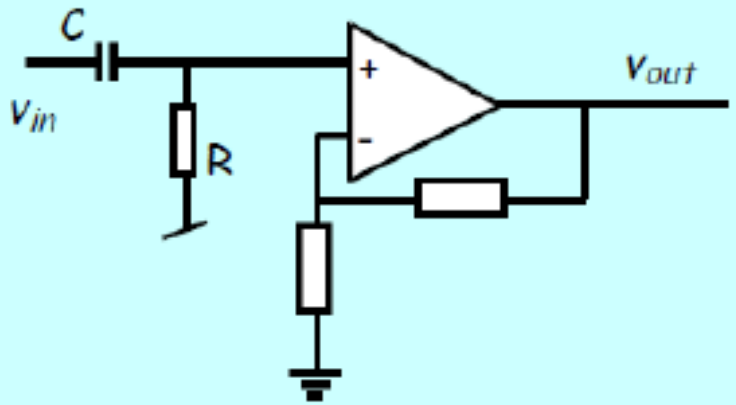
  convenient for driving from any source

- Coupling signals in

  real amplifiers do draw small currents

  so if input is ac coupled, need a path for current to flow to ground

  make RC >> relevant time constant



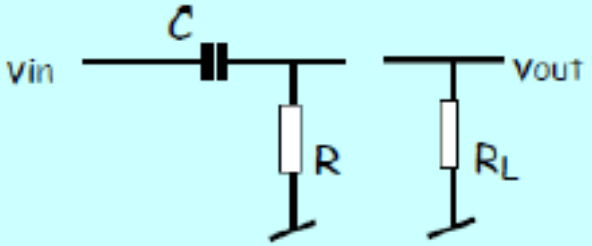
Buffers and loading

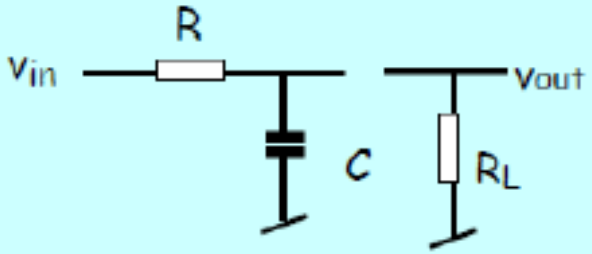
- Play an important role in connecting circuit elements or blocks

  eg a block may have a high output impedance where a low value is required

  or a high input impedance where … etc

- A load can change the characteristics of the circuit…

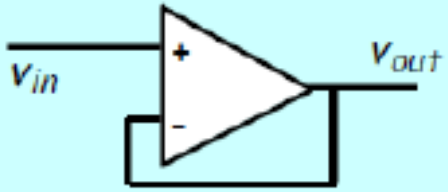




to overcome, insert a stage which matches impedances better

ie. isolates one stage from another

eg



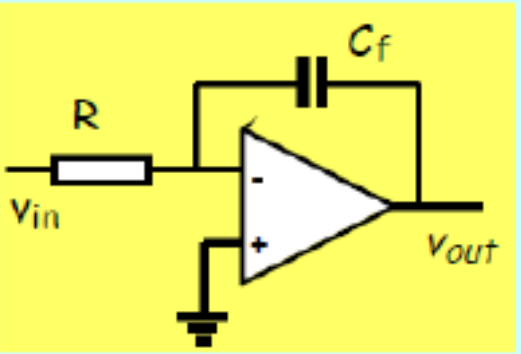
Integrator

- Variant of inverting amplifier where current is integrated on feedback capacitor

$i_{in} = v_{in}/R$

$V_{out} = -(1/RC_f)\int v_{in} dt$

useful for control circuits



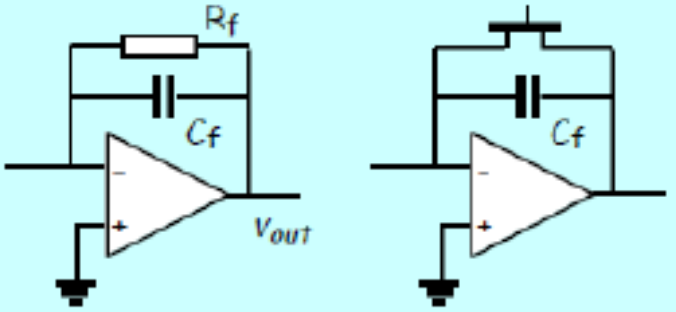
- it will often be convenient to analyse this circuit for pulse processing, where often more convenient to work in frequency domain

$v_{out} = -i_{in}/j\omega C_f$

R is noise source and adds to input impedance

remove for charge integrator

$v_{out} = -Q_{in}/C_f$



- Must have a means of resetting the amplifier

provide a parallel resistor or a transistor switch

R_fC_f >> integration time

Other useful blocks

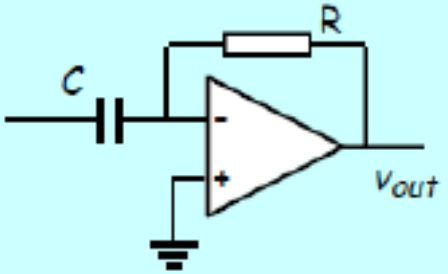
- Differentiator

  $i = C dV/dt$

  $v_{out} = -RC dV/dt$

  or

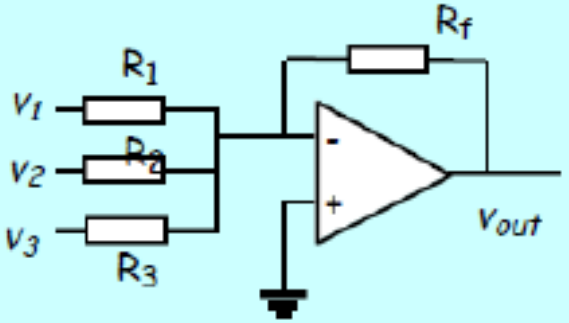
  $v_{out}/v_{in} = -j\omega RC$



- Summing amplifier

  weighted sum of inputs

  (consider currents)

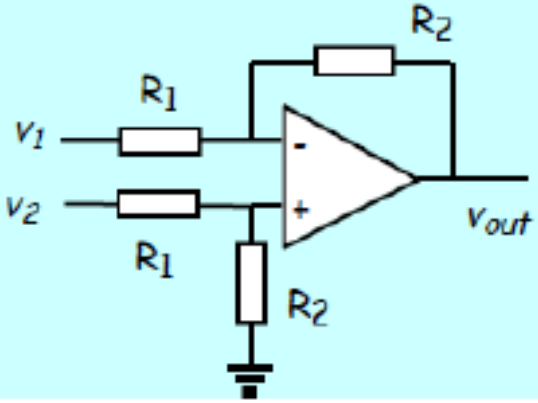


- Differential amplifier

  $v_{out} = (R_2/R_1)(v_2 - v_1)$

  for matching need accurate component values

  nice feature: removes common mode signal



Common mode

- Suppose two signals at differential amplifier input are v_1 & v_2

  in many cases they may have a common component

  ie $v_1 = u_1 + v_{cm}$ $\quad\quad$ $v_2 = u_2 + v_{cm}$

  v_{cm} is called the common mode, remainder is normal mode

- The nice feature of a differential amplifier is

  $v_{out} = G(v_2 - v_1) = G(u_2 - u_1)$

  this is a very effective way of subtracting interference which affects both signals equally

  eg power supply ripple

  can't be used as universal remedy: lose dynamic range

- Common Mode Rejection Ratio - CMRR

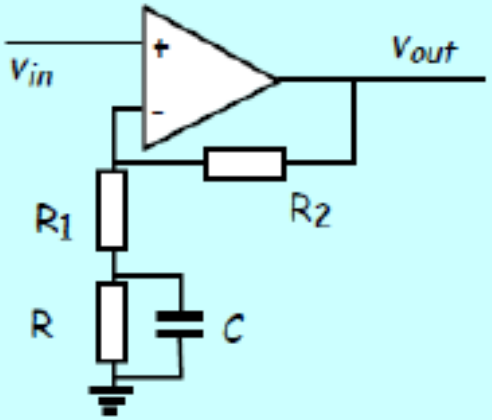
  CMRR = differential gain/common mode gain

  ~ 100-140dB for precision op-amps

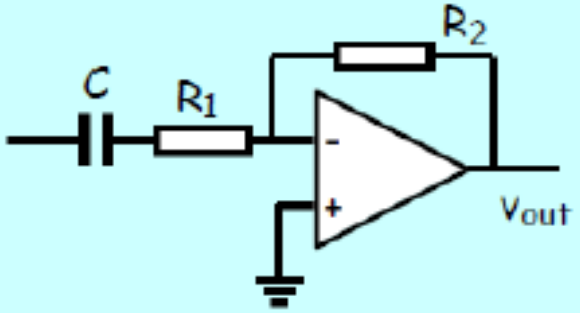
Many other possibilities

- Not restricted to using resistors only in circuit

  eg gain at low f (or DC) with different value at high f



differentiator/high pass filter with gain & inversion



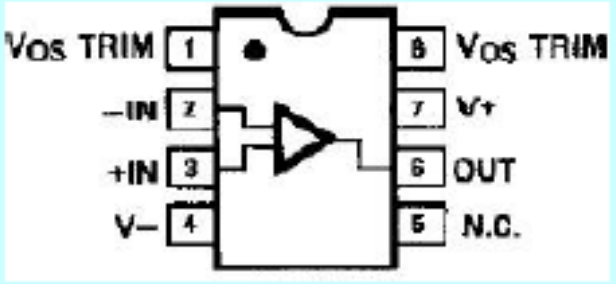
Non-ideal op-amp behaviour

- Just seen one example
  - inputs do draw small currents - input impedances are finite
  - real amplifiers do not have infinite gain but very high values can be obtained
    - *some examples of consequences later*
- Practical considerations
  - easy to assume zero output for zero input - may be true for ac, but not dc
  - op-amps have nulling connections, and recommended compensation to adjust
    - *often simple potentiometer (screwdriver adjustment)*
  - output impedance - ideal op-amp has open-loop $R_{out} \approx 0$
  - slew rate - how fast can output voltage change?
  - applied voltages are limited - certainly can't expect to exceed supply voltages!
  - behaviour can change with temperature - powered circuits need cooling!
  - frequency response and bandwidth - discuss further

- - most parameters are clearly specified so should use manufacturer's data to select best component for application
  - many of these are important in precision applications

Specifications & typical values

- Along with obvious parameters; R_{in}, R_{out}, CMRR, V_S, bandwidth, power consumption, gain and phase shift, manufacturer's data sheets also give:



- Input bias current I_B

  $0.5*(i_+ + i_-)$ with $v_+ = v_- = 0$ ~pA - nA

- Input offset current I_B

  $i_+ - i_-$ with $v_+ = v_- = 0$ ~fraction of I_B

- Input offset voltage V_{OS} & adjustment range

  v_{out} with $v_+ = v_- = 0$ ~ 10μV - 5mV

NB some of these are T dependent
so take care in assumptions when adjusted

- Input voltage range

  ~ $\pm|V_S|$ - 1V

- Slew rate (f dependent)

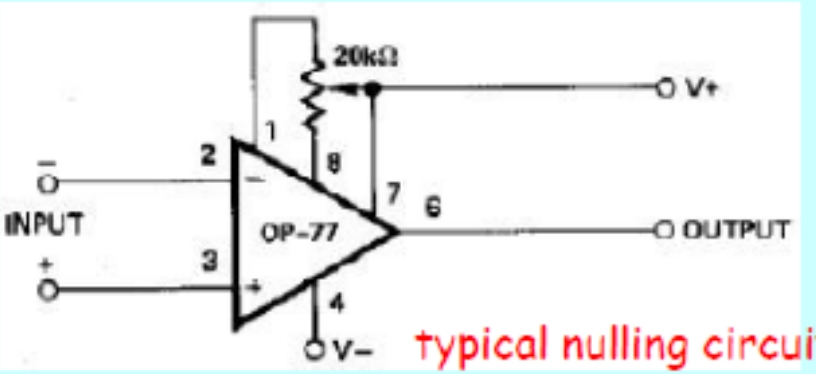
  maximum dv_O/dt ~ V/μs

- Power Supply Rejection Ratio (PSRR)

  small changes in V_S can resemble signals

  dB or μV/V

- Noise voltage & current (for later)



typical nulling circuit

September 25, 2012

LECTURE-9

Amplifiers in systems

- Amplification
  - single gain stage rarely sufficient
  - add gain to avoid external noise eg to transfer signals from detector
  - practical designs depend on detailed requirements
    - constraints on power, space,... cost in large systems
  - e.g. ICs use limited supply voltage which may constrain dynamic range
- Noise will be an important issue in many situations
  - most noise originates at input as first stage of amplifier dominates
  - often refer to Preamplifier = input amplifier
  - may be closest to sensor, subsequently transfer signal further away
- In principle, several possible choices
  - V sensitive
  - I sensitive
  - Q sensitive

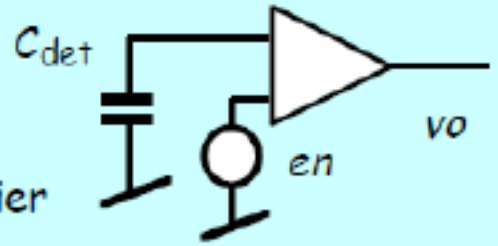
Voltage sensitive amplifier

- As we have seen many sensors produce current signals but some examples produce voltages - thermistor, thermocouple,...

  op-amp voltage amplifier ideal for these

  especially slowly varying signals - few kHz or less

- For sensors with current signals voltage amplifier usually used for secondary stages of amplification



- Signal $V_{out} = Q_{sig}/C_{tot}$

  C_{tot} = *total input capacitance*

  C_{tot} will also include contributions from wiring and amplifier

  V_{out} depends on C_{tot}

  not desirable if C_{det} is likely to vary

  eg with time, between similar sensors, or depending on conditions

- Noise to be discussed more later

  contribution from amplifier, and possibly sensor

  $S/N = Q_{sig}/(C_{tot} \cdot v_{noise})$ can it be optimised?

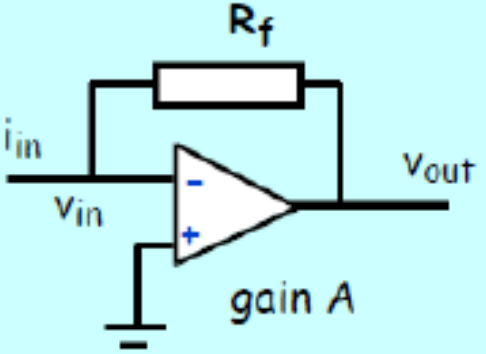
Current sensitive amplifier

- Common configuration, eg for photodiode signals

$v_{out} = -Av_{in}$

$v_{in} - v_{out} = i_{in}R_f$

$v_{out} = -[A/(A+1)].i_{in}R_f \approx -i_{in}R_f$



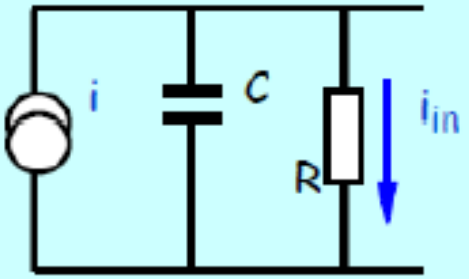
- Input impedance

$v_{in} = i_{in}R_f/(A+1)$ $\quad Z_{in} = R_f/(A+1)$

- Effect of C & R_{in} - consider in frequency domain

$v_0 = i(1/j\omega C||R_{in})$

$= i(\omega)R/(1 + j\omega\tau)$



input signal convoluted with falling exponential

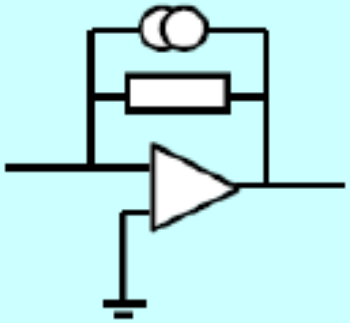
increasing R_f to gain sensitivity will increase τ

fast pulses will follow input with some broadening

- Noise

will later find that feedback resistor is a noise source

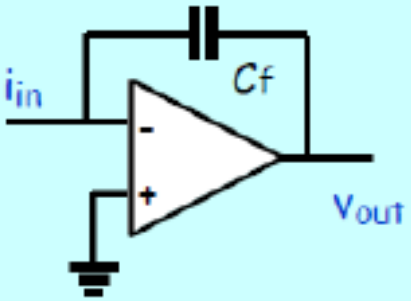
contributes current fluctuations at input ~ $1/R_f$



Charge sensitive amplifier

- Ideally, simple integrator with C_f

  but need means to discharge capacitor - large R_f



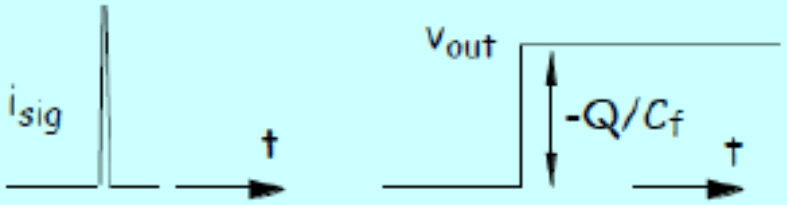
- Assume amplifier has Z_{in} very high (usual case)

$$v_{out} = -Av_{in}$$

$$v_{out} - v_{in} = i_{in}/j\omega C_f$$

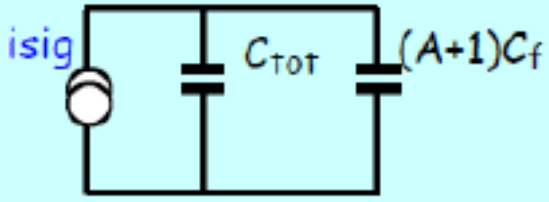
$$v_{out} = -[A/(A+1)].i_{in}/j\omega C_f \approx i_{in}/j\omega C_f$$

$$\Rightarrow -Q/C_f$$



- Input impedance

$$v_{in} = i_{in}/(A+1)j\omega C_f \qquad C=(A+1)C_f \text{ at low f}$$



so amplifier looks like large capacitor to signal source

low impedance but some charge lost

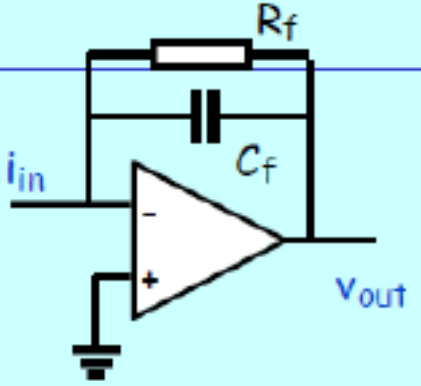
$$Q_A = Q/[1 + C_{tot}/(A+1)C_f]$$

e.g. $A = 10^3$ $C_f = 1pF$

$C_{tot} = 10pF$ $Q_A/Q = 0.99$

$C_{tot} = 100pF$ $Q_A/Q = 0.90$

Feedback resistance



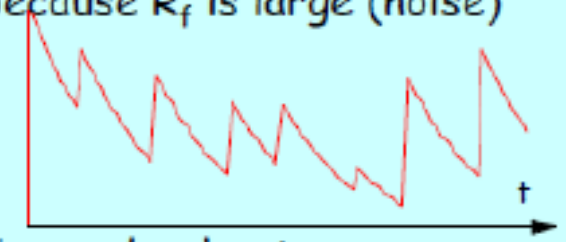
- Must have means to discharge capacitor so add R_f

$Z_f = R_f||1/j\omega C_f$

$v_{out} = -[A/(A+1)].i_{in}Z_f$

$= i(\omega)R_f/(1 + j\omega\tau_f)$ $\quad \tau_f = R_fC_f$

step replaced by decay with ~ $\exp(-t/R_fC_f)$ τ is long because R_f is large (noise)

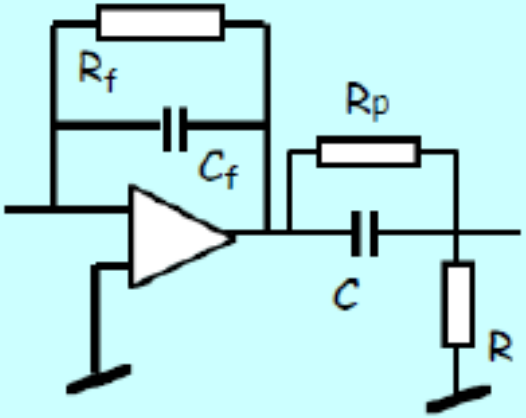


easiest way to limit pulse pileup - differentiate
ie add high pass filter

- Pole-zero cancellation

exponential decay + differentiation => unwanted baseline undershoot

introduce canceling network



$v_0 = 1/(1 + j\omega\tau_f)$

$v_1 = 1/(1 + j\omega\tau_f)(1 + j\omega\tau_1)$

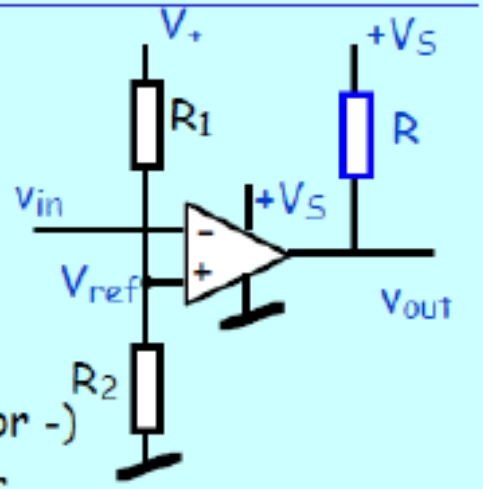
$\tau_1 = RC < \tau_f$

add resistor R_p so $R_pC = \tau_f$

then

$v_1' = 1/(1 + j\omega\tau_3)$ with $\tau_3 = (R||R_n)C < \tau_f$

Comparators



- Frequently need to compare a signal with a reference
  - eg temperature control, light detection, DVM,...
  - basis of analogue to digital conversion -> 1 bit
- Comparator
  - high gain differential amplifier,
    - difference between inputs sends output to saturation (+ or -)
  - could be op-amp - without feedback - or purpose designed IC
  - Sometimes ICs designed with open-collector output so add pull-up R to supply
    - also available with latch (memory) function
- NB
  - no negative feedback so $v_- \neq v_+$
  - saturation voltages may not reach supply voltages - check specs
  - speed of transition
- Potential problem
  - multiple transitions as signal changes near threshold

Hysteresis

- Add positive feedback (Schmitt trigger)

  V_{ref} changes as v_{out} -> $+V_S$

  ie threshold falls once transition is made

  preventing immediate fall

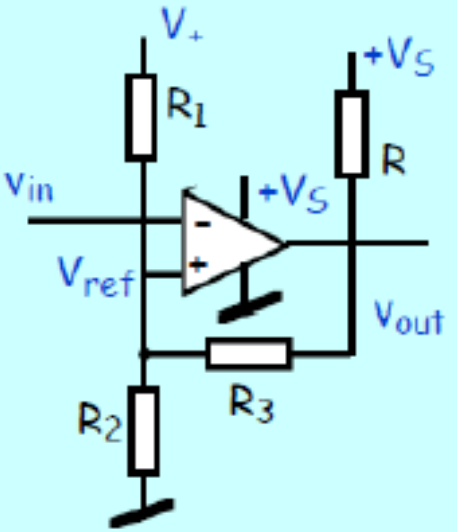
  positive feedback speeds transition

  $v_{out} = A(V_{ref} - v_-)$

  $V_{ref} > v_-$ => $v_{out} = V_s$ $V_{ref} = V_{high}$

  $V_{ref} < v_-$ => $v_{out} = 0V$ $V_{ref} = V_{low}$

  here, signal => logical "1": $v_{out} = 0V$



- Output depends on history

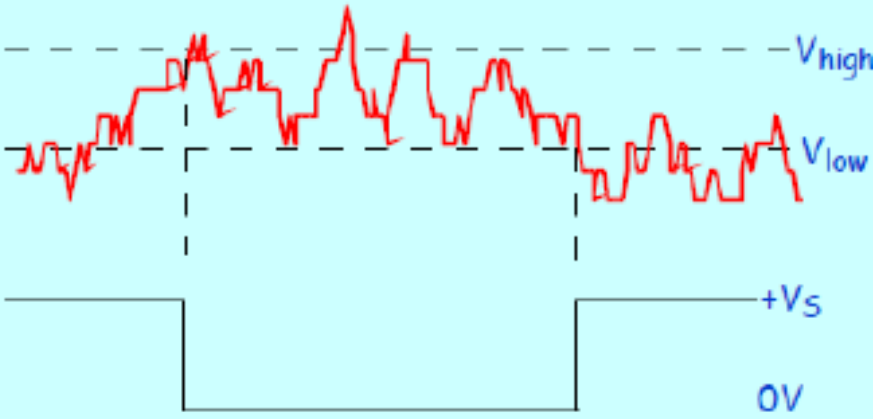
  eg $V_+ = 10V$, $V_S = +5V, 0V$

  $R_1 = 10k\Omega$, $R_2 = 10k\Omega$, $R_3 = 100k\Omega$

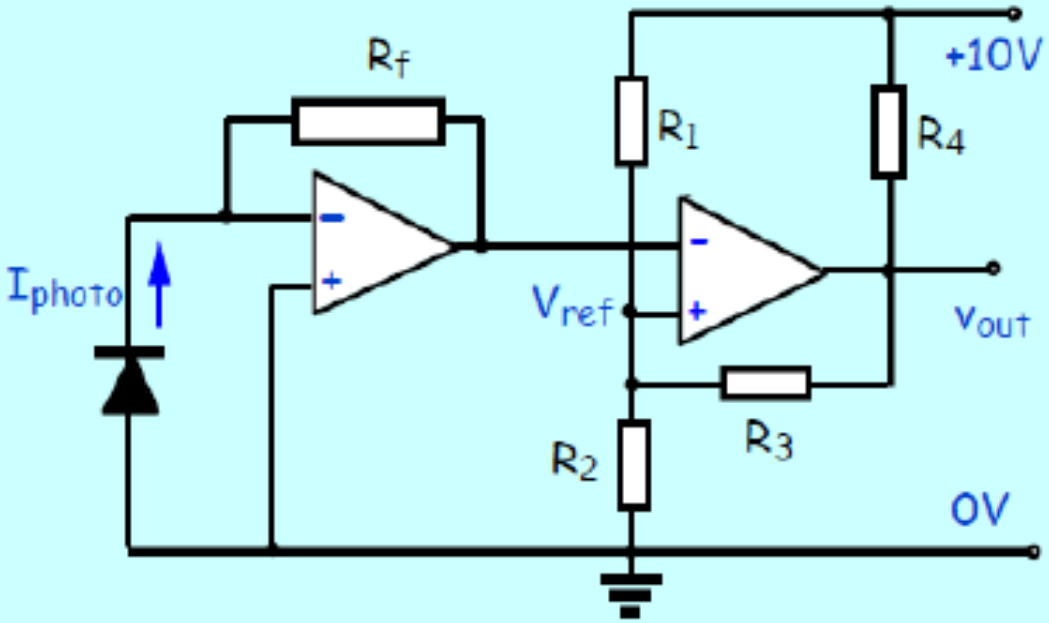
  $V_{out} = 0V$, $V_{ref} = 4.76V$

  $V_{out} = 5V$, $V_{ref} = 5V$

  hysteresis = $\Delta V_{ref} = 0.24V$



Example - alarm



Digital electronics

- Explosive growth over 10-20 years - now dominates applications, still growing…
  - computing
  - communications: mobile/fixed phones, radio, data links,…
  - other: digital audio, consumer goods,…
- Why?
  - binary logic
  - almost complete noise immunity
  - high speed, still increasing
    - *Ethernet: ~Gb/s, phones, links: >Gb/s, computing ~GHz*
  - ease of use
    - *many analogue functions now easier to implement by digital summation, etc*
  - availability
    - *basic logic to complete IC assemblies of big range of complex functions*
- Bits, Bytes & Words
  - byte = 8 bits word: usually multiple of bytes 8, 16, 32, 64 bits

Basic logic

- bits can be represented in several ways, almost invariably voltage

  0/1: Low/High (voltage level) … or High/Low

  values and range depend on families, most common are…

- TTL (bipolar) Transistor-Transistor Logic

  usually V_S = 0 to +5V

  V_T ~ 1.5V ΔV ~ 1V

  outputs & inputs sink/source currents

  not identical levels

- *CMOS* - now most common

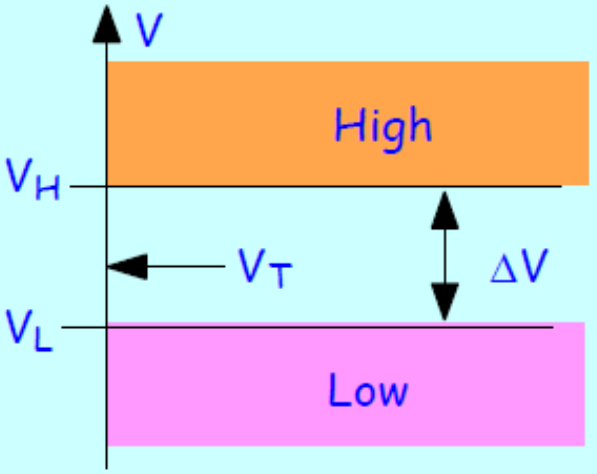
  V_S = 0 to +5V but +12V, +3.5V and lower

  V_T ~ V_S /2 ΔV ~ 0.4 V_S

  outputs swing between supplies

- ECL Emitter Coupled Logic

  high speed, but power hungry



designs must tolerate variations

- component manufacture
- operating temperature
- supply voltage
- loading
- noise

September 27, 2012

LECTURE-10

Logic gates

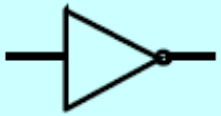
- Logical functions, described by truth table

  define output for inputs A & B use High = 1

- NOT (Inverter)

  $\overline{A}$ or A'

A	out
1	0
0	1



- OR

A+B

A	B	out
1	1	1
1	0	1
0	1	1
0	0	0

NOR

(A+B)'

A	B	out
1	1	0
1	0	0
0	1	0
0	0	1

XOR exclusive OR

$A \oplus B$

A	B	out
1	1	0
1	0	1
0	1	1
0	0	0

- AND

A.B
or AB

A	B	out
1	1	1
1	0	0
0	1	0
0	0	0

NAND

(AB)'

A	B	out
1	1	0
1	0	1
0	1	1
0	0	1

multiple inputs are often allowed, eg

Negative-true logic

- What if - instead of High = 1 - we choose Low = 1?

  equivalent functions but different symbols

- NOT 

- OR  NOR  XOR 

- AND  NAND 

it may be easier to think in terms of High & Low, eg...

Negative-true

A	B	A′	B′	A′.B′	Q
L	L	H	H	H	L
L	H	H	L	L	H
H	L	L	H	L	H
H	H	L	L	L	H

OR

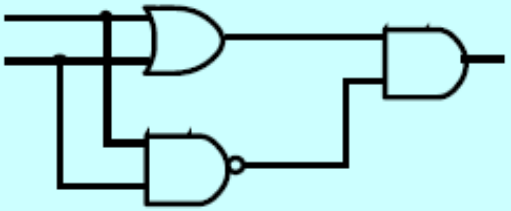
A	B	Q
L	L	L
L	H	H
H	L	H
H	H	H

Which gates are needed?

- Logic functions can be constructed from other combinations

eg XOR

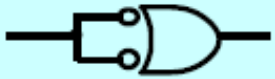
start from OR, change...



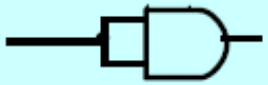
A	B	OR
1	1	1
1	0	1
0	1	1
0	0	0

A	B	XOR
1	1	0
1	0	1
0	1	1
0	0	0

- A couple of examples...



what purpose could they serve?



- Several simple theorems of logic help to do translations if needed (see H&H)

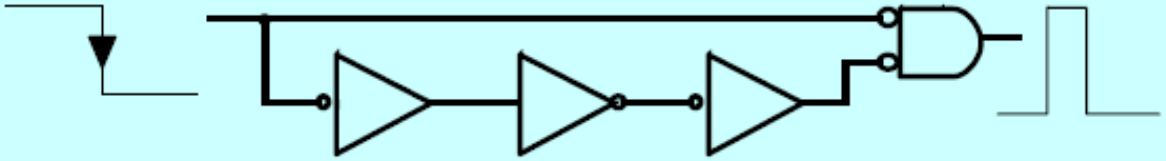
DeMorgan's: Not(A+B) = NotA.NotB

Not(A.B) = NotA + NotB

NotA = A' = $\overline{A}$

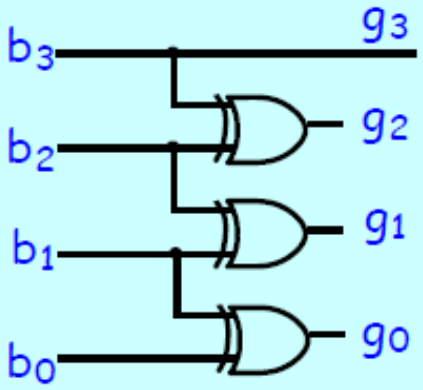
A few applications

- Pulse on falling edge



- Gray coding

binary	Gray
0000	0000
0001	0001
0010	0011
0011	0010
0100	0110
0101	0111
0110	0101
0111	0100
...	



in Gray code, only 1 bit changes between states

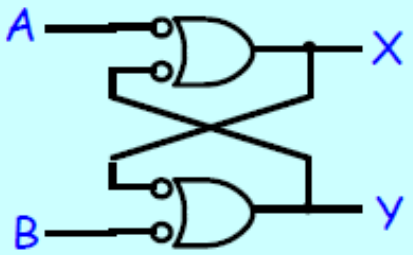
eg, valuable for controlling stepping motors

simplifying logic sequences

Memory - the Flip-flop

- Work out the truth table

A	B	X	Y
L	L	H	H
L	H	H	L
H	L	L	H
H	H	L	H
H	H	H	L



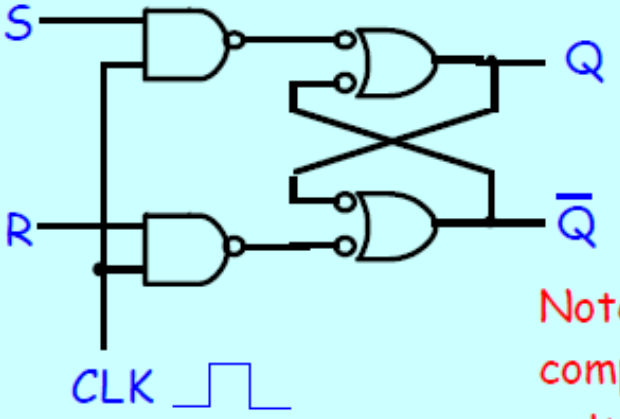
Note the symmetry

so the state depends on the previous history of the flip-flop

- Clocked flip-flop

if CLK = L, state is maintained

S	R	Q_{n+1}
L	L	Q_n
L	H	L
H	L	H
H	H	-



Note the complementary outputs

why is HH output undefined?

- We now have a memory device with Set & Reset, which runs sequentially

D and JK flip flops

- even the clocked flip-flop is not quite sufficient

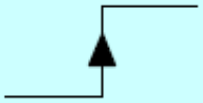
  can't guarantee inputs will not change during clock high

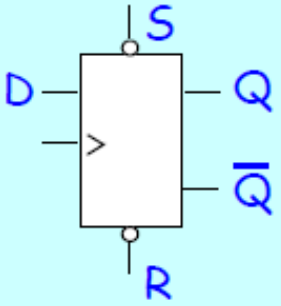
  the solutions are Master-Slave and edge triggered D flip-flops

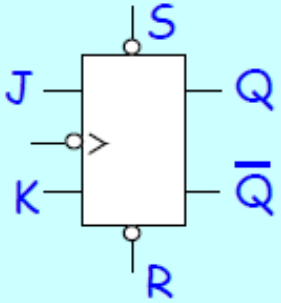
- D-type flip-flop

  transmits value at Data input to Q, on clock edge

  both positive and negative edge types available







J	K	Q_{n+1}
L	L	Q_n
L	H	L
H	L	H
H	H	Q_n'

- JK flip-flop - two data inputs

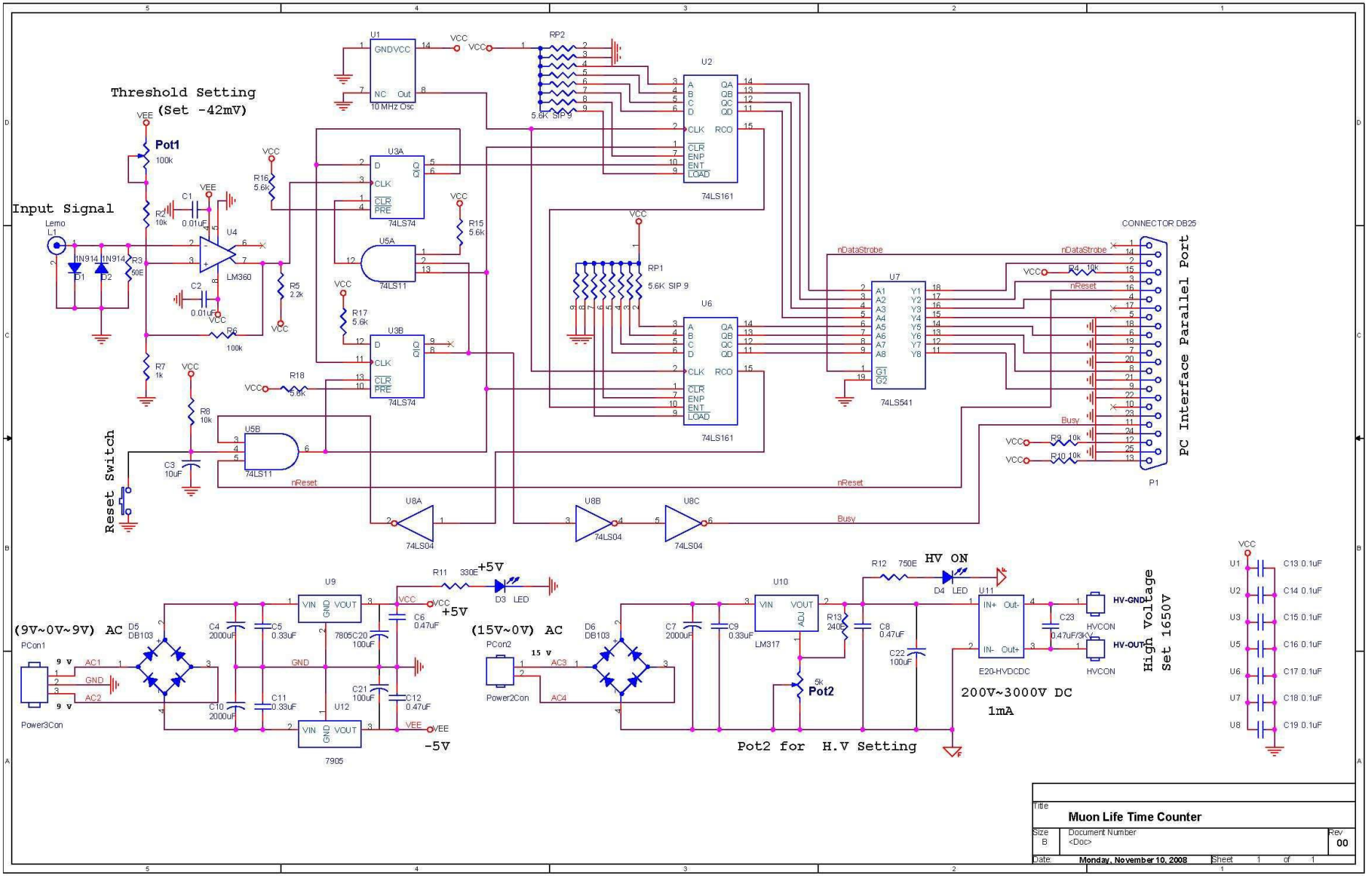
  both low: unchanged

  both high: complement of last state

  complementary data: output follows J input

> symbol = edge

o> = negative going edge

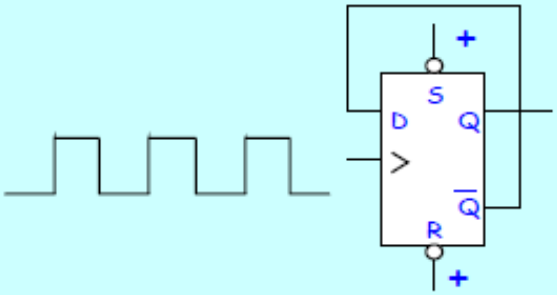

Threshold Setting
(Set -42mV)
Input Signal
Lemo
Pot1
100k
1N914
1N914
LM360
74LS74
74LS11
74LS161
74LS541
74LS04
10 MHz Osc
5.6K SIP 9
CONNECTOR DB25
PC Interface Parallel Port
nDataStrobe
nReset
Busy
Reset Switch
(9V~0V~9V) AC
(15V~0V) AC
+5V
-5V
7905
7805C20
LM317
HV ON
D4 LED
D3 LED
E20-HVDCDC
HVCON
HV-GND
HV-OUT
200V~3000V DC
1mA
High Voltage
Set 1650V
Pot2
Pot2 for H.V Setting
Power3Con
Power2Con
DB103
Muon Life Time Counter
Monday, November 10, 2008

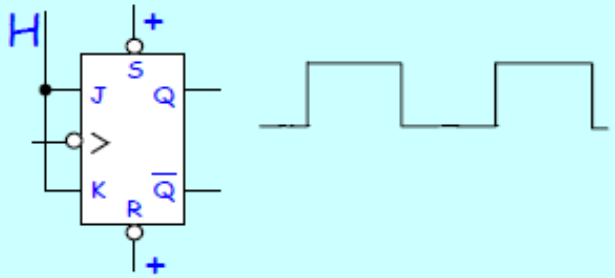
October 23, 2012

LECTURE-11

Examples

- Divide clock frequency by 2



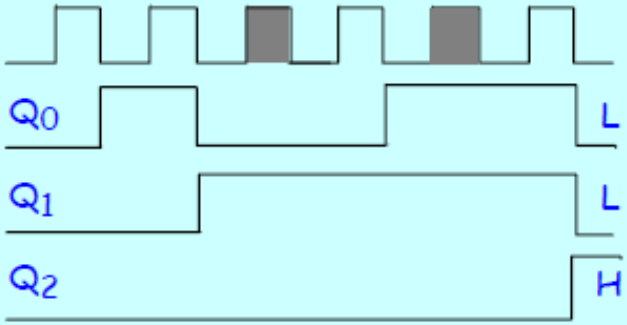


- n-bit Counter

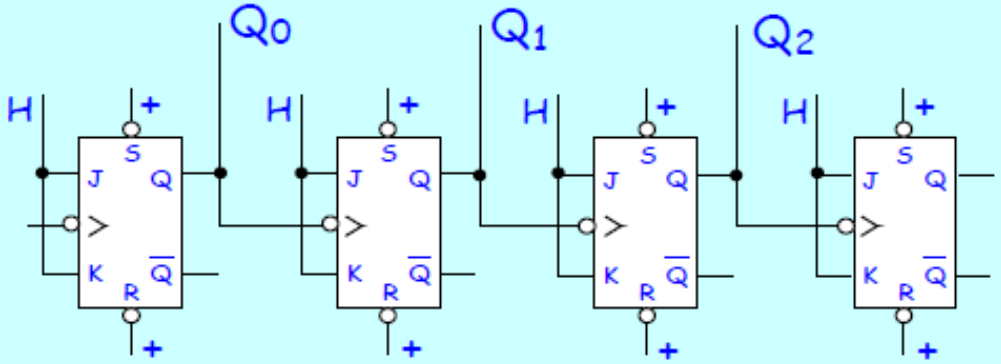
set all Q_i = L

output changes on negative edge

follow outputs



LSB



output = HLL = 100_2 = 4

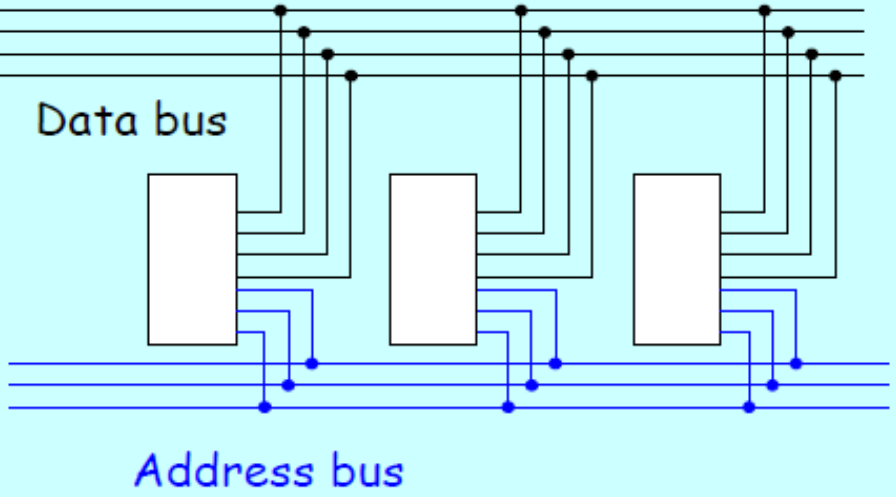
Tri-state logic

- In some applications there is a need to connect to a "bus"
- Bus

  series of parallel lines shared

  between multiple devices

  typically 8-bit, 16-bit, 32-bit,..



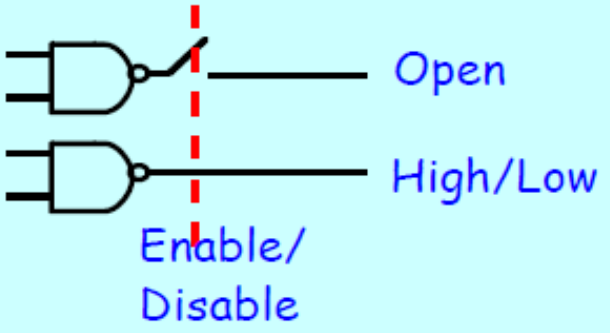
- but if all devices are connected to the bus... who has priority?

  potential recipe for confusion

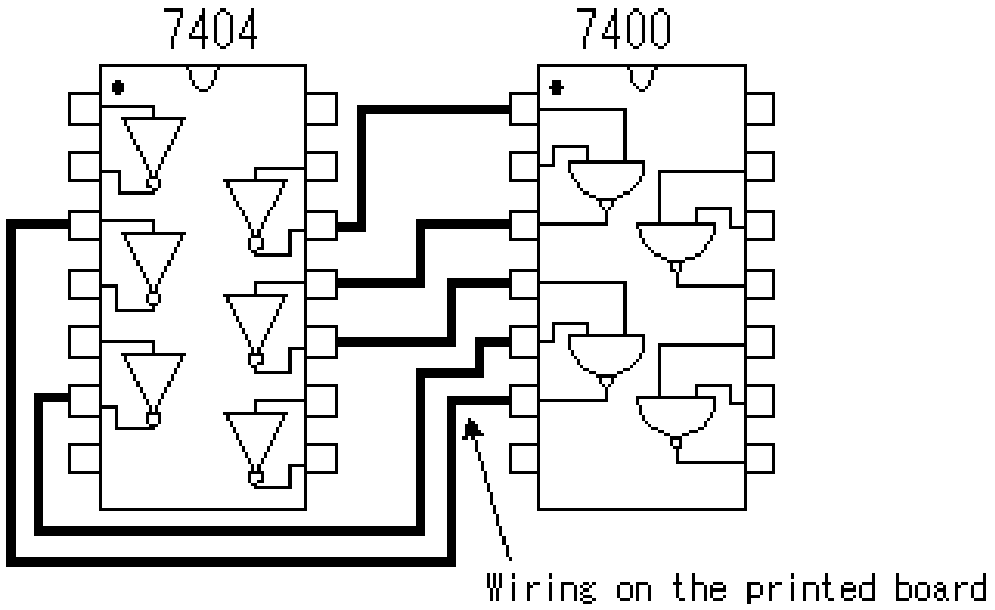
- Solution, third logic state: "open circuit"

  ie HIGH, LOW and "OPEN"

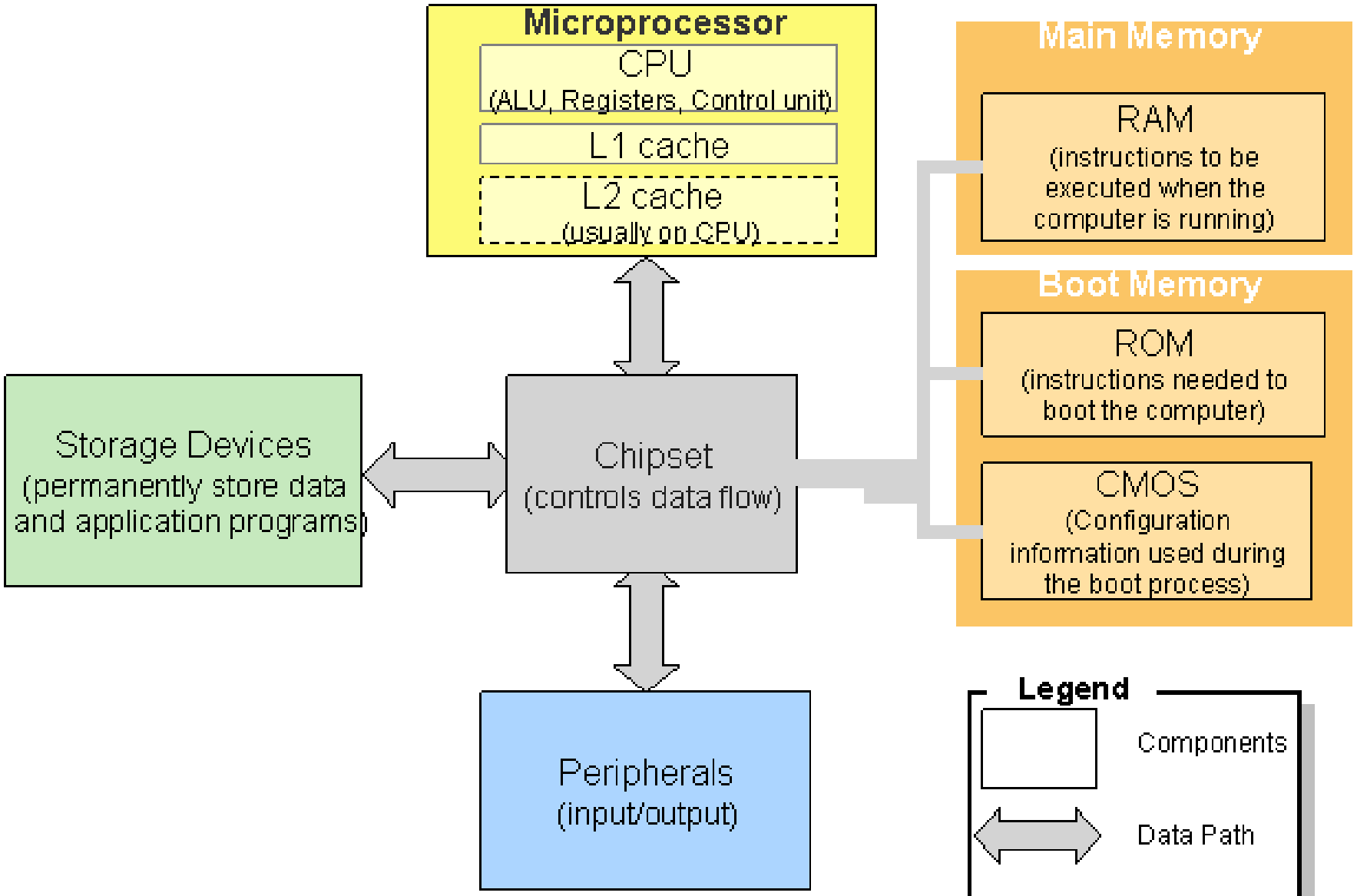
  controlled by additional input: Enable



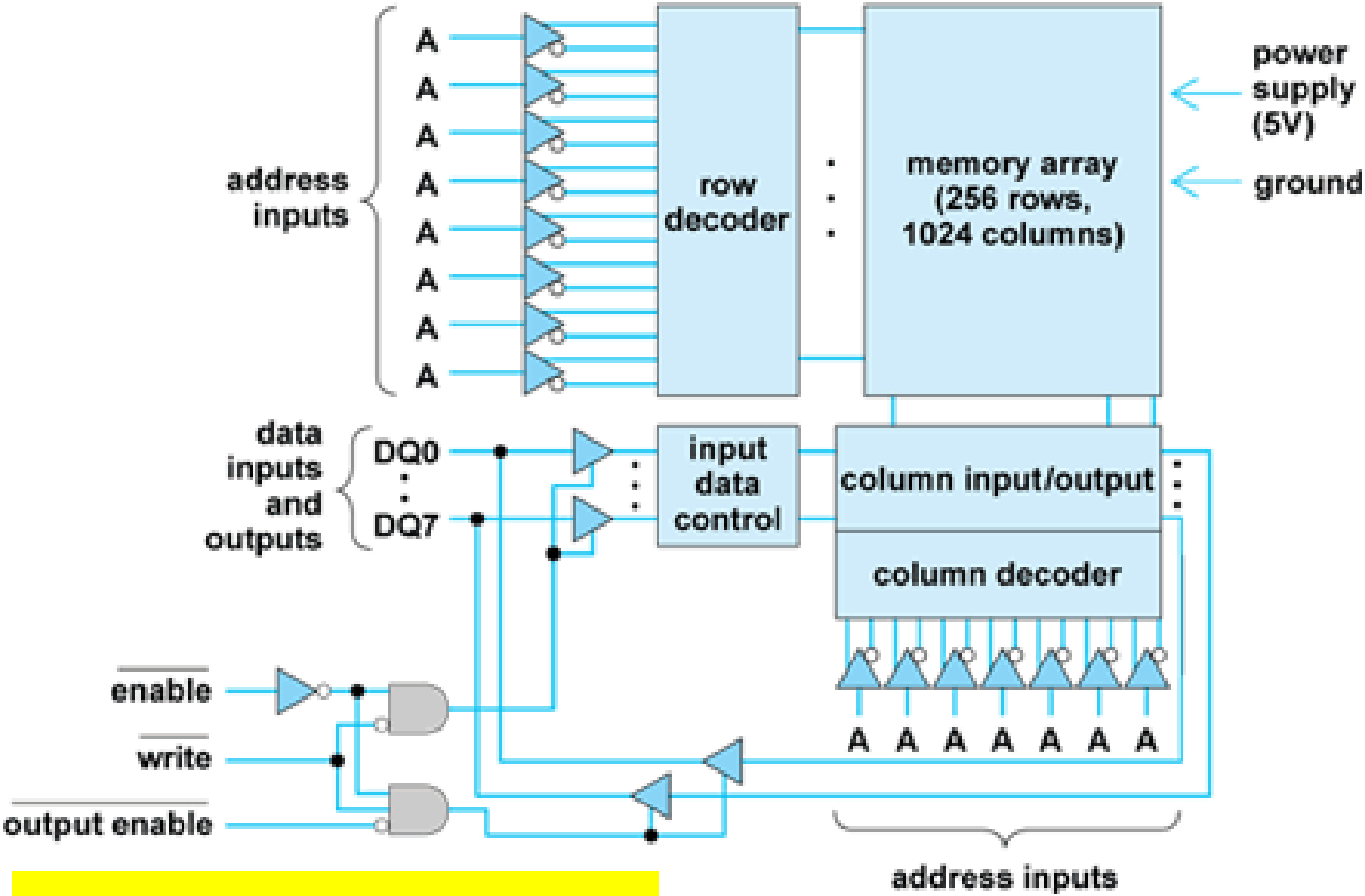
Discrete digital circuits



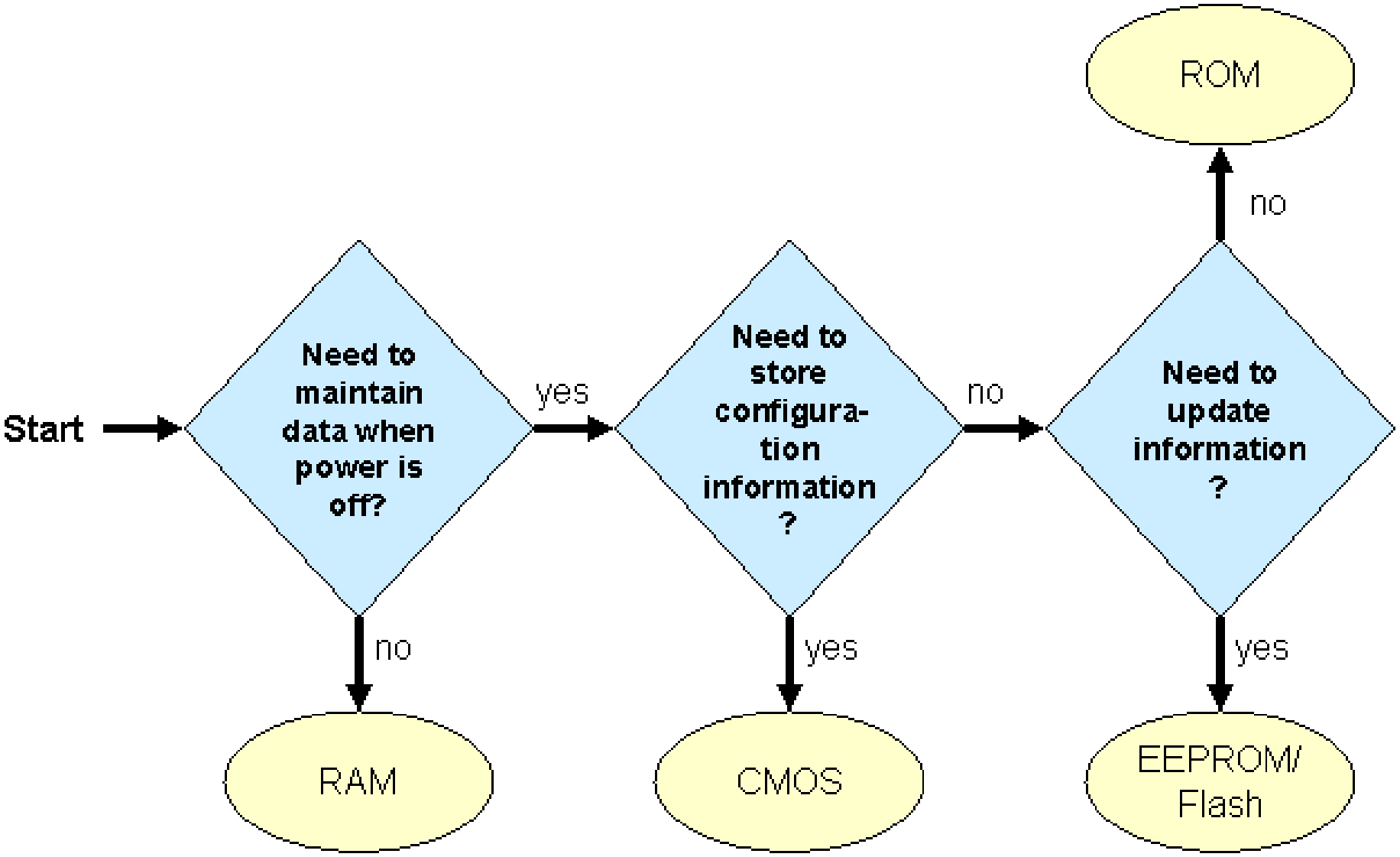
For example, in case of the 7400 IC, 4 circuits of 2 input NAND gate are housed. In case of 7404, 6 circuits of inverter are housed. These are separate ICs. Therefore, to compose a circuit, it is necessary to do each wiring among the pins using the printed board.



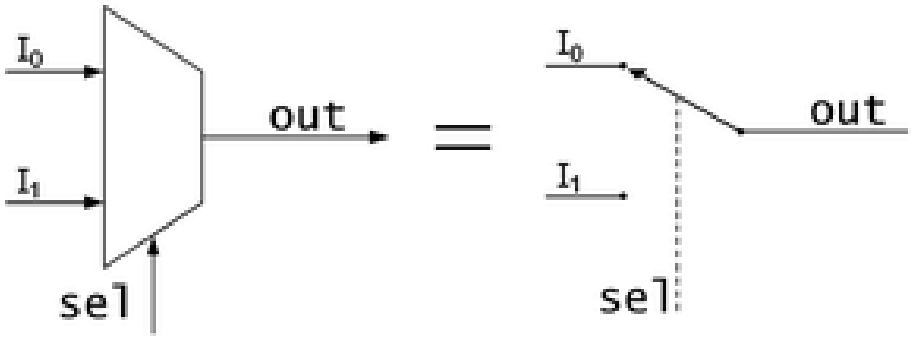
Typical computer system

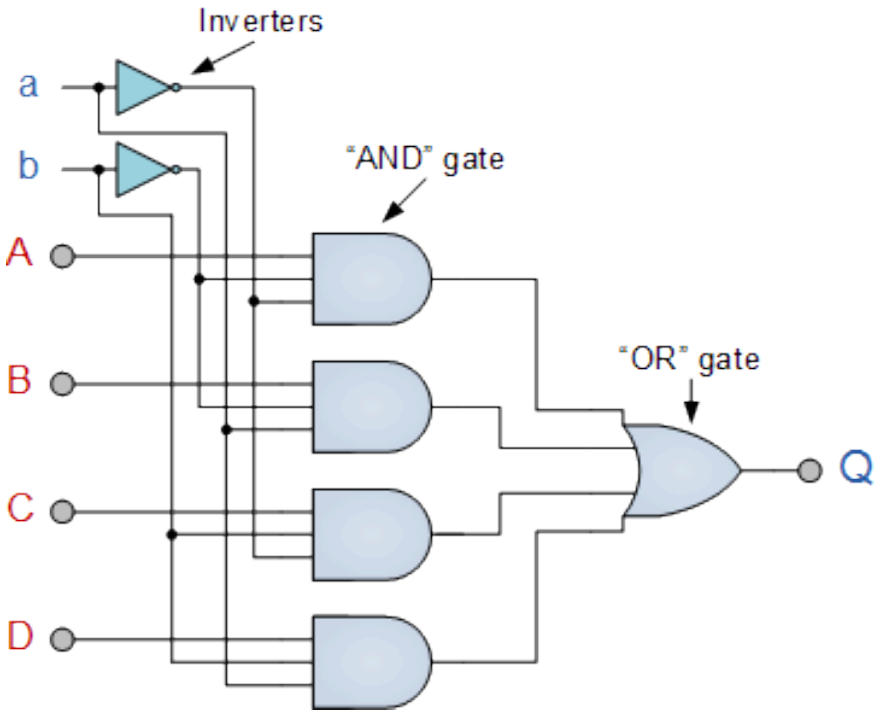


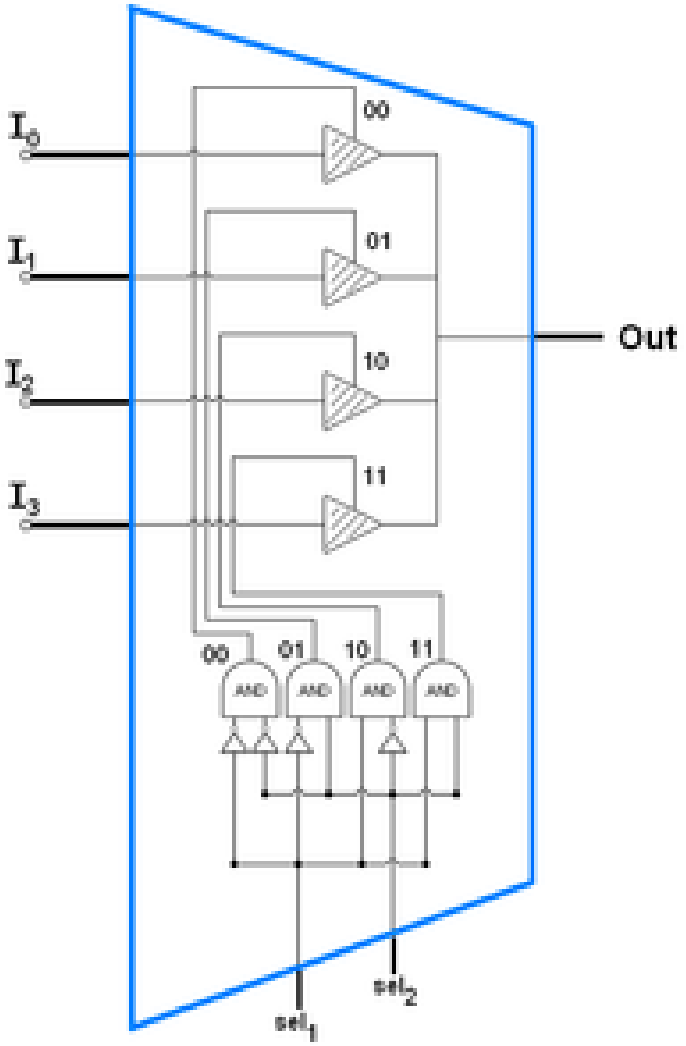
Memory organisation


Start
Need to maintain data when power is off?
yes
Need to store configura-tion information ?
no
Need to update information ?
no
ROM
no
RAM
yes
CMOS
yes
EEPROM/ Flash

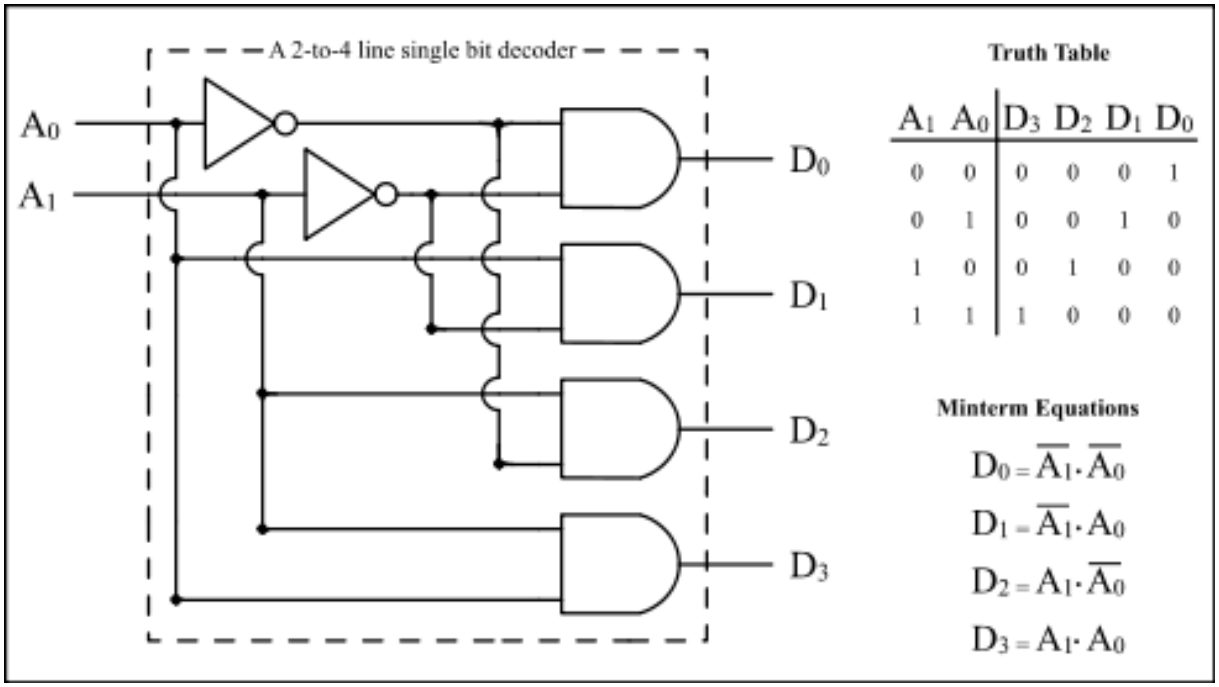
Multiplexer







Decoder



Truth Table

A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Minterm Equations

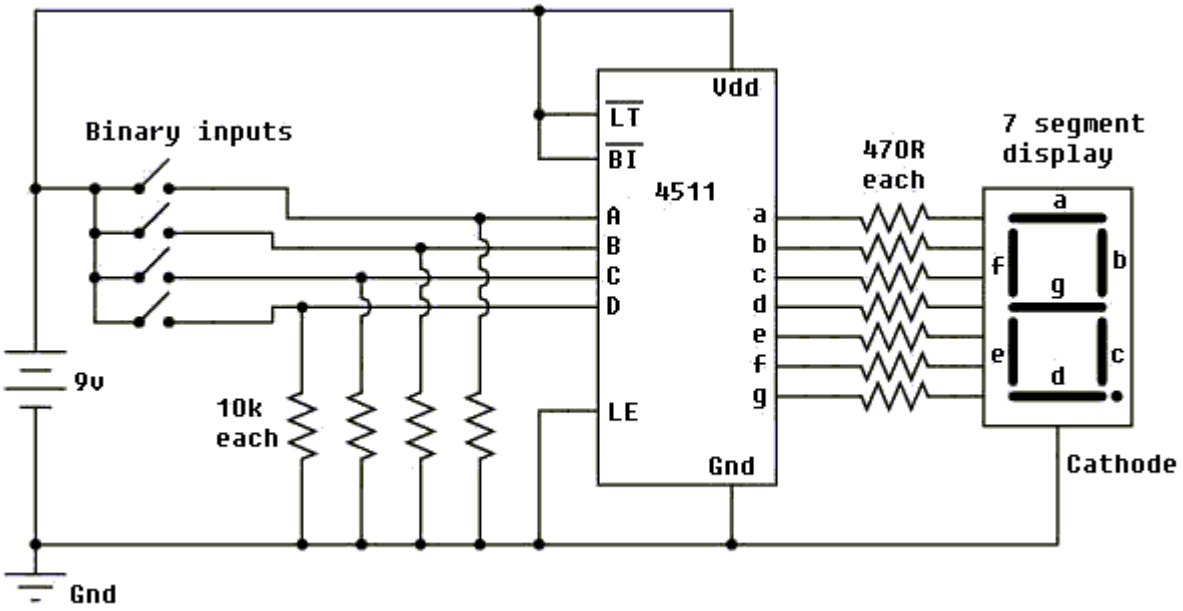
$D_0 = \overline{A_1} \cdot \overline{A_0}$

$D_1 = \overline{A_1} \cdot A_0$

$D_2 = A_1 \cdot \overline{A_0}$

$D_3 = A_1 \cdot A_0$

Example application



October 25, 2012

LECTURE-12

Monostable Multivibrator/ Single Shot multivibrators

As the name indicates, Monostable Multivibrators having only single Stable State and the other is QUASI stable state.

1. Positive edge Triggered
2. Negative edge Triggered
3. Level Triggered

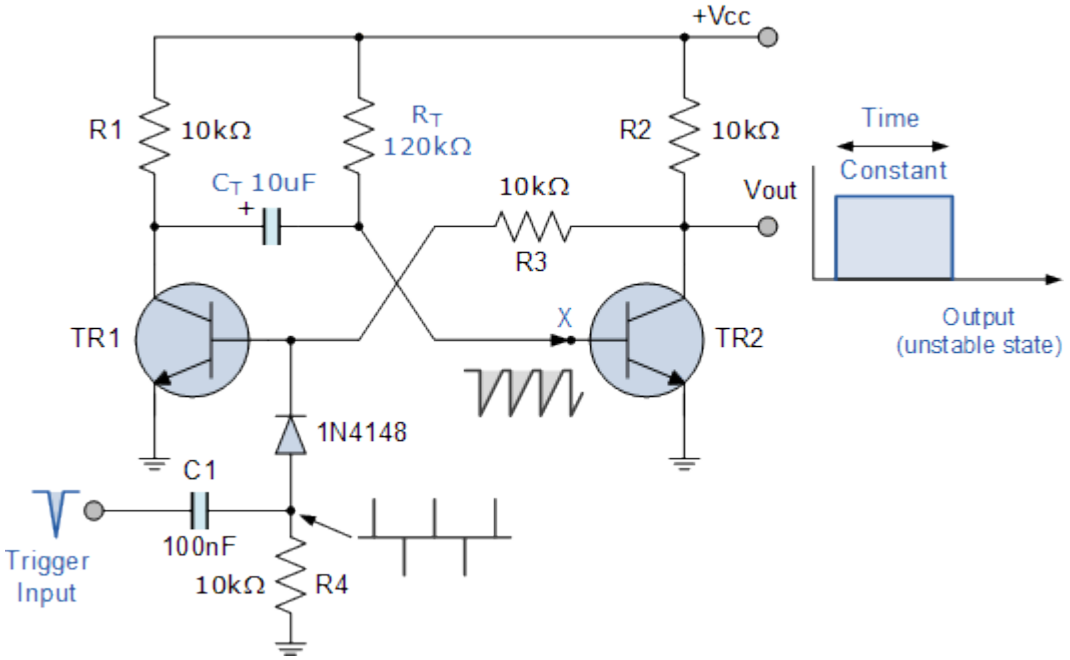
By giving an input trigger the monostable/ single shot multivibrator generates an output voltage corresponding to the time predetermined by the circuit elements (RC network).

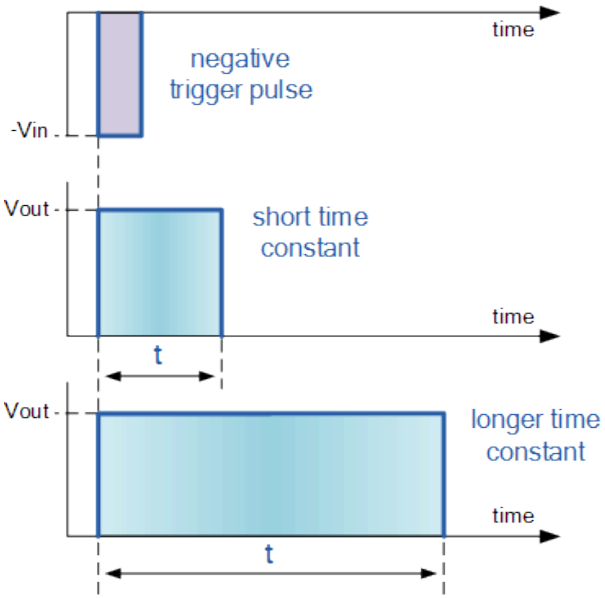
ie; The output wave extends as long as the time constant determined by RC network and come back to its reference position.

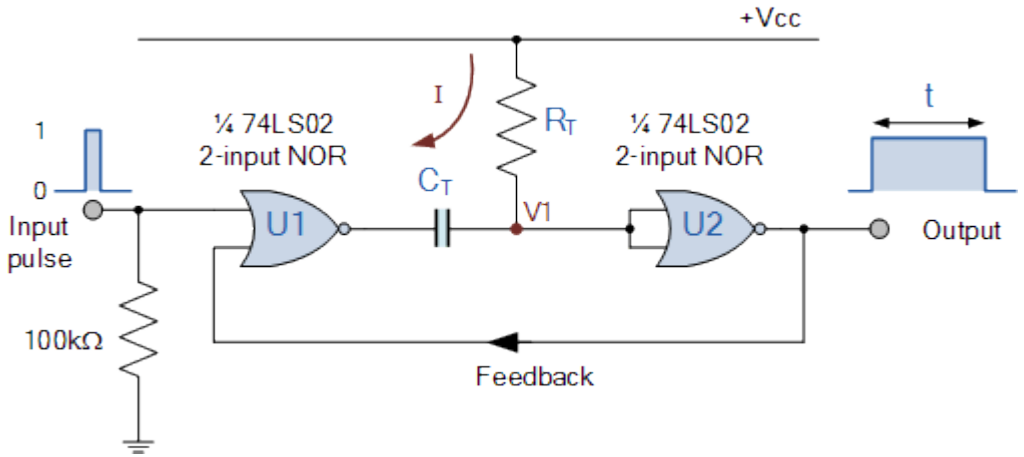
So Monostable Multivibrator produce a Single Shot of output voltage for a trigger pulse. If their is no trigger, the output voltage will be zero.

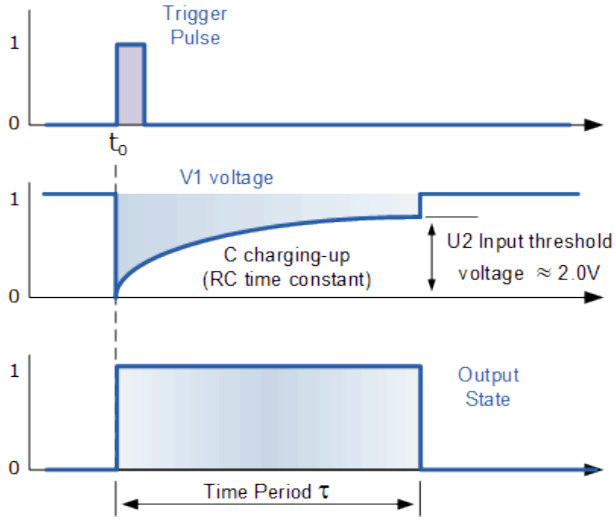
In monostable multivibrator, the HIGH state is called QUASI STABLE state because, it is not stable in output waveform. ie; the output will returns to LOW state after the time t.

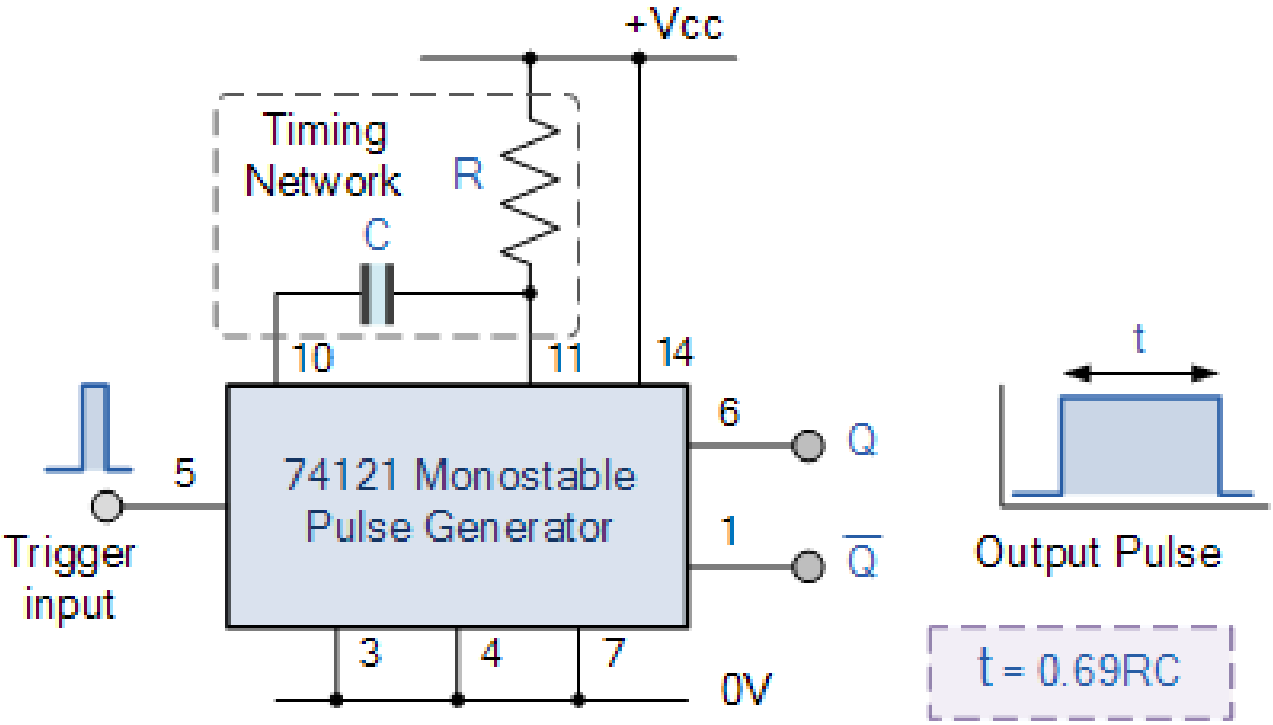
Monostable multivibrator





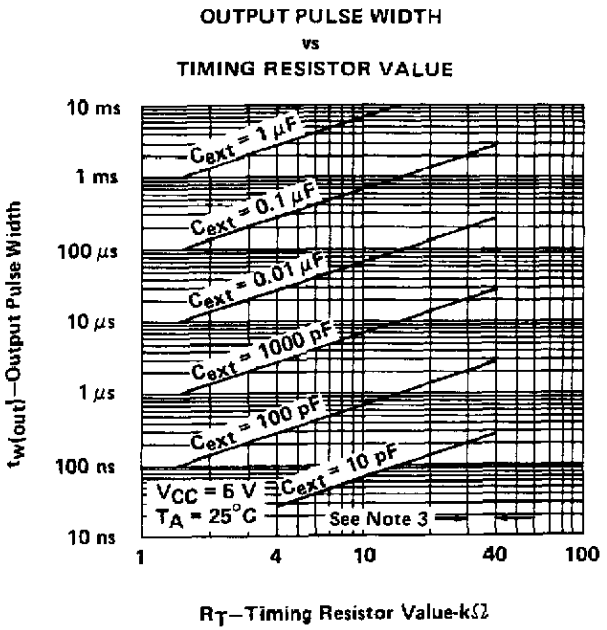






FUNCTION TABLE

INPUTS			OUTPUTS	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⊓	⊓
↓	H	H	⊓	⊓
↓	↓	H	⊓	⊓
L	X	↑	⊓	⊓
X	L	↑	⊓	⊓

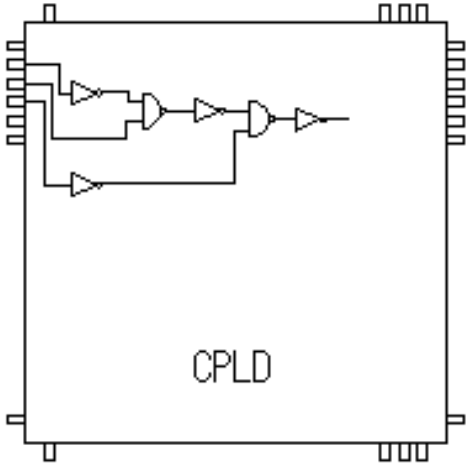


Programmable logic

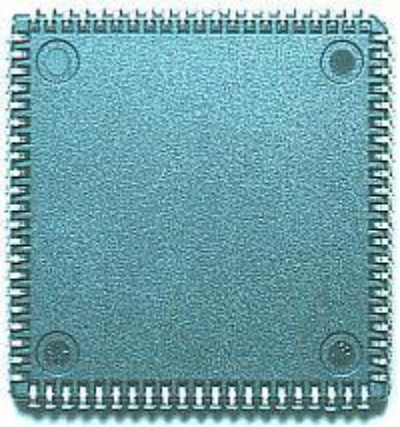
- For very complex logic, it's time consuming and risky to develop circuits
  programmable logic solves both problems
- PLA programmable logic array
  transistor array with connections set by fuses to burn
- FPGA field programmable gate array
  MOS array of uncommitted gates - few k to several M
  connections made by downloading code which sets biasing of circuits
  fully re-programmable
- DSP digital signal processor
  cut-down microprocessor with limited instruction set

- Various levels of complexity and skills to learn
  eg 2M gate FPGA needs sophisticated design and simulation software

What is a CPLD?



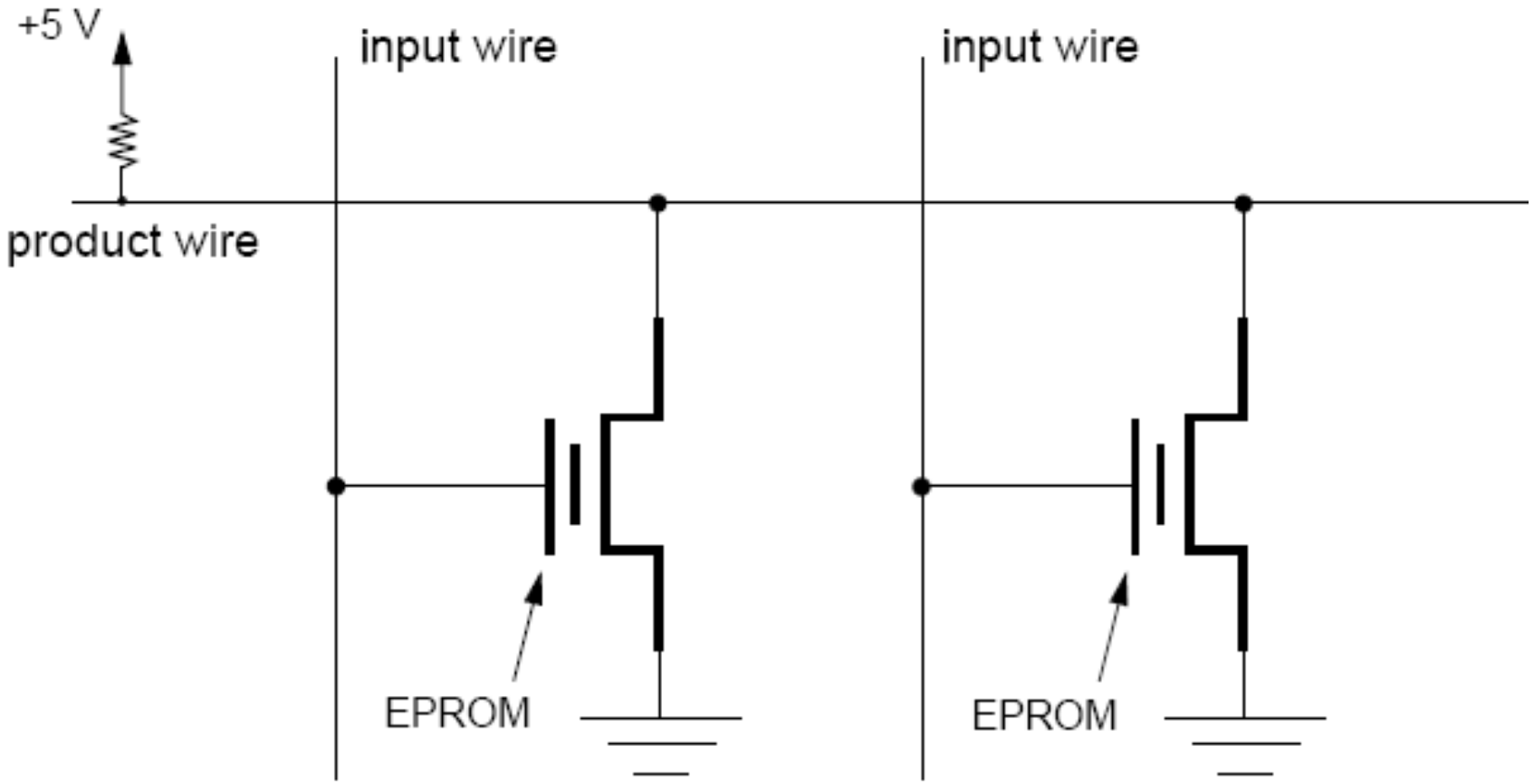
Top side



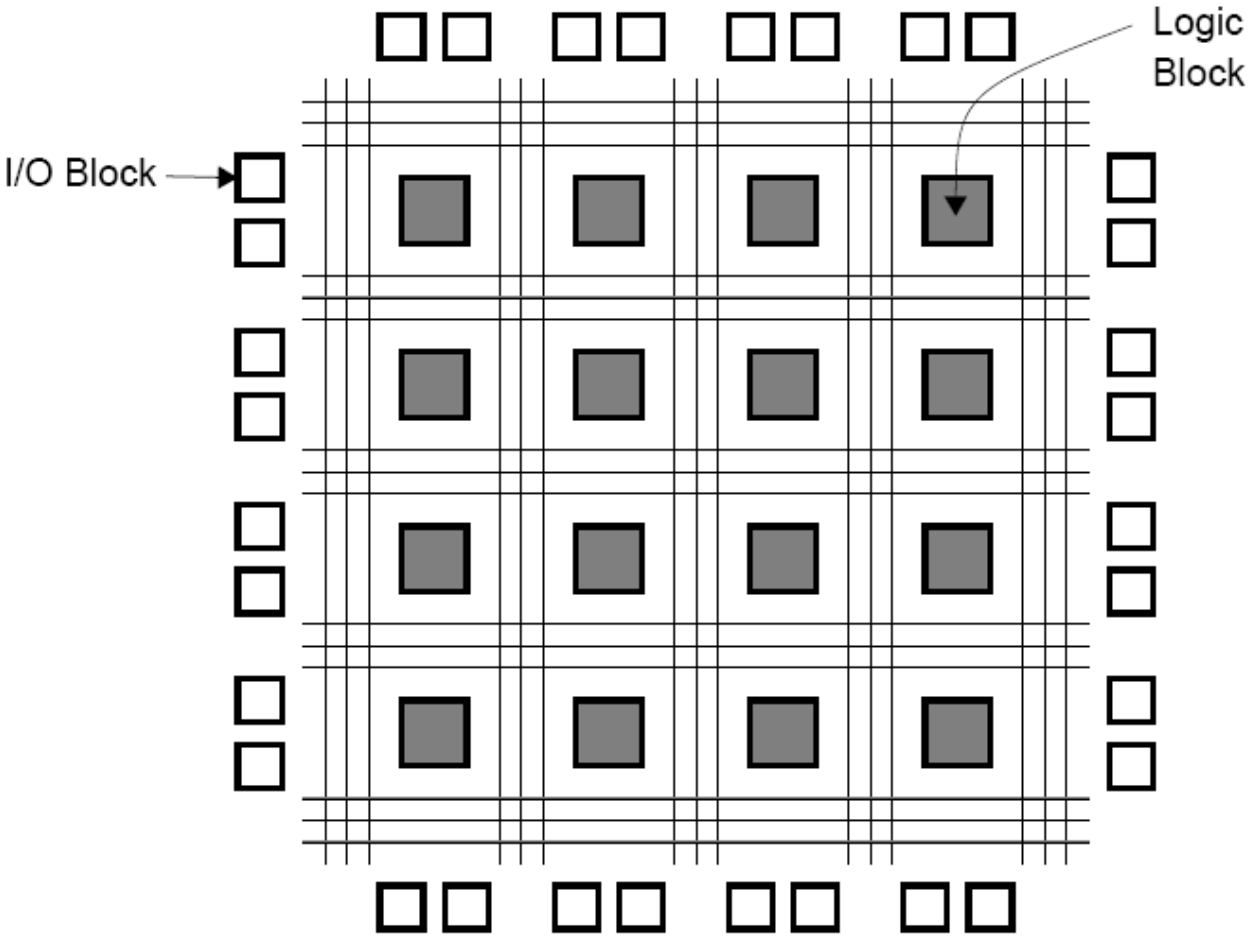
Bottom side

- In case of CPLD, it has wiring among the logic in the IC. So, the wiring on the printed board can be made little.
- A lot of logic devices are housed in CPLD and those connections can be specified by the program.
- The capacity of CPLD is limited. There is limitation on the number of the pins, too.
- It is possible to rewrite CPLD many times because it is recording the contents of the circuit to the flash memory.
- In-situ programming of the chip possible.

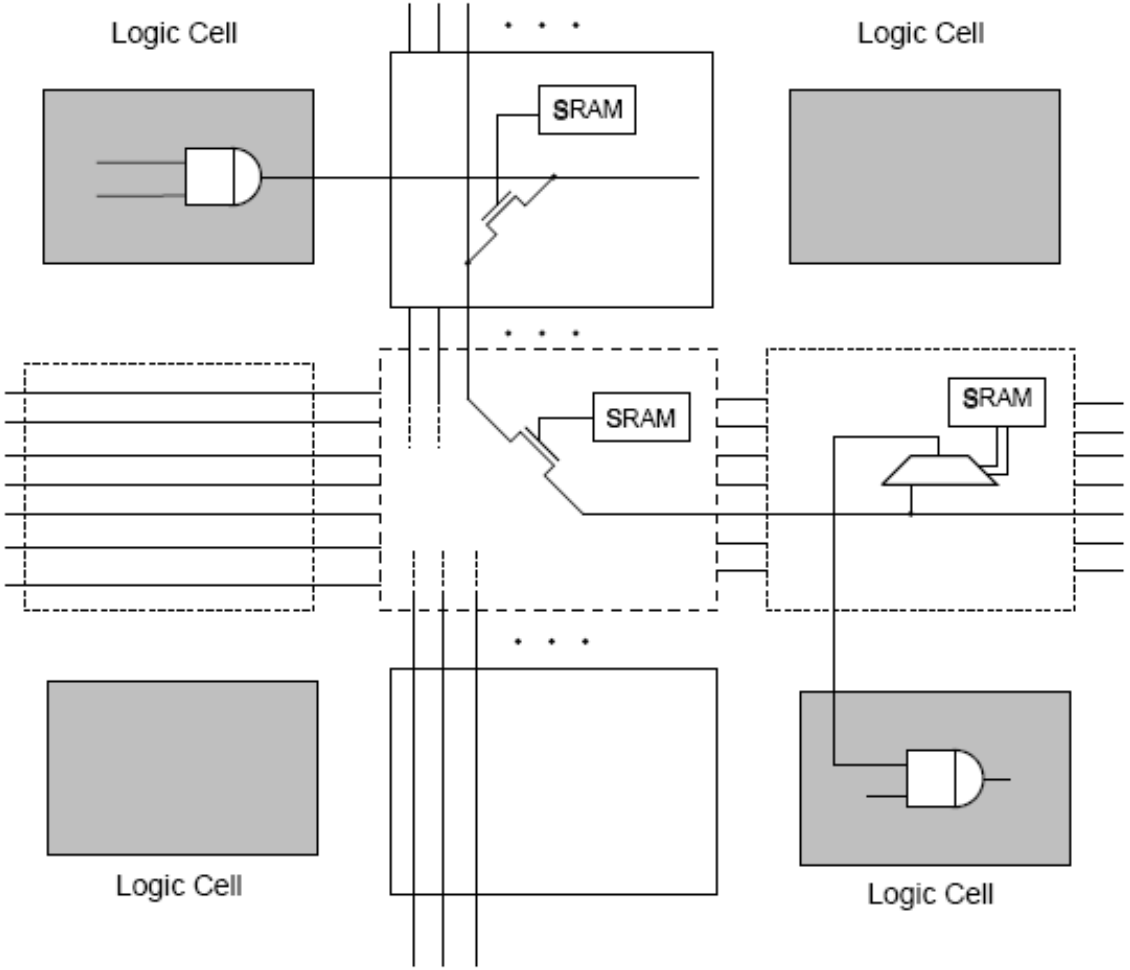
EPROM programmable switches



Structure of a FPGA

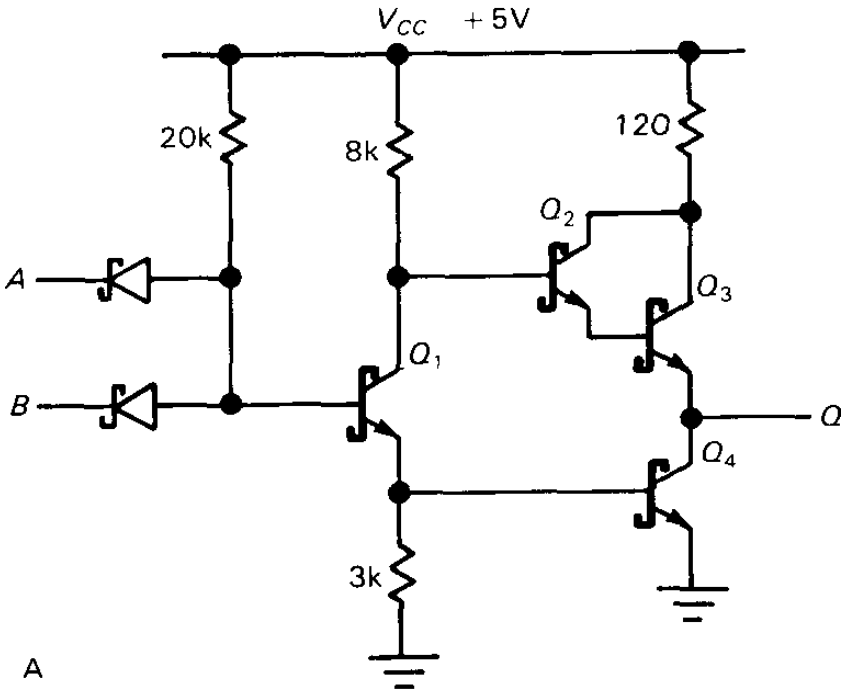


SRAM controlled programmable switches

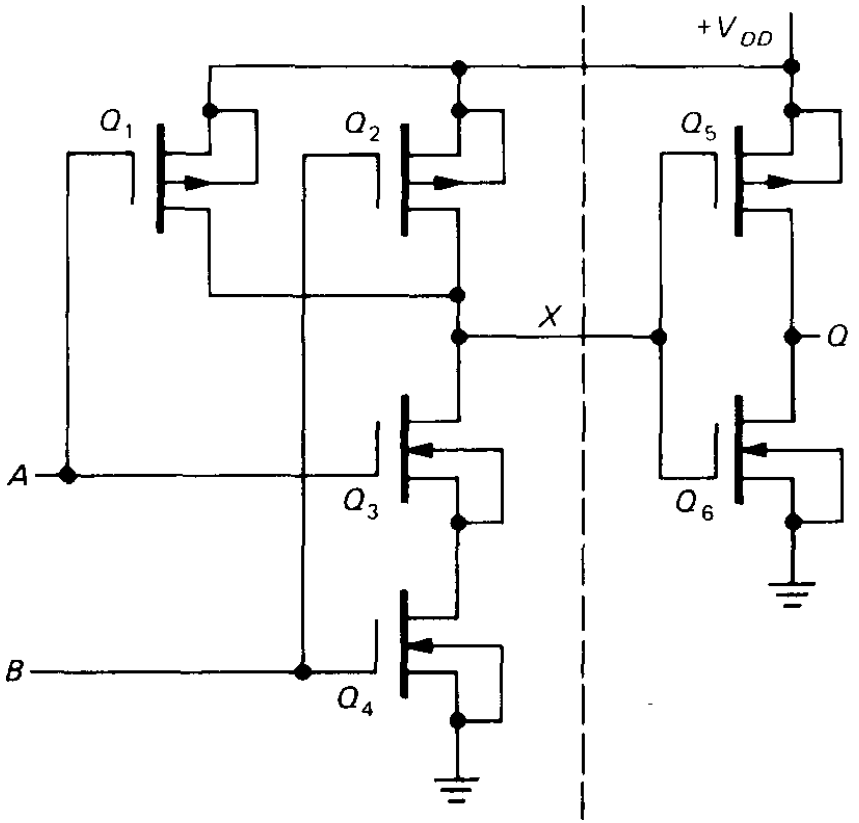


TTL AND CMOS

TTL (transistor-transistor logic) and CMOS (complementary MOS) are the two most popular logic families in current use.



TTL NAND gate



CMOS AND gate.

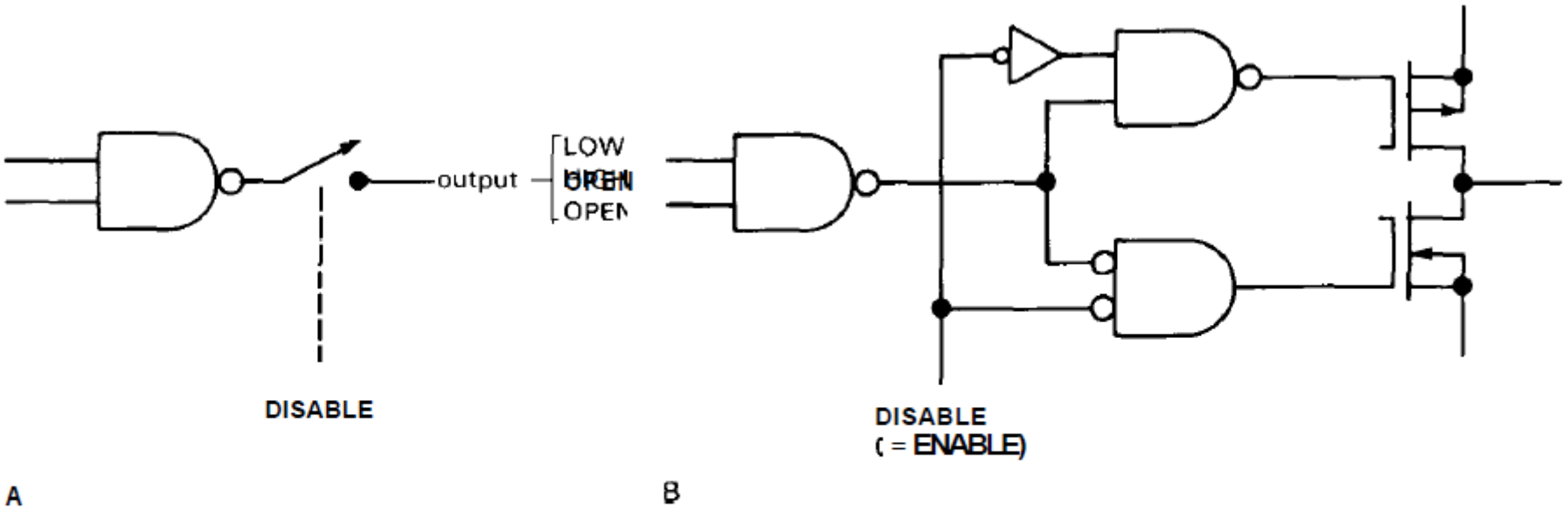
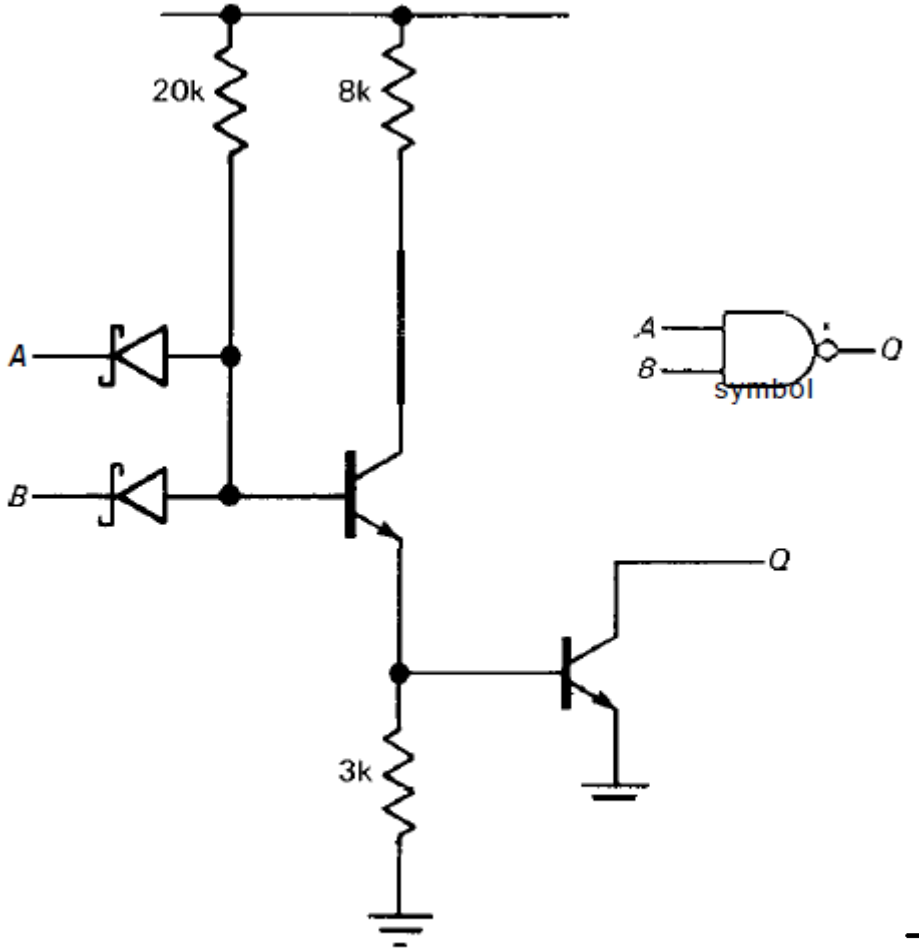
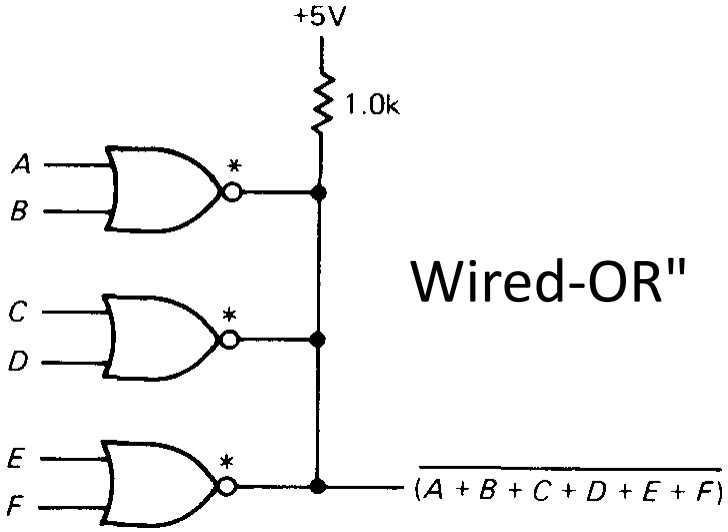
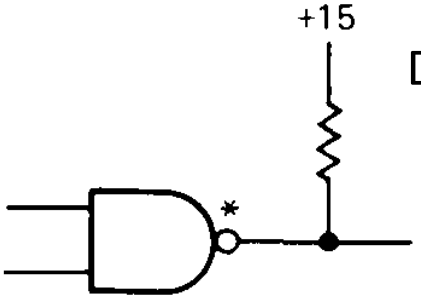


Figure 8.19. Three-state **CMOS** NAND gate.
A. Conceptual diagram.
B. Realization with internal **CMOS** gates.





Wired-OR"



Driving external loads

Figure 8.21. LS TTL open-collector NAND.

TTL and CMOS characteristics

- Supply voltage: TTL families require +5 volts, whereas the CMOS families have a wider range: +2 to +15 volts

- Input: A TTL input held in the LOW state sources current into whatever drives it , so to pull it LOW you must sink current. Since the TTL output circuit is good at sinking current, this presents no problem when TTL logic is wired together, but you must keep it in mind when driving TTL with other circuitry. By contrast, CMOS has no input current.

TTL and CMOS characteristics

- The TTL input logic threshold is about two diode drops above ground (about 1.3V), whereas most CMOS families have their threshold nominally at half the supply voltage. The HCT and ACT CMOS families are designed with a low threshold similar to bipolar TTL for compatibility, since a bipolar TTL output does not swing all the way to +5 volts.

- CMOS inputs are susceptible to damage from static electricity during handling. In both families, unused inputs should be tied HIGH or LOW, as necessary

TTL and CMOS characteristics

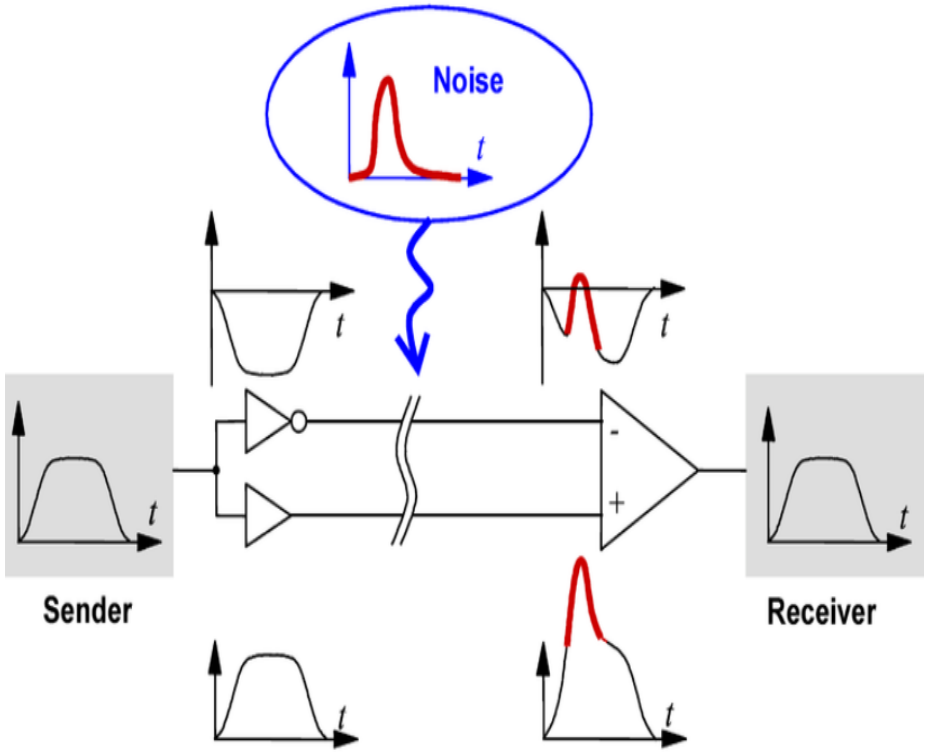
- Output: The TTL output stage is a saturated transistor to ground in the LOW state. For all CMOS families the output is a turned-on MOSFET, either to ground or to V+; i.e., rail-to-rail output swings.

- Speed and power: The bipolar TTL families consume considerable quiescent current. The corresponding speeds go from about 25MHz to about 100MHz. All CMOS families consume zero quiescent current. However, their power consumption rises linearly with increasing frequency, and CMOS operated near its upper frequency limit often dissipates as much power as the equivalent bipolar TTL family. The speed range of CMOS goes from about 2MHz to about l00MHz.

Families of TTL and CMOS ICs

- Bipolar
  - 74 - the "standard TTL" logic family had no letters between the "74" and the specific part number.
  - 74L - Low power (compared to the original TTL logic family), very slow
  - H - High speed (still produced but generally superseded by the S-series, used in 1970s era computers)
  - S - Schottky (obsolete)
  - LS - Low Power Schottky
  - AS - Advanced Schottky
  - ALS - Advanced Low Power Schottky
  - F - Fast (faster than normal Schottky, similar to AS)
- CMOS
  - C - CMOS 4–15 V operation similar to buffered 4000 (4000B) series
  - HC - High speed CMOS, similar performance to LS, 12 nS
  - HCT - High speed, compatible logic levels to bipolar parts
  - AC - Advanced CMOS, performance generally between S and F
  - AHC - Advanced High-Speed CMOS, three times as fast as HC
  - ALVC - Low voltage - 1.65 to 3.3 V, Time Propagation Delay (TPD) 2 nS
  - AUC - Low voltage - 0.8 to 2.7 V, TPD < 1.9 nS@1.8 V
  - FC - Fast CMOS, performance similar to F
  - LCX - CMOS with 3 V supply and 5 V tolerant inputs
  - LVC - Low voltage – 1.65 to 3.3 V and 5 V tolerant inputs, tpd < 5.5 nS@3.3 V, tpd < 9 nS@2.5 V
  - LVQ - Low voltage - 3.3 V
  - LVX - Low voltage - 3.3 V with 5 V tolerant inputs
  - VHC - Very High Speed CMOS - 'S' performance in CMOS technology and power

Elimination of noise by using differential signaling



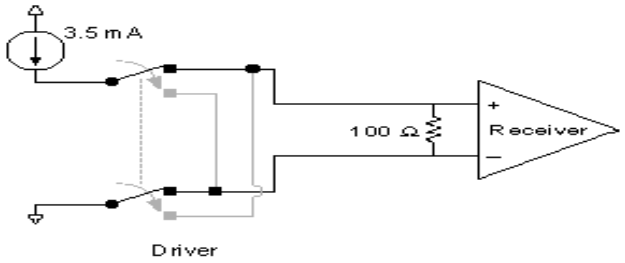


Figure 1. LVDS Driver and Receiver

In differential signaling, the transmitter translates the single input signal into a pair of outputs that are driven 180° out of phase. Since external interference tend to affect both the wires together, the receiver recovers the signal as the difference in the voltages on the two lines thus improving immunity to such problems. This transmission scheme provides large common-mode rejection and noise immunity to a data transmission system that a single-ended system referenced only to ground cannot provide.

Advantages of LVDS

- **Ability to reject common-mode noise**

When the two lines of a differential pair run adjacent and in close proximity to one another, environmental noise, such as EMI (electromagnetic interference), is induced upon each line in approximately equal amounts. Because the signal is read as the difference between two voltages, any noise common to both lines of the differential pair is subtracted out at the receiver. The ability to reject common-mode noise in this manner makes LVDS less sensitive to environmental noise and reduces the risk of noise related problems, such as crosstalk from neighboring lines.

- **Reduced amount of noise emission**

When the two adjacent lines of a differential pair transmit data, current flows in equal and opposite directions, creating equal and opposite electromagnetic fields that cancel one another. The strength of these fields is proportional to the flow of current through the lines. Thus the lower current flow in an LVDS transmission line produces a weaker electromagnetic field than other technologies.

- **Flexibility around their power supply**

LVDS offers designers flexibility around their power supply solution, working equally well at 5V, 3.3V and lower.

November 1, 2012

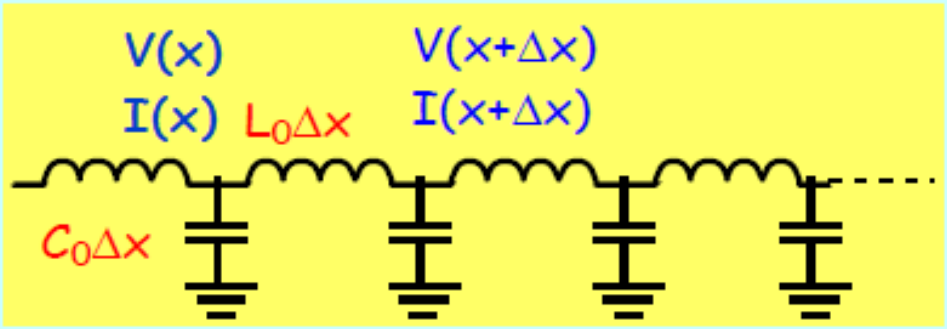
LECTURE-13

Transmission of data

- Real systems are often distributed
  - Data source is remote from signal processing
  - Instruments in hazardous or very remote environment
    - Eg. satellites, HEP, nuclear reactors,..,
  - But also applies to much shorter distances - like nearby labs or instruments in the same room
  - Need to transfer data from source to receiver
  - And usually send messages (eg. control signals) back
- Need to understand
  - Practical ways of doing this
  - Issues: power, speed, noise,… other physical constraints
- Methods - a mixture
  - Electrical, but increasing use of optical fibres,
  - Radio for satellites and space, mobile telephones,...

Electrical transmission lines

- Line with characteristic inductance and capacitance per unit length



An important assumption
R negligible

- Voltage and current satisfy 2nd order differential equation

$d^2V/dx^2 = -\omega^2 L_0 C_0 V = -k^2 V$ ie $k = \omega(L_0C_0)^{1/2}$

- Solution

$V = Ae^{jkx} + Be^{-jkx}$

Inject signal $\sim e^{j\omega t}$ $V = Ae^{j(kx+\omega t)} + Be^{-j(kx-\omega t)}$ *two opposite direction waves*

- Speed $v = \omega/k = 1/(L_0C_0)^{1/2}$

- Impedance $Z_0 = (L_0/C_0)^{1/2}$

NB real, ie resistive, but defined by L and C

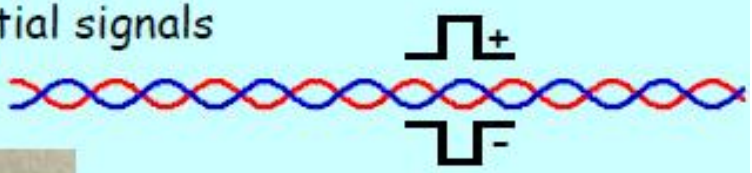
Cables

- Any wire has inductance, capacitance and resistance

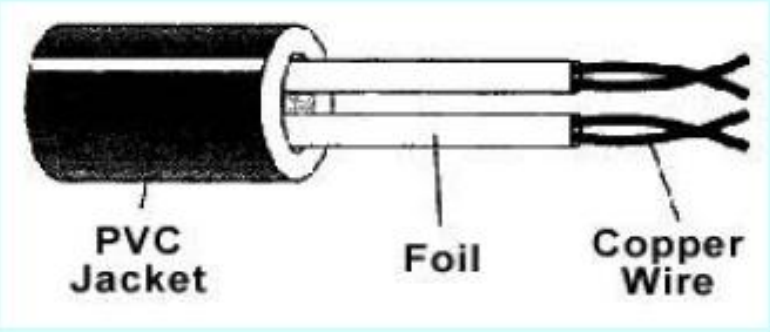
  so when is it a transmission line?

- Twisted pair

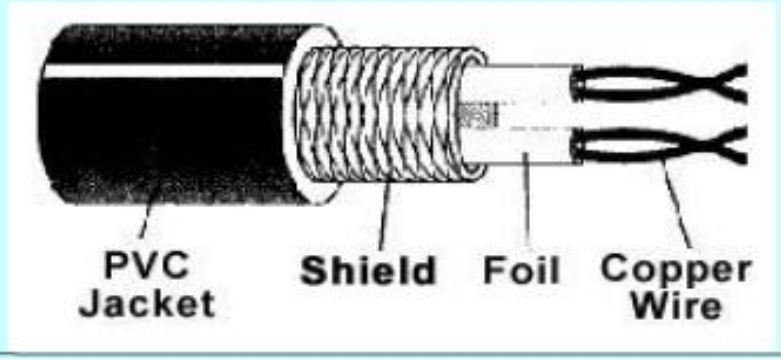
  simple pair of wires, mainly intended for differential signals



Can also be unshielded…



or shielded



Coaxial cable

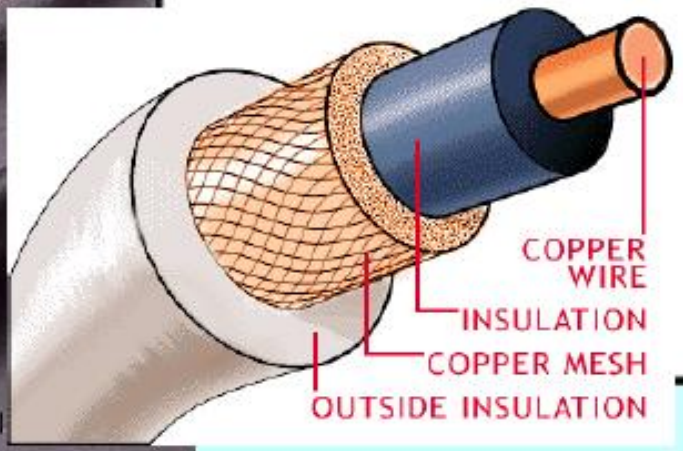
central copper core radius r_1, with plastic dielectric, braided metal shield in cylindrical geometry radius r_2

$$C_0 = 2\pi\varepsilon/\ln(r_2/r_1) \quad L_0 = (\mu_0/2\pi).\ln(r_2/r_1)$$

- Design

  Cu braid connected to ground provides electrical shield

  use special connectors

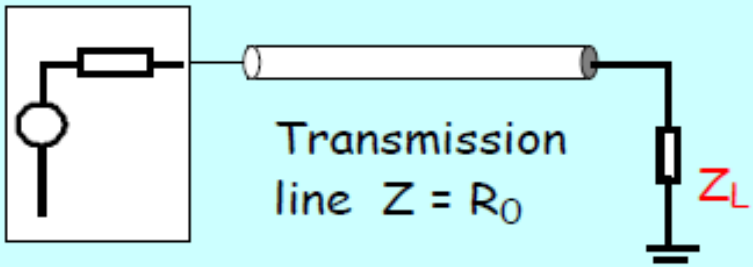


Coaxial cable properties

	RG-58	RG-178	RG-8	RG-11	RG-62	
typical dielectric	Polyethylene	Teflon	Polyethylene	Gas injected polyethylene	Foamed Fluorinated Ethylene Propylene	
outer diameter	5.0	1.8	10.3	10.3	6.1	**mm**
v/c	0.659	0.694	0.659	0.659	0.840	
Z_0	50	50	52	75	93	Ω
C_0	100.1	95.1	96.8	67.3	44.3	**pF/m**
calculated data						
L_0	0.25	0.24	0.26	0.38	0.38	**μH/m**
dielectric constant	2.30	2.08	2.30	2.30	1.42	
inner diameter	1.4	0.5	2.8	1.5	1.0	**mm**
C_0	101.2	96.1	97.3	67.5	42.7	**pF/m**
R_{core} [ρ_{Cu}=17.2nΩ.m]	2.8	18.7	0.7	2.3	5.9	**mΩ /m**
RC (1m)	0.28	1.78	0.07	0.15	0.26	**ps**
RC (100m)	2.8	17.8	0.7	1.5	2.6	**ns**

- TV antenna cables typically have 75Ω, although look similar to these
- Twin lead portable TV cables Z ~ 300Ω

Termination and Matching



- boundary conditions at termination

  $I_{inc} + I_{ref} = I_L$ & $V_{inc} + V_{ref} = V_L$

  apply them (NB $V_{ref} = -I_{ref}Z_0$)

  $V_{ref}/V_{inc} = (Z_L - Z_0)/(Z_L + Z_0)$

  $V_L/V_{inc} = 2Z_L/(Z_L + Z_0)$

- open circuit termination $Z_L = \infty$

  $V_{ref}/V_{inc} = +1$ $V_L/V_{inc} = 2$ reflected signal = incident signal

- short circuit termination $Z_L = 0$

  $V_{ref}/V_{inc} = -1$ $V_L/V_{inc} = 0$ inverted fully reflected signal

- matched termination $Z_L = Z_0$

  $V_{ref}/V_{inc} = 0$ $V_L/V_{inc} = 1$ 100% transmission to load

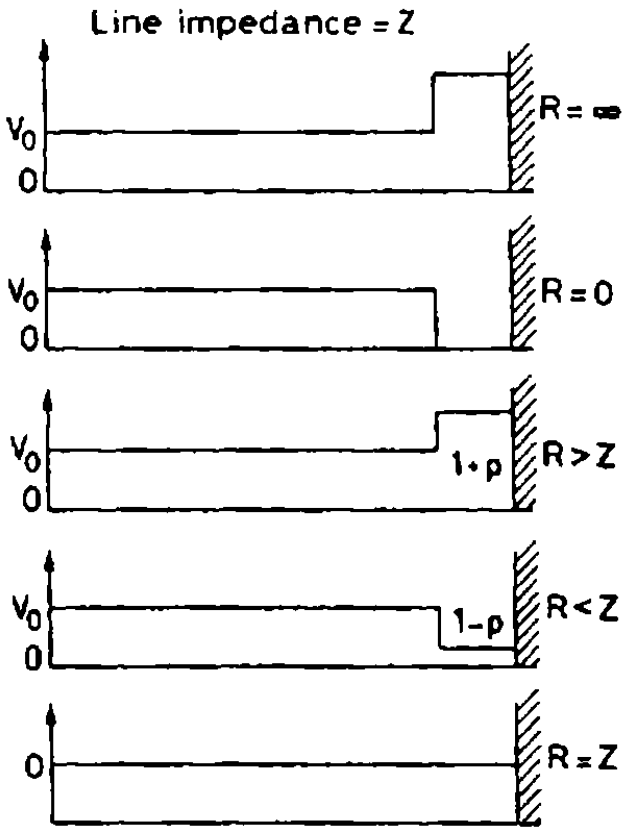
- improper termination usually causes unwanted effects

  but can sometimes make make use of reflection

  eg short circuit termination + step pulse = square pulse with width = $2\Delta t$

- why don't we always match terminate?

Reflections & terminations of a transmission line



$$\rho = \frac{V_r}{V_0} = \frac{-I_r}{I_0} = \frac{R - Z}{R + Z},$$

Cable impedance = Z_c

Source	*Load*	*Termination scheme*
$Z_s = Z_c$ — Z_c —	$Z_L = Z_c$	No termination necessary
$Z_s = Z_c$ — Z_c —	$Z_L > Z_c$	Receiving end; parallel $R = Z_c/(1 - Z_c/Z_L)$
$Z_s = Z_c$ — Z_c —	$Z_L < Z_c$	Receiving end; series $R = Z_c - Z_L$
$Z_s < Z_c$ — Z_c —	$Z_L = Z_c$	Sending end; series $R = Z_c - Z_s$
$Z_s > Z_c$ — Z_c —	$Z_L = Z_c$	Sending end; parallel $R = Z_c/(1 - Z_c/Z_s)$

Combinations of the above situations may also arise in which case an appropriate combination of termination schemes may be used, e.g.,

$Z_s < Z_c$ — Z_c —	$Z_L > Z_c$	Receiving end; parallel $R = Z_c/(1 - Z_c/Z_L)$ with sending end; series $R = Z_c - Z_s$

To match or not? (i)

- Impedance matching is a general question, not only for transmission lines
- Match if
  - to transfer maximum power to load (source must be capable)
    - eg audio speakers
  - minimise reflections from load
    - very important in audio, fast (high frequency) systems, to avoid ringing
    - or multiple pulses (eg in counting systems)
  - fast pulses
    - pulse properties can contain important information
    - usually don't want to change
    - sometimes we wish to do this with "too fast" signals - "spoiling"
- Usually match by choosing impedances, adding voltage buffers
  - transformer matching is another method if this is impractical

To match or not? (ii)

- Don't match if
  - High impedance source with small current signals - typical of many sensors
    - photodiode, or other sensors must drive high impedance load
    - short cables are required to avoid difficulties
  - Weak voltage source, where drawing power from source would affect result
    - eg bridge circuits
  - require to change properties of fast pulse
    - eg pulse widening for ease of detection
  - electronics with limited drive capabilities
    - eg logic circuits, many are designed to drive other logic, not long lines
    - CMOS circuits, even with follower, are an example
  - If you get this wrong, often end up with new time constants in the system
    - or prevent system from working at all, eg diode with low R load

Coaxial cable limits

- Transmission speed and bandwidth limiting
  - all cables have finite resistance (though remarkably small)
  - for long cables, RC time constant per unit length becomes noticeable
  - therefore expect delay, attenuation and finite rise time in fast pulses
- When is a cable a transmission line?
  - not reasonable to assume transmission line behaviour unless length of line is at least ~ 1/8 wavelength
- Other forms of transmission line
  - in high speed circuits, tracks must be laid out carefully using knowledge of the characteristics of the boards to control delays, rise times and signal velocities
  - eg parallel tracks,...
  - often need measurement to define parameters precisely
  - ultra high frequencies need waveguides or alternative

Pulse distortions in cables

Signal losses in a transmission line arise from resistance in the conductors and leakage through the dielectric. In addition, some loss may also result from electromagnetic radiation; however, this effect is small, especially in coaxial cables with their inherent shielding, and can be neglected for most purposes.

As frequency of the signal increases, the current in the conductors confines itself to thinner and thinner layers near the conductor surface. The effective cross-sectional area of the conductor is thus reduced and its resistance increased. For a coaxial cable, this results in a resistance per unit length which varies approximately as the square root of the frequency and inversely as the inner and outer radii.

Pulse distortions in cables

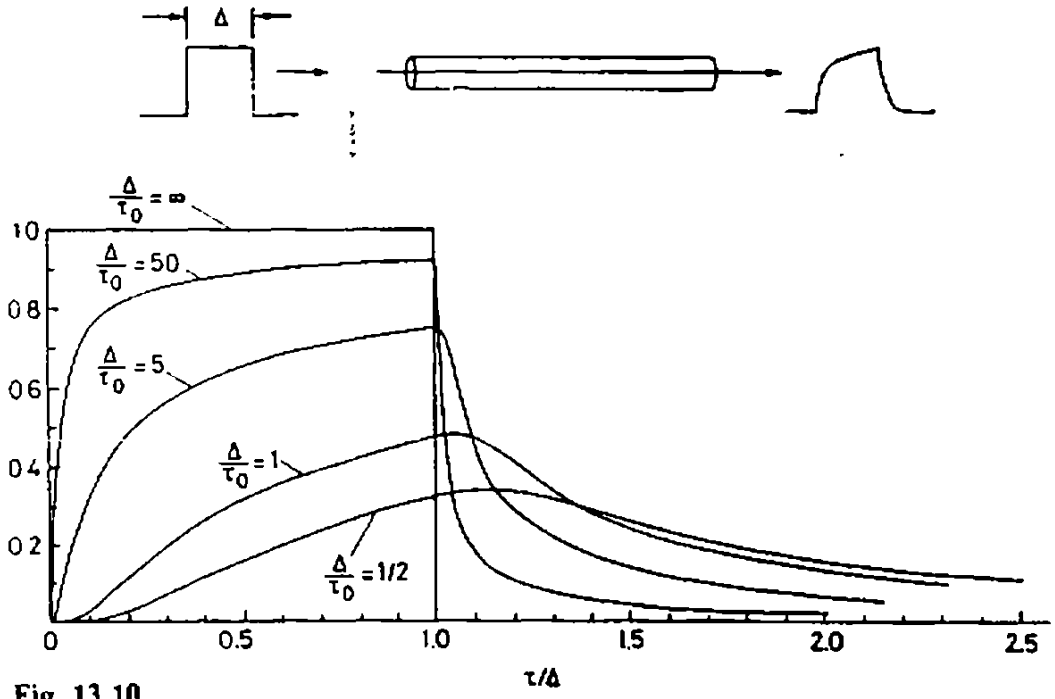


Fig. 13.10

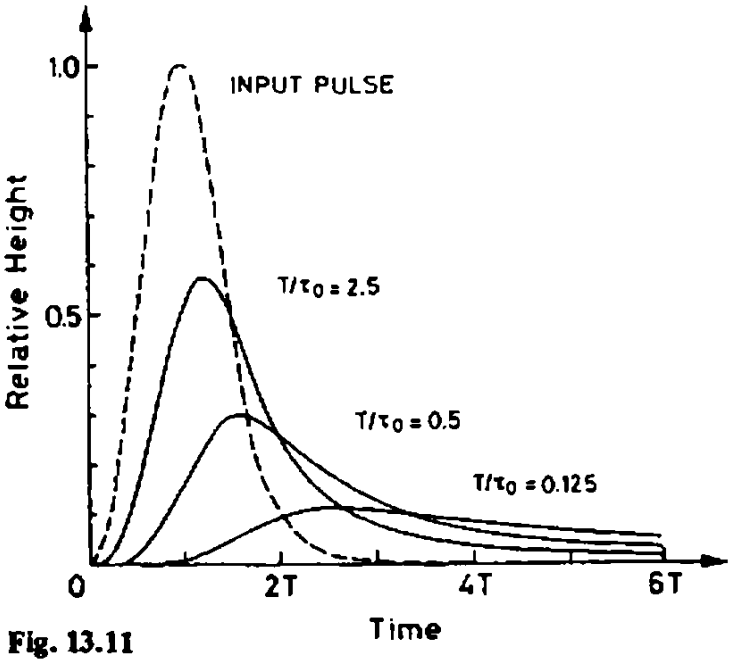


Fig. 13.11

Good reference: Leo, Chapter 9

November 6, 2012

LECTURE-14

Common pulse processing functions

Ⓐ Linear–Linear	In	Out
PREAMPLIFIER	Linear charge pulse from the detector	Linear tail pulse
LINEAR AMPLIFIER	Linear tail pulse	Amplified and shaped linear pulse
BIASED AMPLIFIER	Shaped linear pulse	Linear pulse proportional to amplitude of input pulse that lies above input bias level
PULSE STRETCHER	Fast linear pulse	Conventional shaped linear pulse of amplitude equal to input pulse
SUM AMPLIFIER	Two or more shaped linear pulses	Shaped linear pulse with amplitude equal to the sum of coincident input pulses
DELAY	Fast linear or shaped linear pulse	Identical pulse after a fixed time delay
Linear input — LINEAR GATE (Gate input)	(1) Shaped linear pulse (2) Gate pulse	Linear pulse identical to linear input if gate pulse is supplied in time overlap

November 12, 2012

LECTURE-15

SUDESHNA DASGUPTA

November 20, 2012

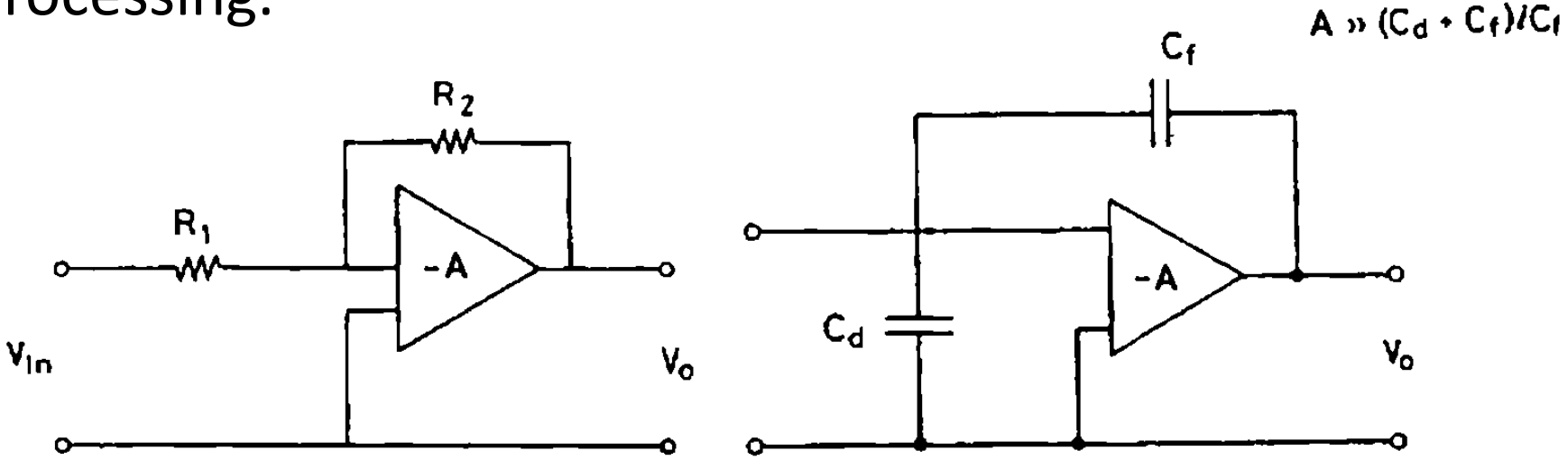
LECTURE-16

Common pulse processing functions

Ⓑ Linear–Logic	In	Out
INTEGRAL DISCRIMINATOR	Shaped linear pulse	Logic pulse if input amplitude exceeds discrimination level
DIFFERENTIAL DISCRIMINATOR (SINGLE-CHANNEL ANALYZER)	Shaped linear pulse	Logic pulse if input amplitude lies within acceptance window
TIME PICK-OFF (TRIGGER)	Fast linear or shaped linear pulse	Logic pulse synchronized with some feature of input pulse
Ⓒ Logic–Linear	**In**	**Out**
START, STOP → TIME–AMPLITUDE CONVERTER	Logic start and stop pulses separated by time Δt	Shaped linear pulse with amplitude proportional to Δt
Ⓓ Logic–Logic	**In**	**Out**
COINCIDENCE	Logic pulses at two or more inputs	Logic pulse if pulses appear at all inputs within a time interval τ (resolving time)
ANTI-COINCIDENCE	Logic pulses at two inputs	Logic pulse only if pulse appears at one input *without* pulse at second input within time τ
SCALER	Logic pulses	One logic pulse for every N input pulses

Preamplifiers

The amplifier serves two main purposes:
1) amplify the signal from the preamplifier
2) shape it to a convenient form for further processing.



▲

Fig. 14.1. Schematic diagram of a voltage-sensitive preamplifier

Fig. 14.2. Schematic diagram of a charge-sensitive preamplifier. To discharge the capacitor C_f, a resistor is also usually placed in parallel with C_f. This results in the exponential *tail* pulse

Resistive vs Optical Feedback

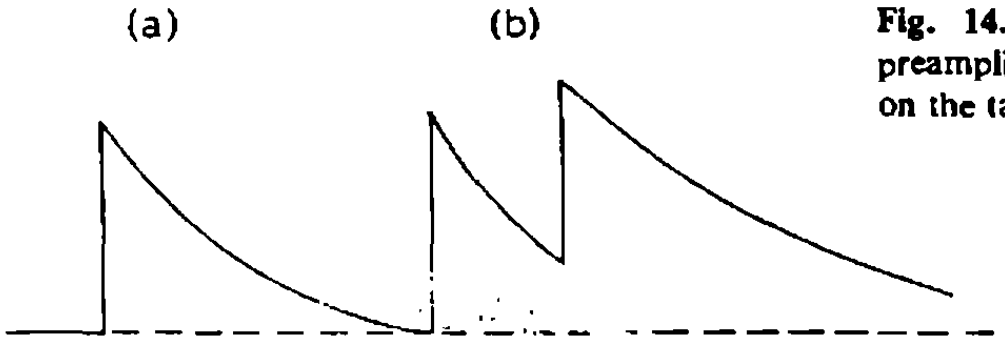


Fig. 14.3. (a) Exponential *tail* pulse from a preamplifier, (b) *pulse pileup*: a second pulse rides on the tail of the first

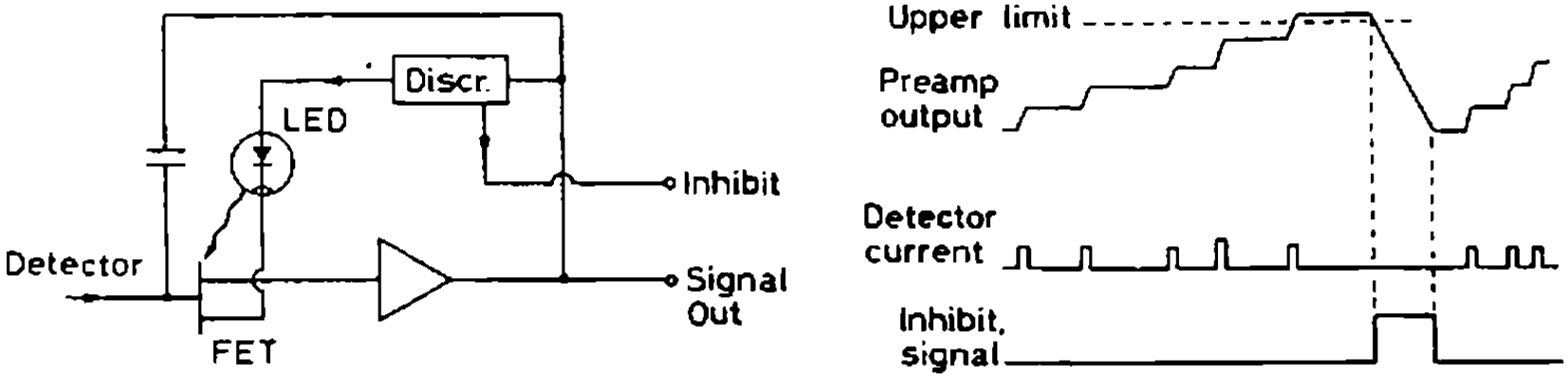


Fig. 14.4. Schematic diagram and pulse putput of an optical feedback preamplifier

Need for pulse shaping

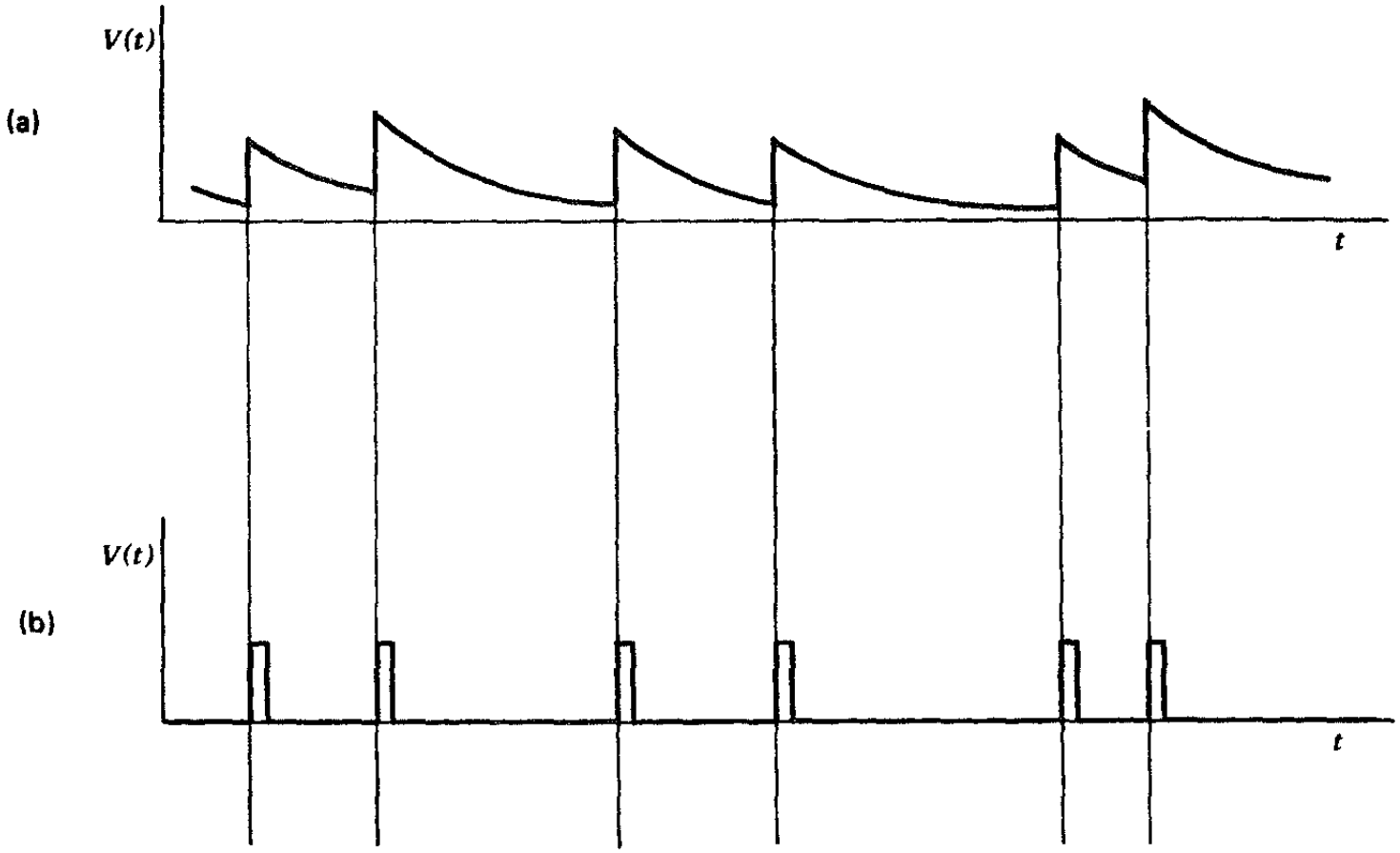
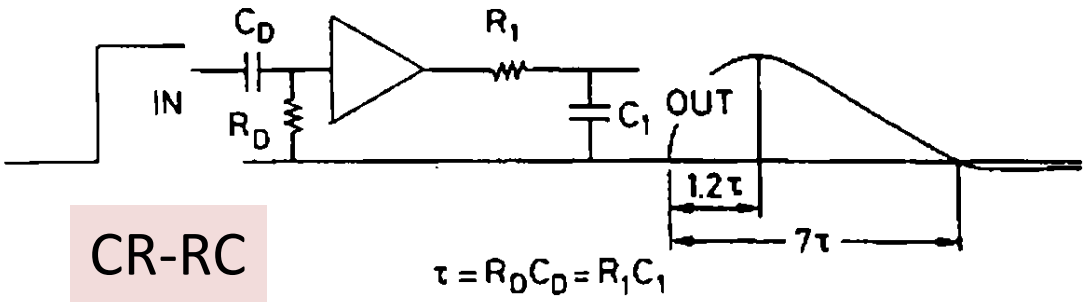


Figure 16.8 The pulses with long tails shown in part (*a*) illustrate the apparent variation in amplitude due to pulse pile-up. These effects can greatly be reduced by shaping the pulses as in part (*b*).

CR-RC shapers



CR-RC

Pole-Zero Cancellation

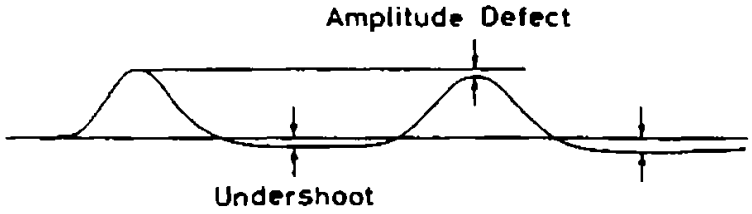


Fig. 14.6. Amplitude defect arising from undershoot in CR-RC pulse shaping

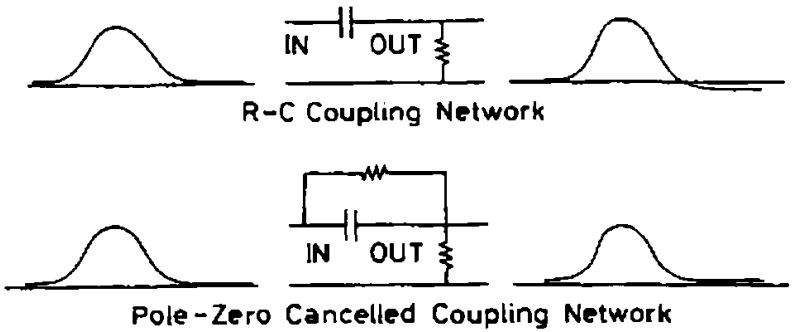
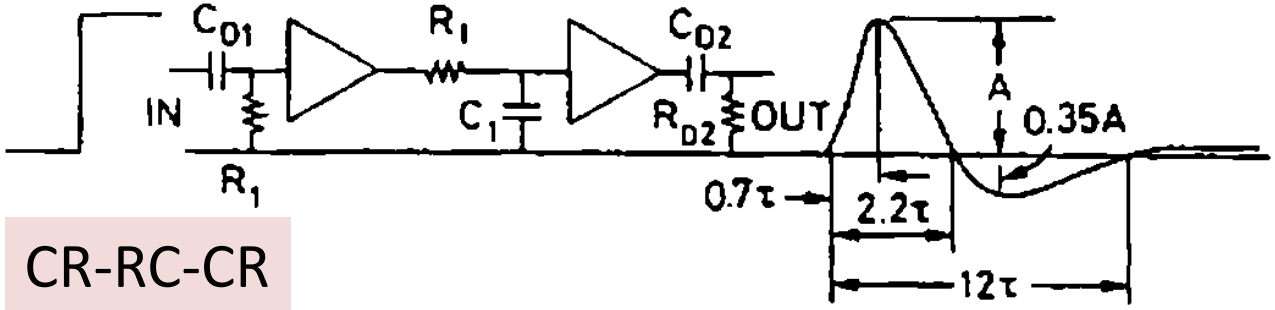


Fig. 14.7. Pole-zero cancellation circuit (from *Ortec* catalog [14.1])



CR-RC-CR

$\tau = R_{D1} C_{D1} = R_1 C_1 = R_{D2} C_{D2}$

Response of CR-RC shaper

$$E_{\text{out}} = \frac{E\tau_1}{\tau_1 - \tau_2}\left(e^{-t/\tau_1} - e^{-t/\tau_2}\right) \tag{16.22}$$

where τ_1 and τ_2 are time constants of the differentiating and integrating networks, respectively. Plots of this response for several different combinations of τ_1 and τ_2 are shown in Fig. 16.12.

In nuclear pulse amplifiers, *CR-RC* shaping is most often carried out using equal differentiation and integration time constants. In that event, Eq. (16.22) becomes indeterminant, and a particular solution for this case is

$$E_{\text{out}} = E\frac{t}{\tau}e^{-t/\tau} \tag{16.23}$$

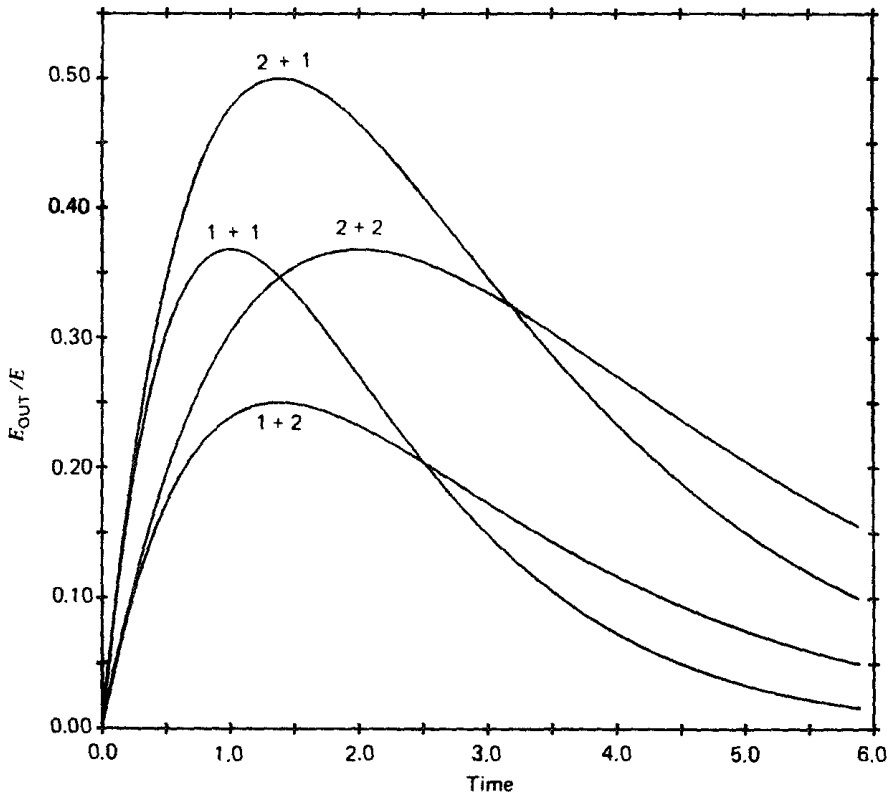


Figure 16.12 The response of a *CR-RC* network to a step voltage input of amplitude E at time zero. Curves are shown for four pairs of differentiator + integrator time constants. Units of the time constants and time scale are identical.

Pole-zero cancellation

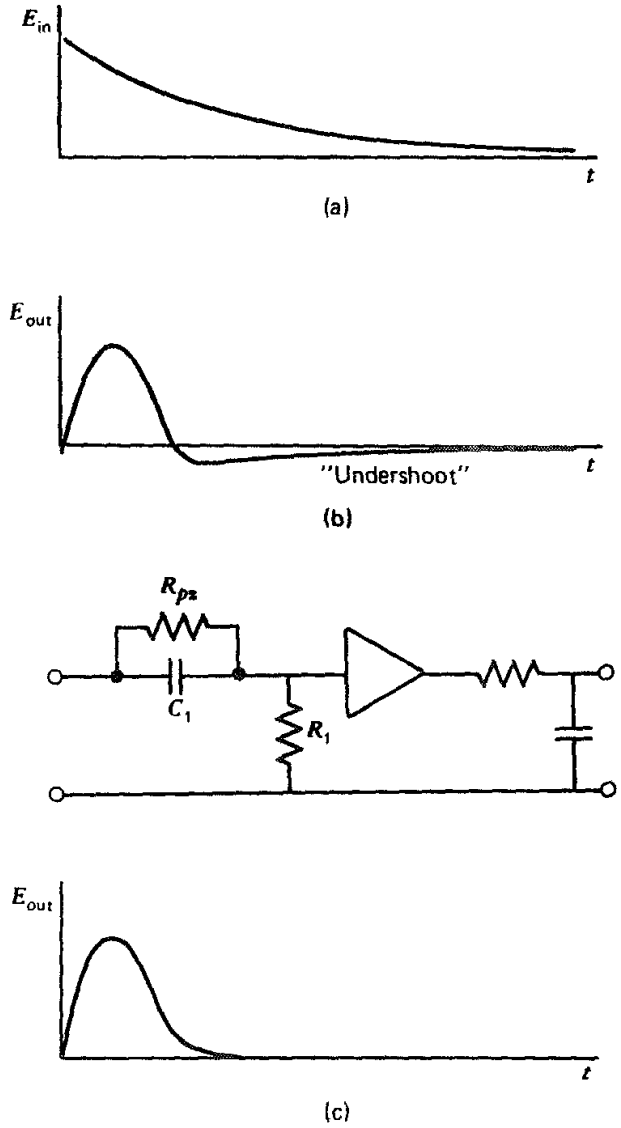
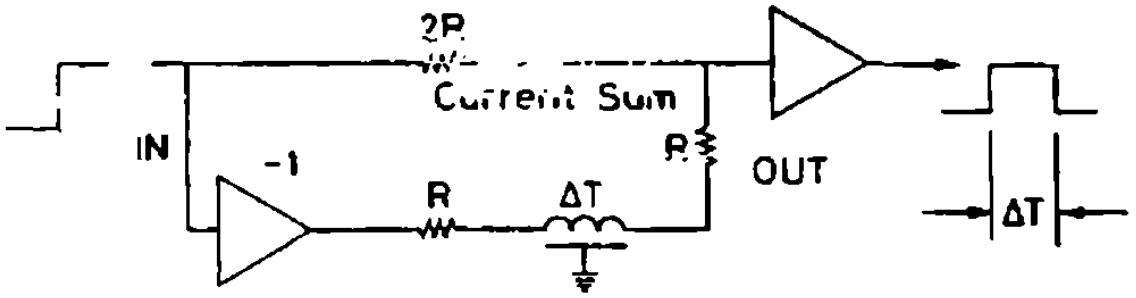
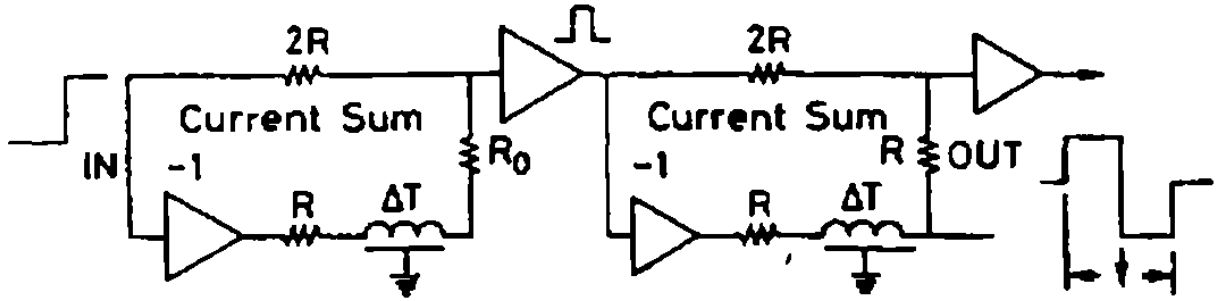


Figure 16.15 Application of pole-zero cancellation to eliminate the undershoot (b) normally generated by a CR-RC shaping network for an input step with finite decay time. By adding an appropriate resistance R_{pz} to the differentiator stage, a waveform without undershoot (c) can be obtained.

Delay line shaping



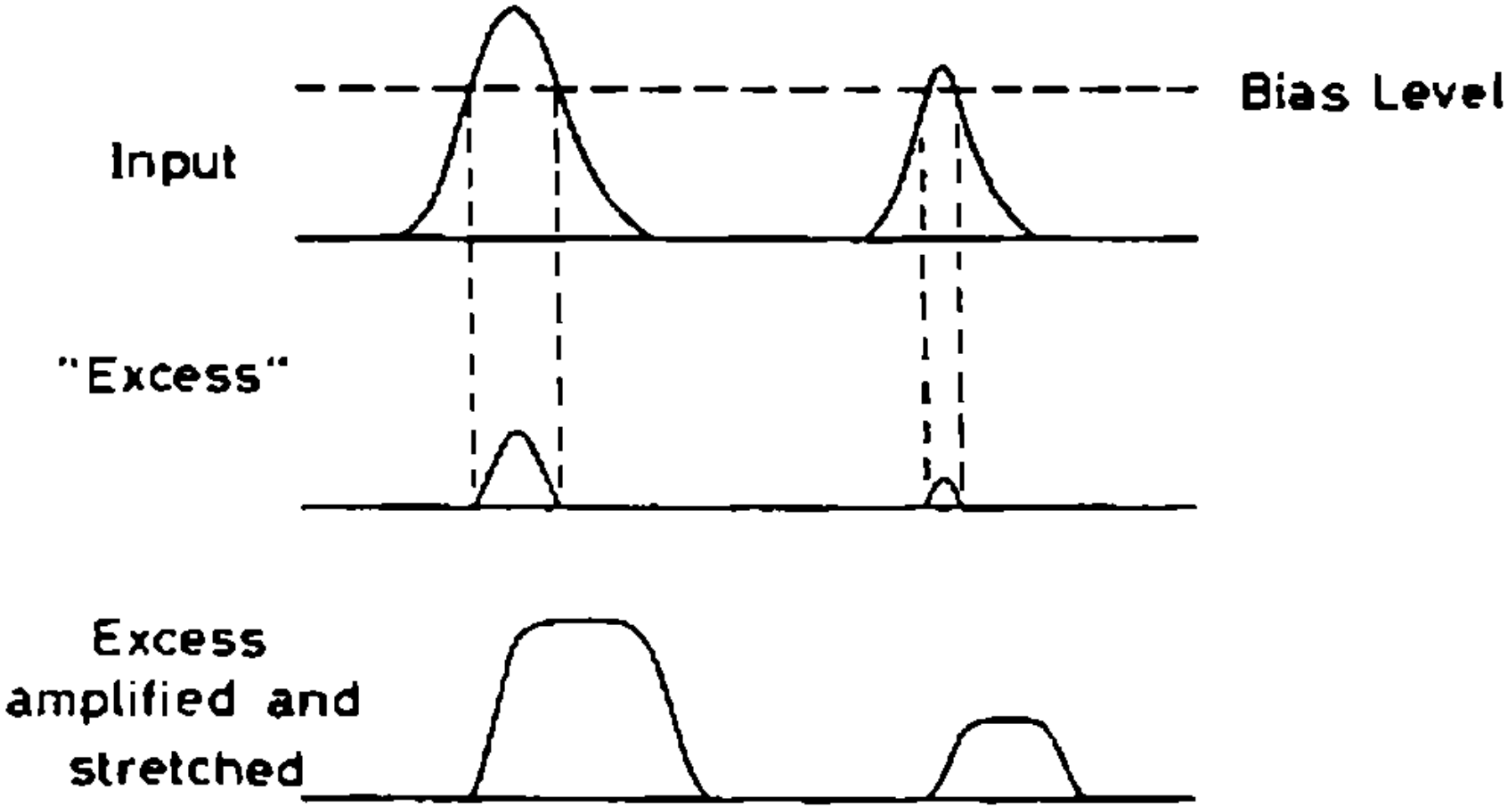
a) Single - Delay - Line



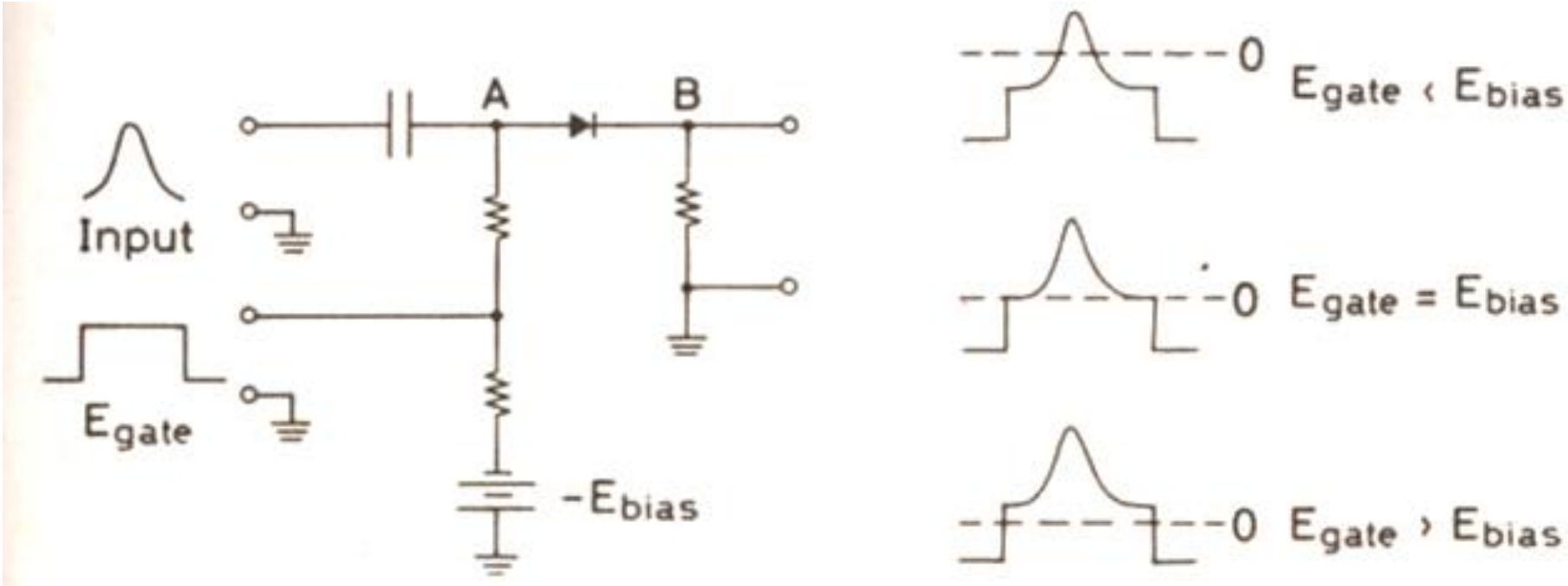
b) Double - Delay - Line

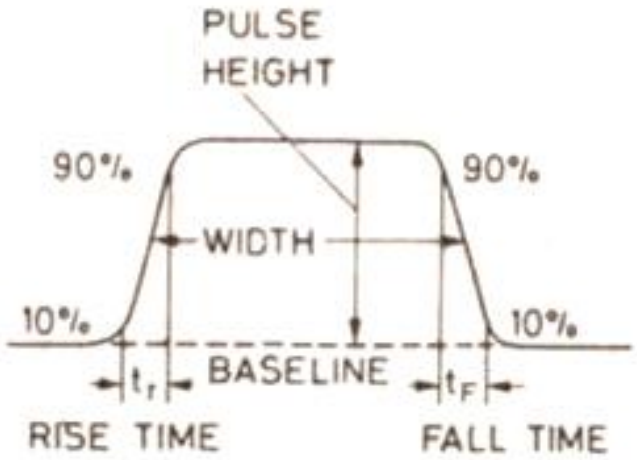
Fig. 14.10. (**a**) Single delay-line pulse shaping, (**b**) double delay line pulse shaping (from *Ortec* catalog [14.1])

Biased amplifiers



Linear gates





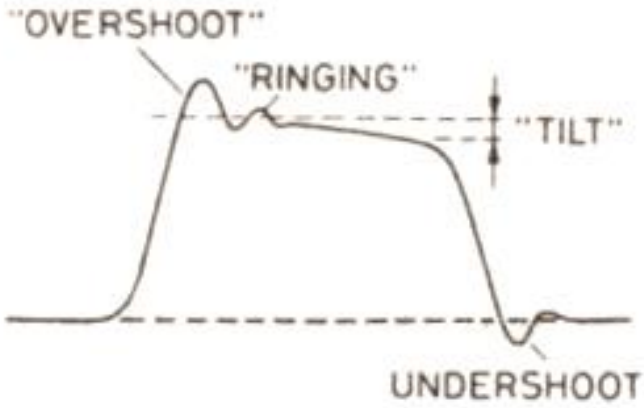


Fig. 11.1. Pulse signal terminology

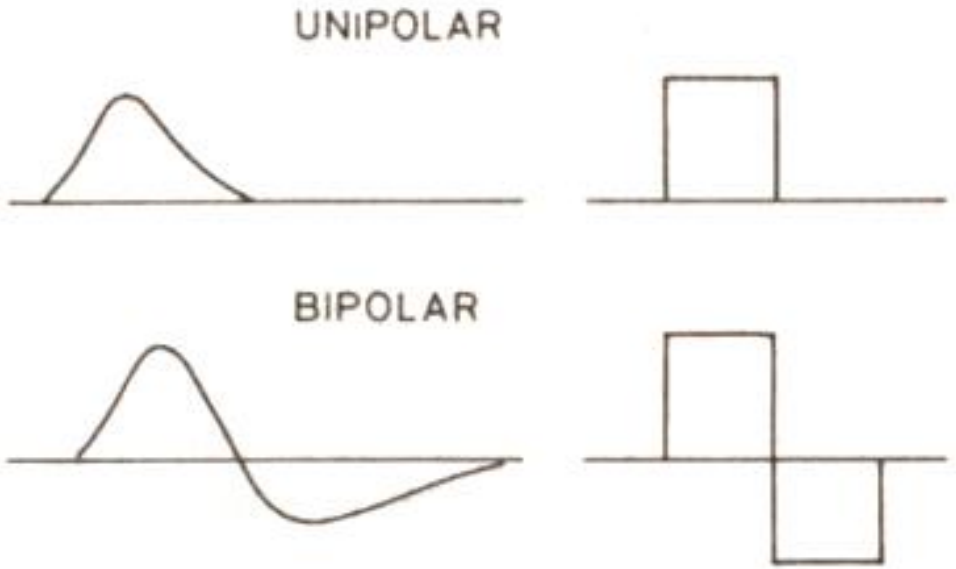
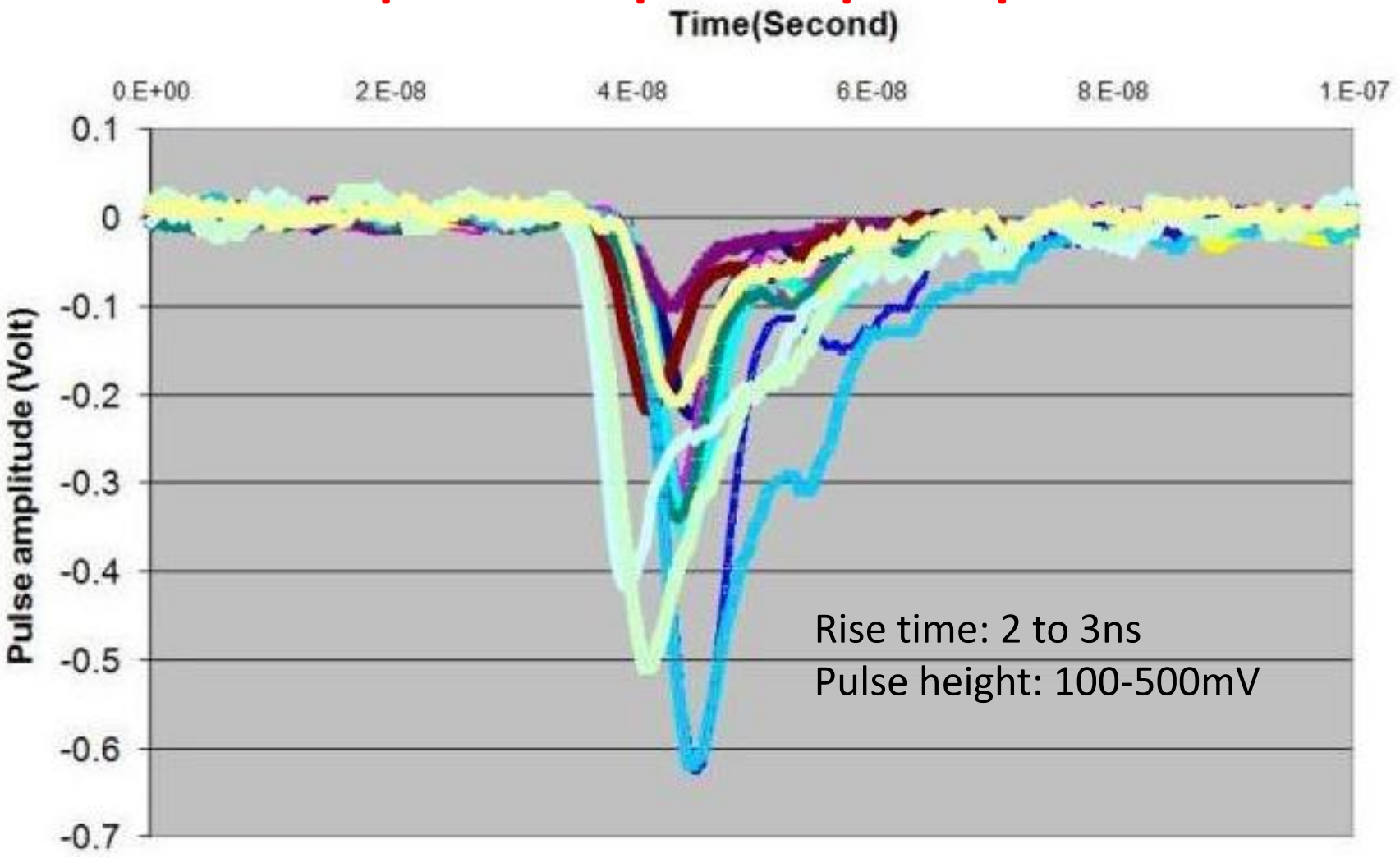


Fig. 11.2. Unipolar and bipolar pulses

November 22, 2012

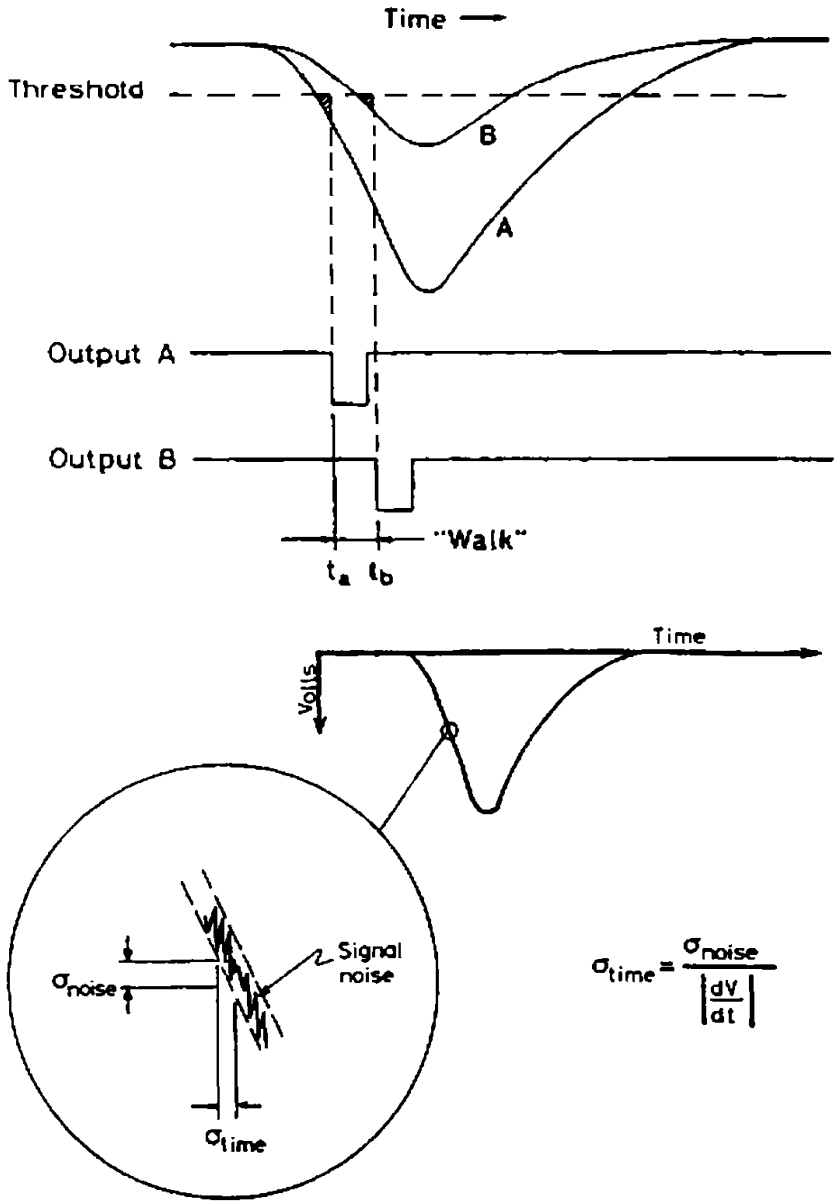
LECTURE-17

HMC preamp output pulses



Considerations for discriminators

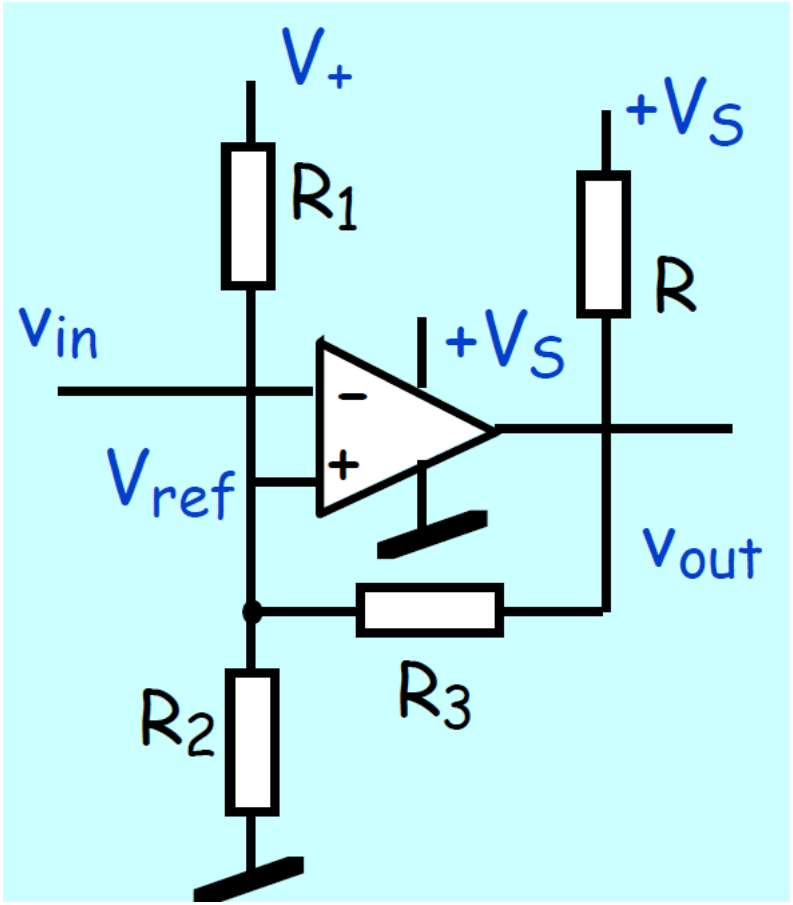
- Two common problems
  - Walk (due to variations in the amplitude and rise time, finite amount of charge required to trigger the discriminator)
  - Jitter (due to intrinsic detection process – variations in the number of charges generated, their transit times and multiplication factor etc.)



Types of discriminators

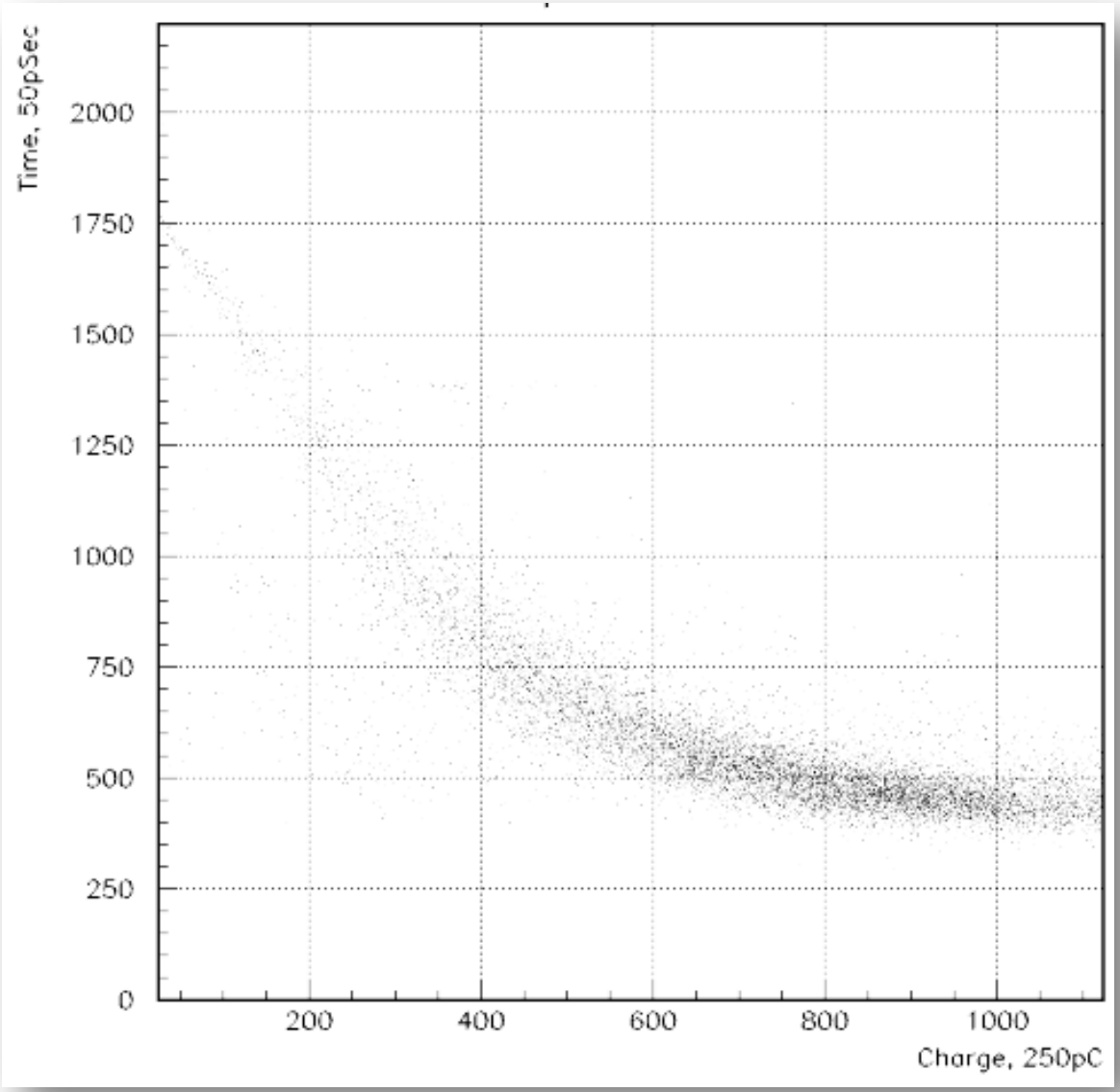
- Leading edge triggering
- Fast zero-crossing triggering
- Constant fraction triggering
- Amplitude and rise time compensated triggering

Leading edge discriminators



- Fine with if input amplitudes restricted to small range.
- For example:
  - With 1 to 1.2 range, resolution is about 400ps.
  - But at 1 to 10 range, the walk effect increases to ±10ns.
- That will need off-line corrections for time-walk using charge or time-over-threshold (TOT) measurements.

Off-line corrections of time-walk



Zero-crossing and Constant fraction

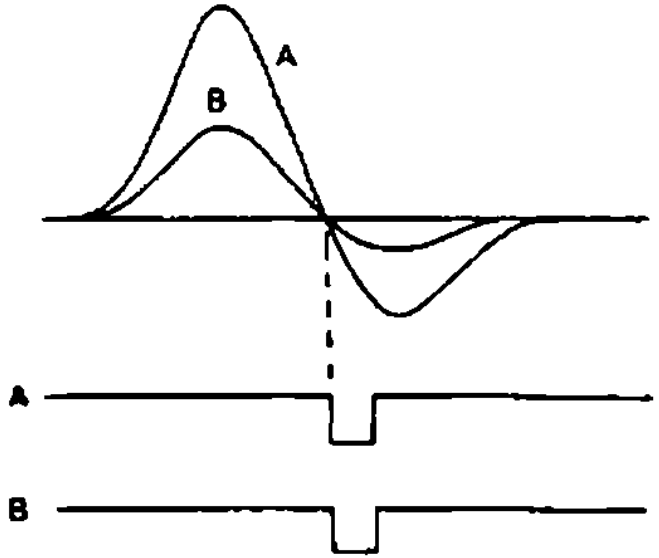


Fig. 17.3. Zero-crossing timing. Variations in the cross-over point are known as *zero-crossing walk*

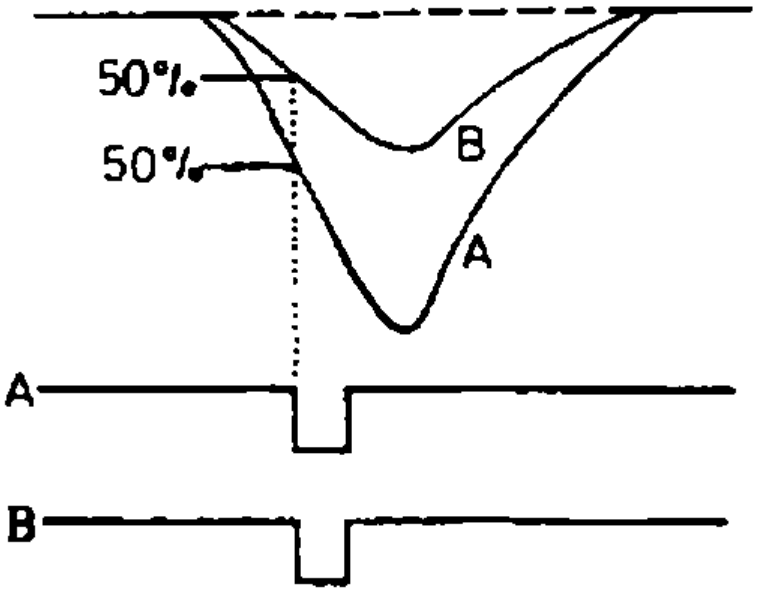


Fig. 17.4. Constant fraction discrimination

- Zero-crossing Triggering:
  - Timing resolution 400ps, if amplitude range is 1 to 1.2
  - Timing resolution 600ps, even if the amplitude range is 1 to 10
  - But, requires signals to be of constant shape and rise-time.

CF and ARC triggering

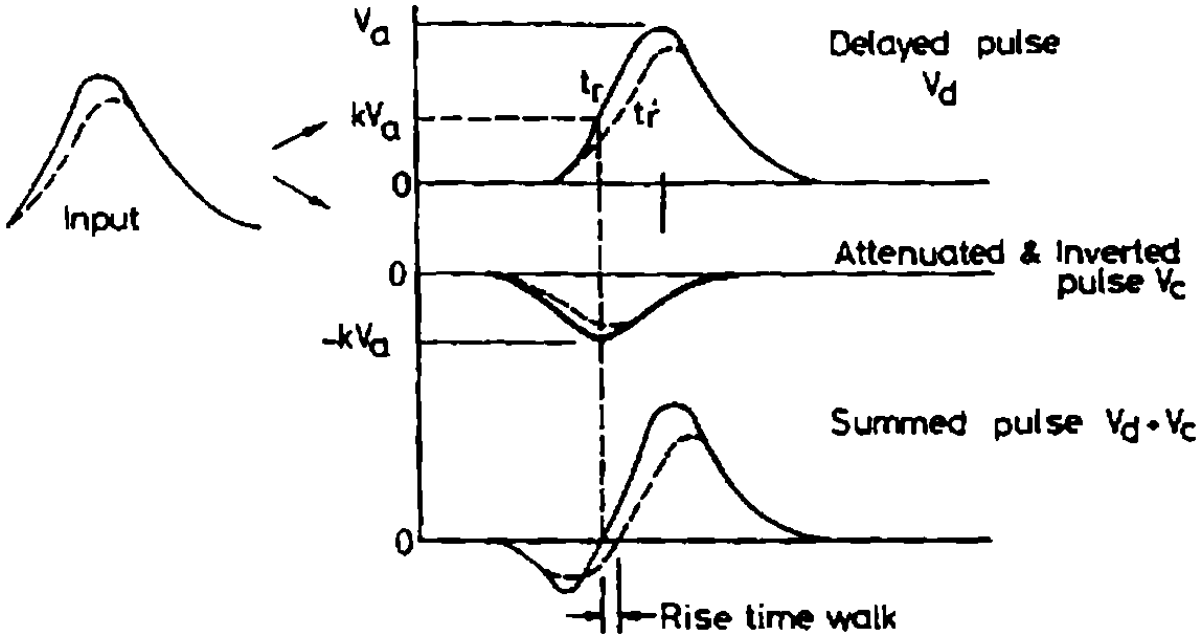


Fig. 17.5. Technique for constant fraction triggering. In order for this technique to work rise times of all signals must be the same. The dotted line shows the result with a different rise time signal

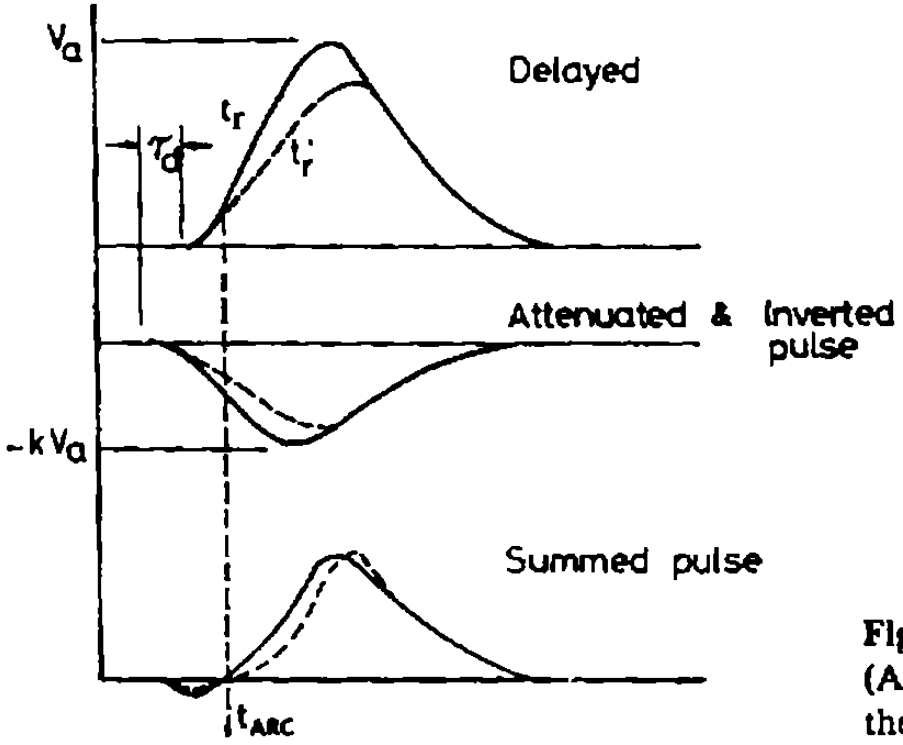


Fig. 17.6. Amplitude and risetime compensation (ARC) triggering. The zero-crossover occurs before the signal peak is reached

Basic coincidence technique

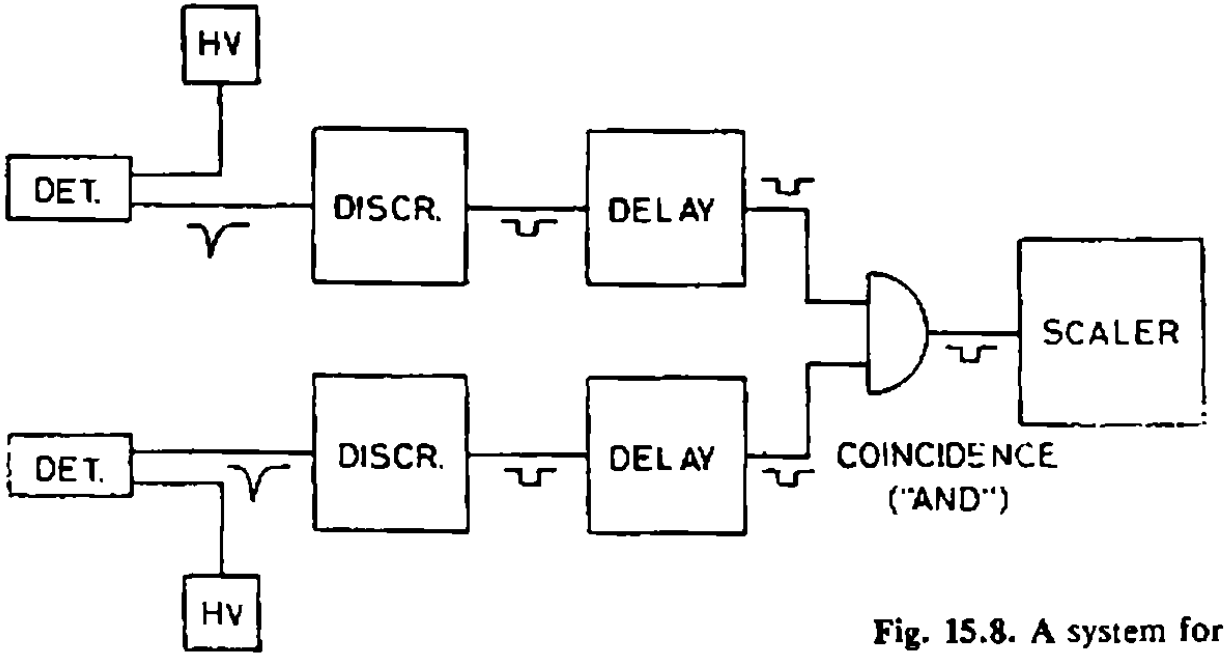


Fig. 15.8. A system for coincidence measurement

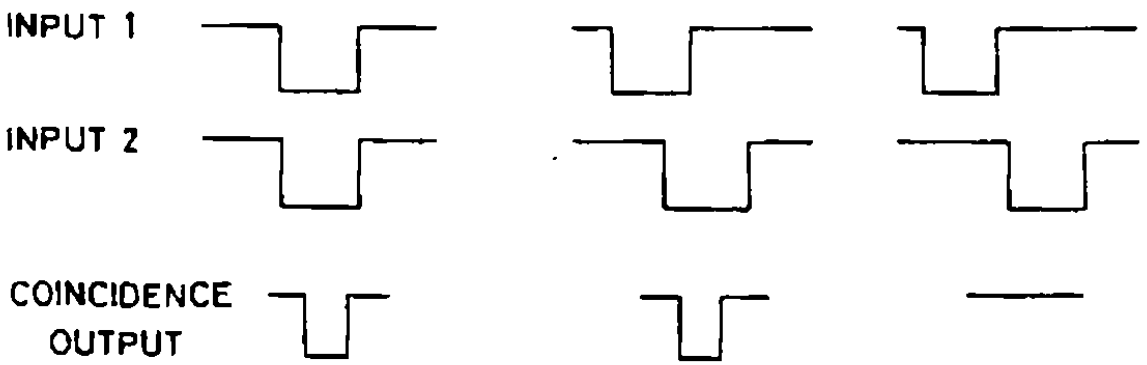


Fig. 15.9.
Coincidence between pulses

Fast-slow coincidence circuits

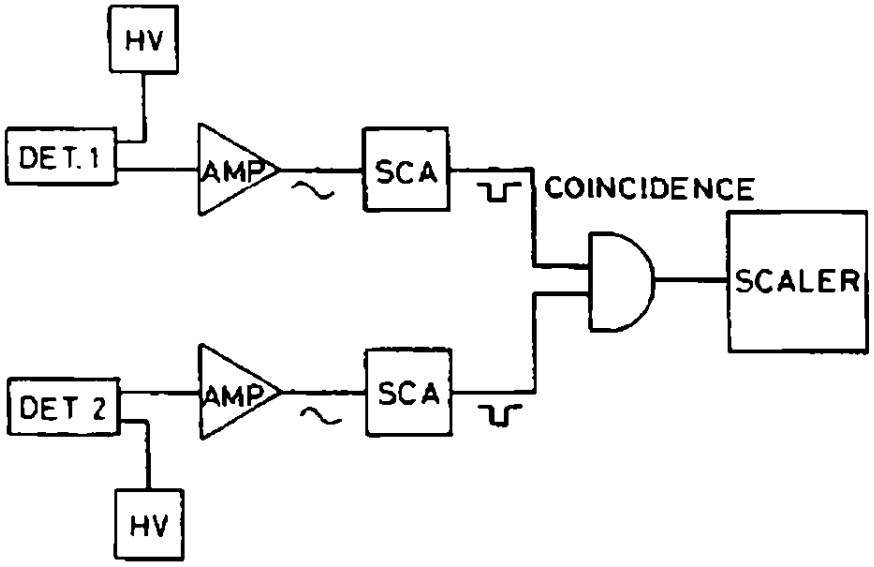


Fig. 15.13. A system with pulse height selection and slow coincidence

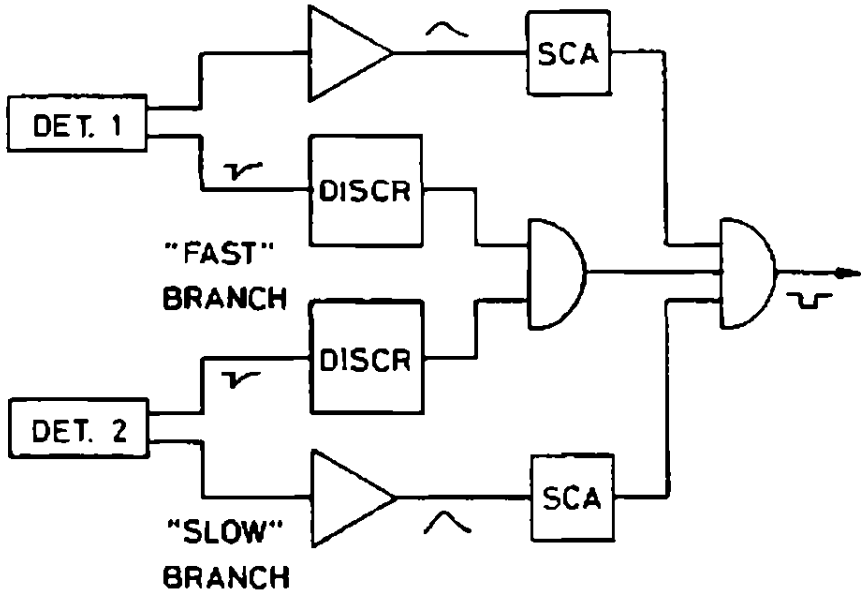


Fig. 15.14. A *fast-slow* coincidence system

November 29, 2012

LECTURE-18

Analogue to Digital Conversion

- Turns electrical input (voltage/current) into numeric value
- Parameters and requirements
  - Resolution
    - the granularity of the digital values
  - Integral Non-Linearity
    - proportionality of output to input
  - Differential Non-Linearity
    - uniformity of digitisation increments
  - Conversion time
    - how much time to convert signal to digital value
  - Count-rate performance
    - how quickly a new conversion can begin after a previous event
  - Stability
    - how much values change with time

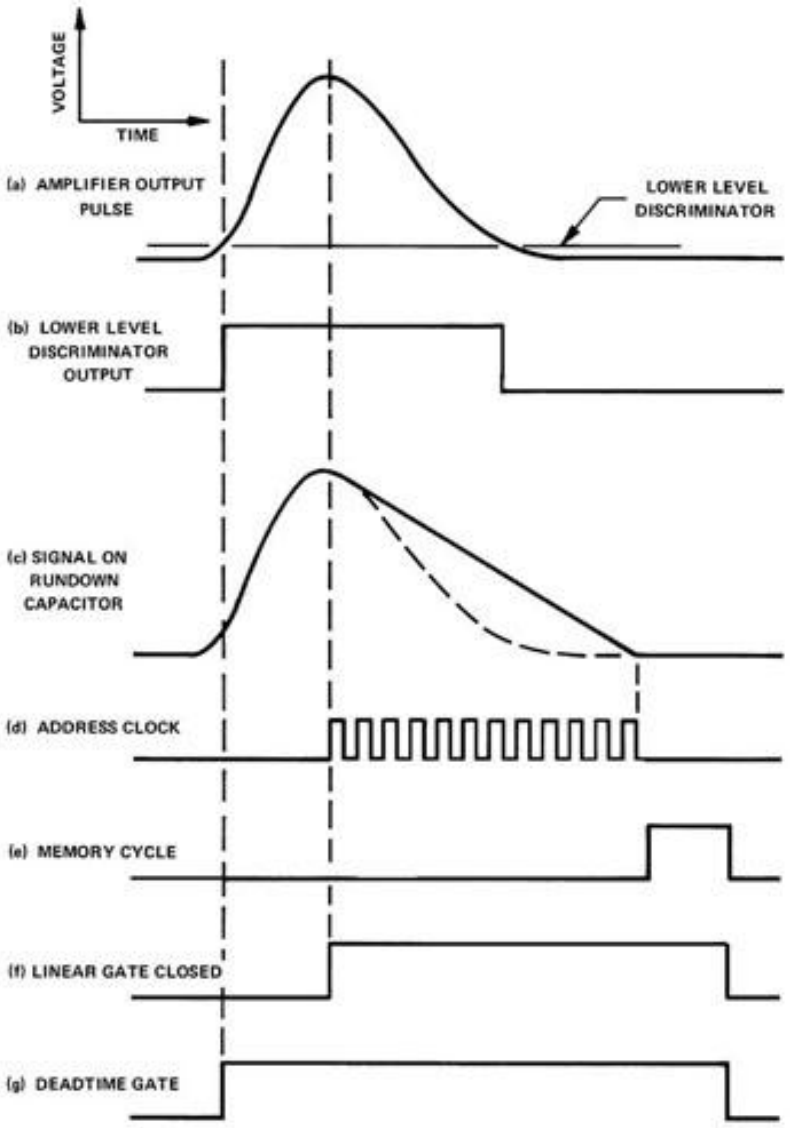
Analog-to-Digital Converters (ADCs)

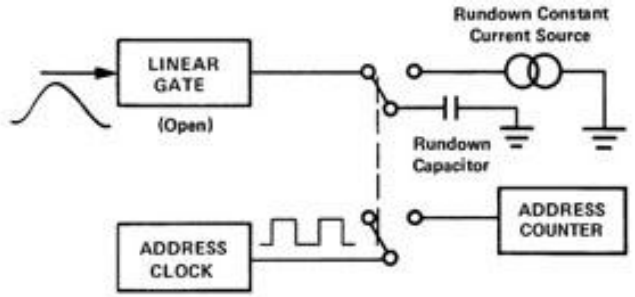
- Peak-sensing
  - Maximum of the voltage signal is digitised
  - Ex: Signal of the PMT in voltage mode (slow signals, already integrated)
- Charge sensitive
  - Total integrated current digitised
  - Ex: Signal of the PMT in the current mode (fast signals)
- Time of integration or the time period over which the ADC seeks a maximum is determined by the width of the gate signal

Types of ADCs

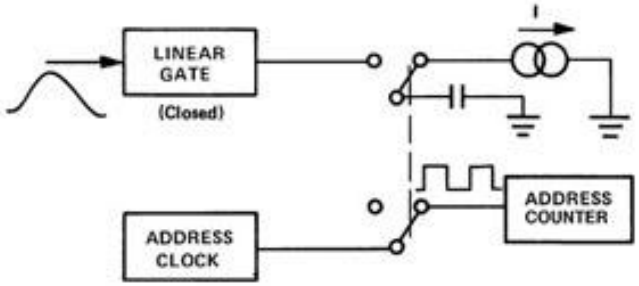
- Ramp or Wilkinson
- Successive approximation
- Flash or parallel
- Sigma-delta ADC
- Hybrid (Wilkinson + successive approximation)
- Tracking ADC
- Parallel ripple ADC
- Variable threshold flash ADC
- …

Ramp or Wilkinson ADC

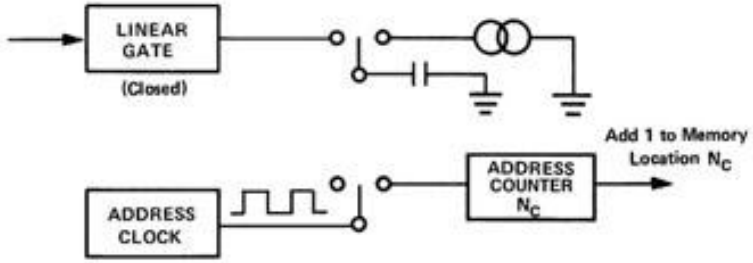




(a) Capacitor Charging



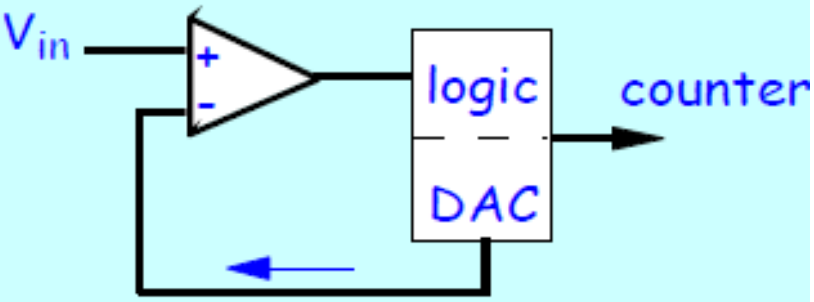
(b) Capacitor Rundown



(c) Memory Cycle

Successive approximation ADC

- analogous to binary search
  - generate $V_{ref} = \Delta V \times (2^{N-1}, 2^{N-2}, \ldots 2^0)$ in N steps
  - set bit = 1
  - if $V_{in} > V_{ref}$
    - leave
  - else bit = 0

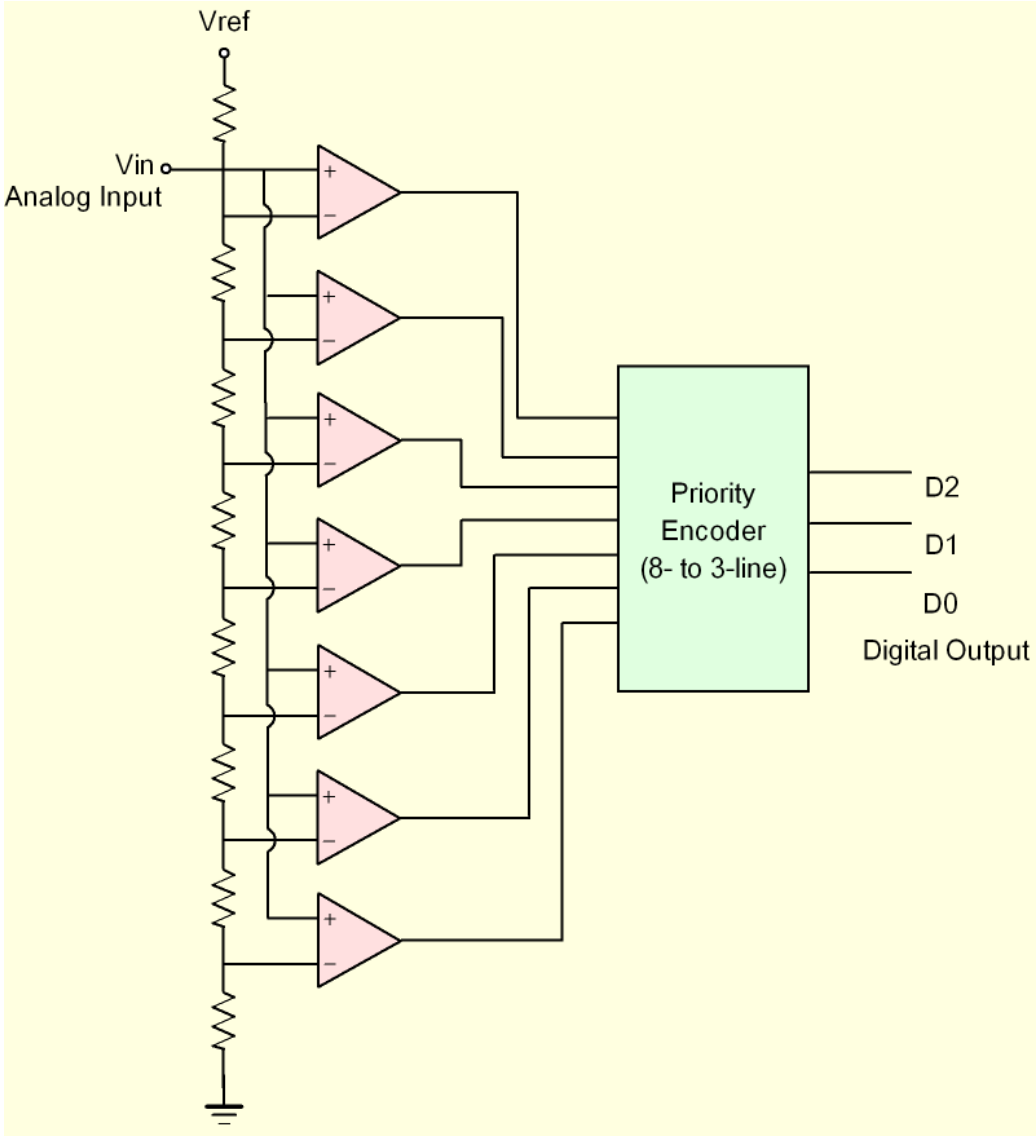


- Pros
  - speed ~ μsec
  - high resolution
- Cons
  - DNL 10-20%
    - *very precise resistors required with DAC for V_{ref}*

DAC = digital to analogue converter
ie number -> voltage

Flash or parallel ADC

- Flash ADC is the fastest ADC type available. The digital equivalent of the analog signal will be available right away at it output – hence the name “flash”.
- The number of required comparers is 2^{n-1}, where n is the number of output bits.
- Since Flash ADC comparisons are set by a set of resistors, one could set different values for the resistors in order to obtain a non-linear output, i.e. one value would represent a different voltage step from the other values.



December 11, 2012

LECTURE-19

Sigma-delta ADC

- Digitise the signal with 1-bit resolution at a high sampling rate (MHz).

  useful for high resolution conversion of low-frequency signals, to 20bits

  low-distortion conversion of audio signals

  good linearity and high accuracy.

- Operation - At t = 0, assume $V_{ref} = 0$

  V_{out} high

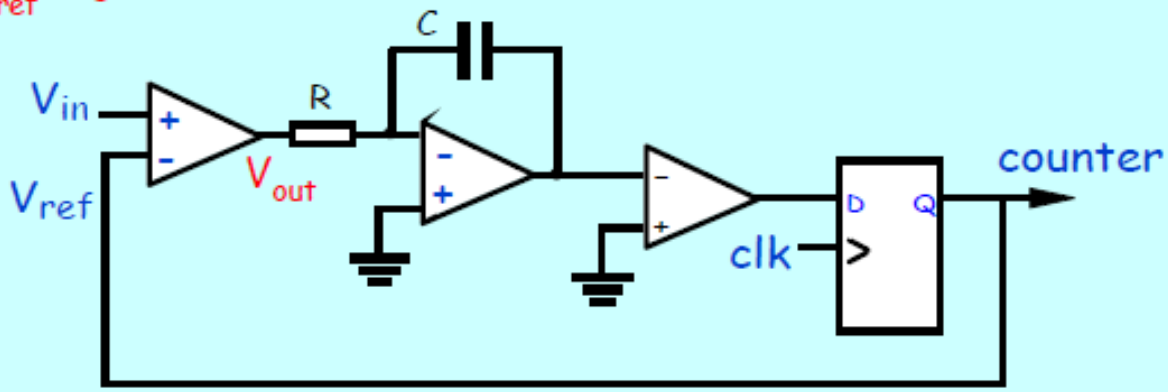
  integrator charges -ve

  at rate ~ V_{in}

  comparator flips

  counter goes low

  clock increments... etc,...



$V_{in} = 0$ => output = 000000...

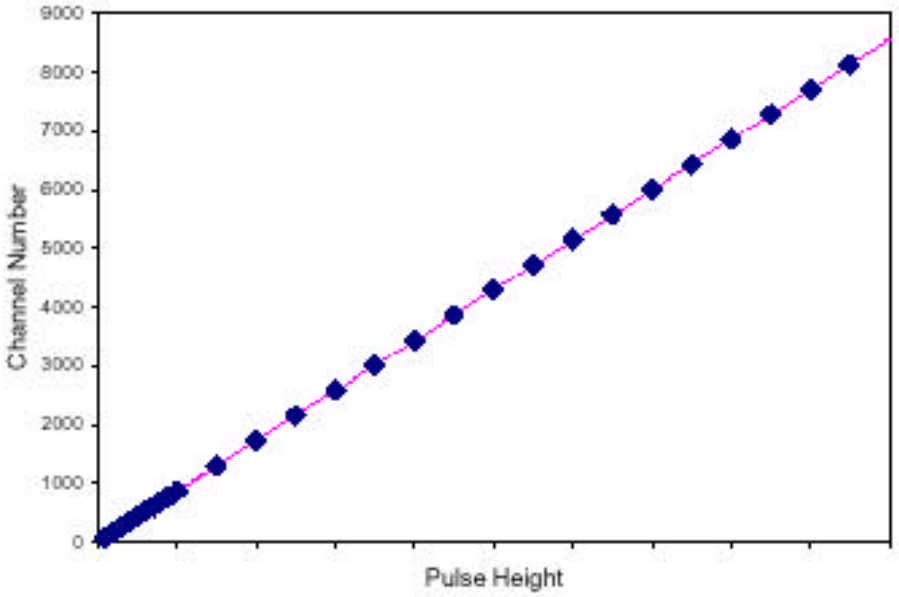
$V_{in} = (1/2)V_{in}(max)$ => output = 101010...

$V_{in} = V_{in}(max)$ => output = 111111...

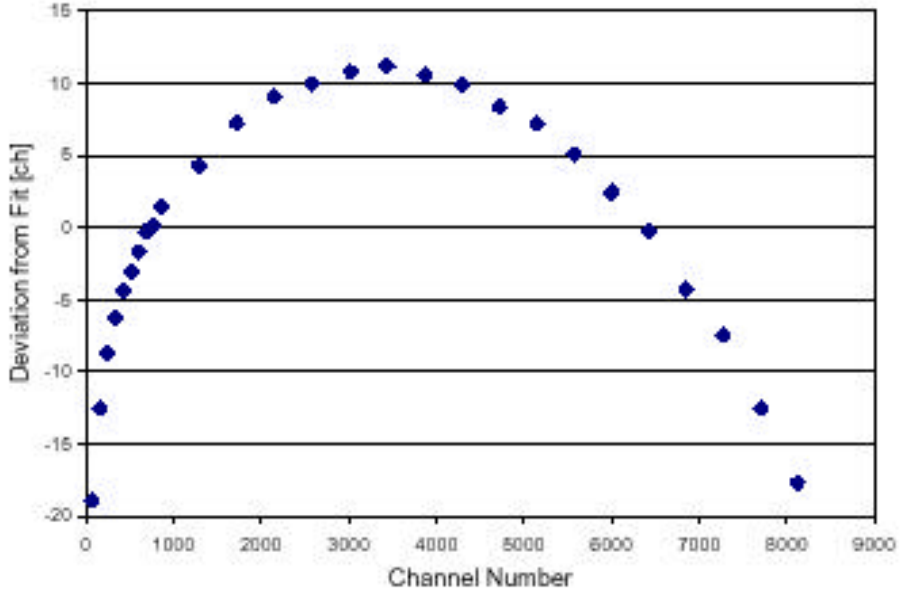
the higher the input voltage, the more 1's at the serial digital output.

Integral non-linearity

- Output value D should be linearly proportional to V
- Check with plot



- For more precise evaluation of INL fit to line and plot deviations
- Plot D_i-D_{fit} vs nchan



Differential non-linearity

- Measures non-uniformity in channel profiles over range

  DNL = $DV_i / \langle DV \rangle - 1$

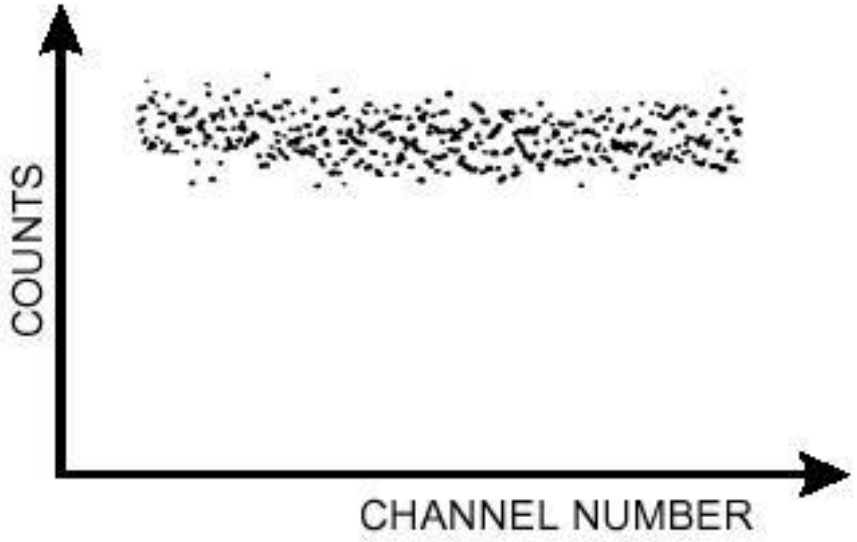
  DV_i = width of channel i

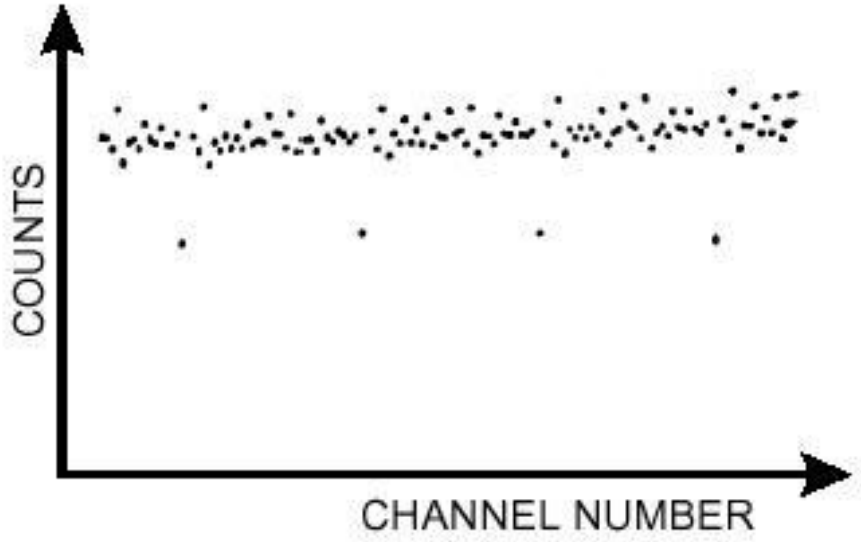
  $\langle DV \rangle$ = average width

- RMS or worst case values may be quoted

  DNL ~ 1% typical but 10^{-3} can be achieved

  can show up systematic effects, as well as random





Resolution

- To convert an analogue value, eg voltage, to digital two parameters are required

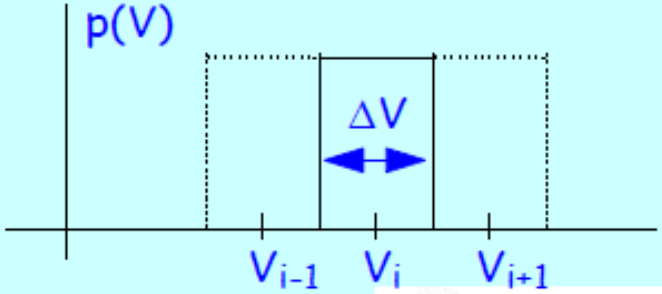
  range and number of bits

  quantum = $\Delta V = (V_{max}-V_{min})*2^{-N}$ referred to as 1LSB (least significant bit)

- eg 10 bits = $2^{10} = 1024$, $V_{max}-V_{min} = 1V$ => $\Delta V = 1V/1024 \approx 1mV$

- Ideal ADC behaviour

  probability vs amplitude

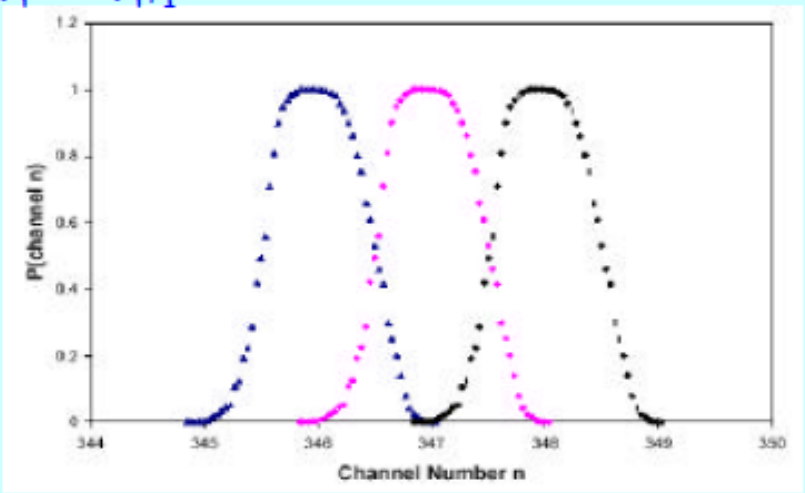


- Real ADC behaviour

  noise in digitisation process

  smears resolution

$\sigma_{noise} < \Delta V/4$



Other variables

- Conversion time
  - finite time is required for conversion and storage of values
  - may depend on signal amplitude
  - gives rise to dead time in system
  - i.e. system cannot handle another event during dead time
  - may need accounting for, or risk bias in results
- Rate effects
  - results may depend on rate of arrival of signals
  - typically lead to spectral broadening
- Stability
  - temperature effects are a typical cause of variations
- A partial solution to most of these problems is regular calibration, preferably under real operating conditions, as well as control of variables

Non-linear ADC

- A integrating system for measuring x-ray photons for crystallography, measuring spots. The most intense spots contain up to ~10^9 photons, the weakest just a few. Measure N in spot

  aim: achieve 1% resolution

  using a 10-bit ADC (cost)

  assume 1V range

  1V = largest signal, defines G_1

  $N < 10^4$ $\sigma(N)/N > 1\%$

  defines smallest signals

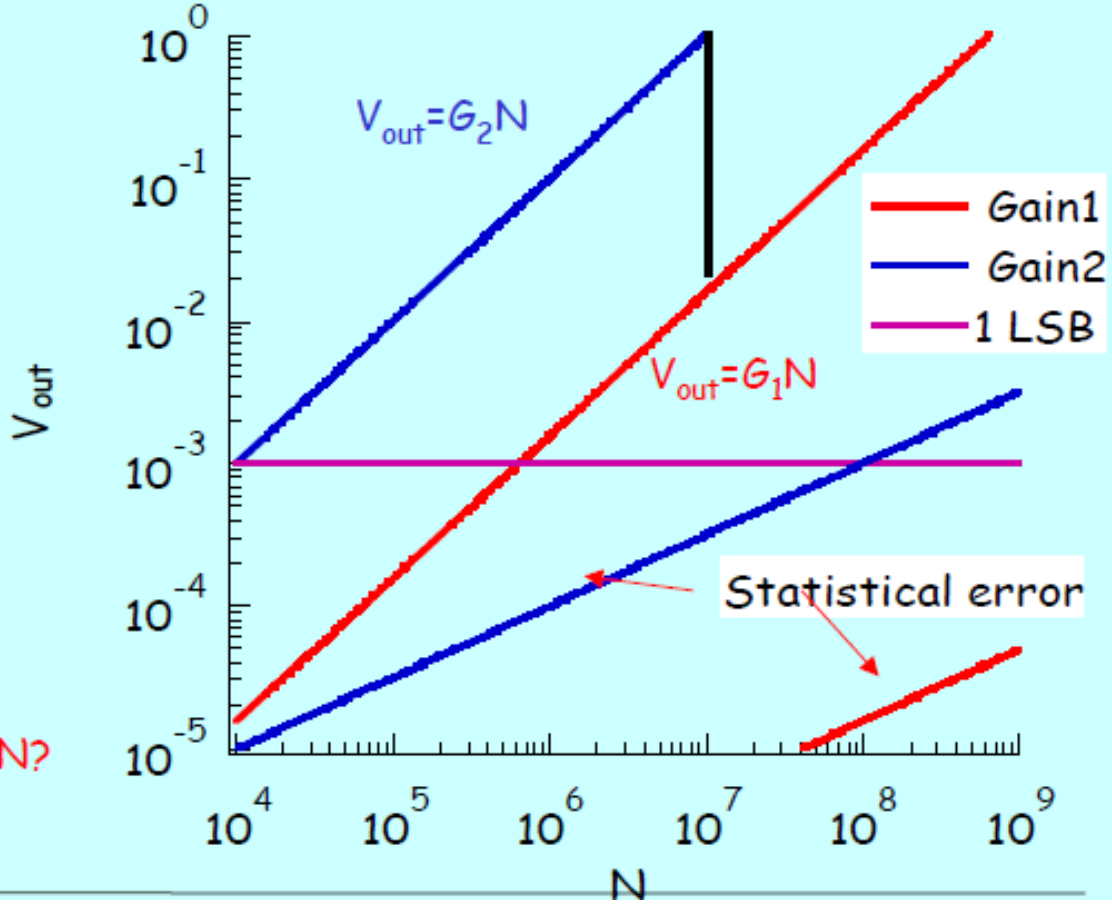
  but ADC LSB > signal

  Increase small signal gain G_2

  Select output in ADC range

- Is 1% resolution achieved for all N?

  If not… ?



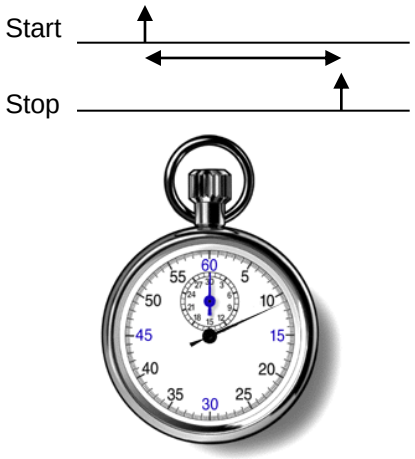
Why TDCs?

TDCs are used to measure time or intervals

- Start – Stop measurement
  - Measurement of time interval between two events:

Start signal – Stop signal

  - Used to measure relatively short time intervals with high precision
  - Like a stop watch used to measure sport competitions

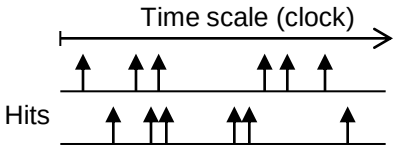


- Time tagging
  - Measure time of occurrence of events with a given time reference:

Time reference (Clock)
Events to be measured (Hits)

  - Used to measure relative occurrence of many events on a defined time scale:

Such a time scale will have limited range; like 12/24 hour time scale on your watch when having no date and year



Where TDCs?

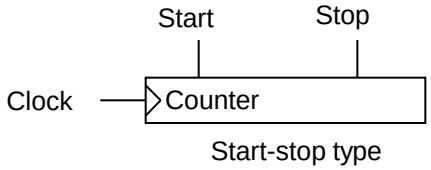
- Special needs for High Energy Physics
  - Many thousands of channels needed
  - Rate of measurements can be very high
  - Very high timing resolution
  - A mechanism to store measurements during a given interval and extract only those related to an interesting event, signaled by a trigger, must be integrated with TDC function
- Other applications
  - Laser/radar ranging to measure distance between cars
  - Time delay reflection to measure location of broken fiber
  - Most other applications only needs one or a few channels

How to compare TDCs?

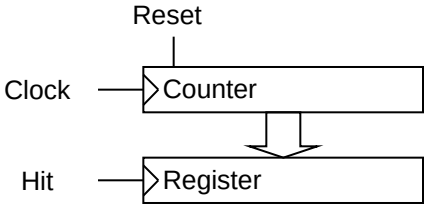
- Merits
  - Resolution
    - Bin size and effective resolution (RMS, INL, DNL)
  - Dynamic range
  - Stability
    - Use of external reference
    - Drift (e.g. temperature)
    - Jitter and Noise
  - Integration issues
    - Digital / analog
    - Noise / power supply sensitivity
    - Sensitivity to matching of active elements
    - Required IC area
    - Common timing block per channel
    - Time critical block must be implemented on chip together with noisy digital logic
- Use in final system
  - Can one actually use effectively very high time resolution in large systems (detectors)
  - Calibration - stability
  - Distribution of timing reference (start signal or reference clock)
  - Other features: data buffering, triggering, readout, test, radiation, etc.

Basic TDC types - I

- Counter type
  - Advantages
    - Simple; but still useful!
    - Digital
    - large dynamic range possible
    - Easy to integrate many channels per chip
  - Disadvantages
    - Limited time resolution (1ns using modern CMOS technology)
    - Meta stability (use of Gray code counter)
- Single Delay chain type
  - Cable delay chain (distributed L-C)
    - Very good resolution (5ps mm)
    - Not easy to integrate on integrated circuits
  - Simple delay chain using active *gates*
    - Good resolution (~100ps using modern tech)
    - Limited dynamic range (long delay chain and register)
    - Only start-stop type
    - Large delay variations between chips and with temperature and supply voltage

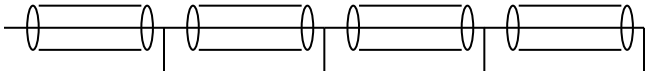


Start-stop type

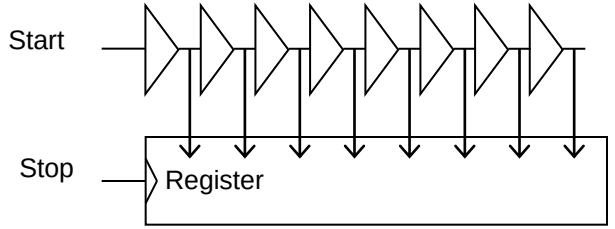


Time tagging type

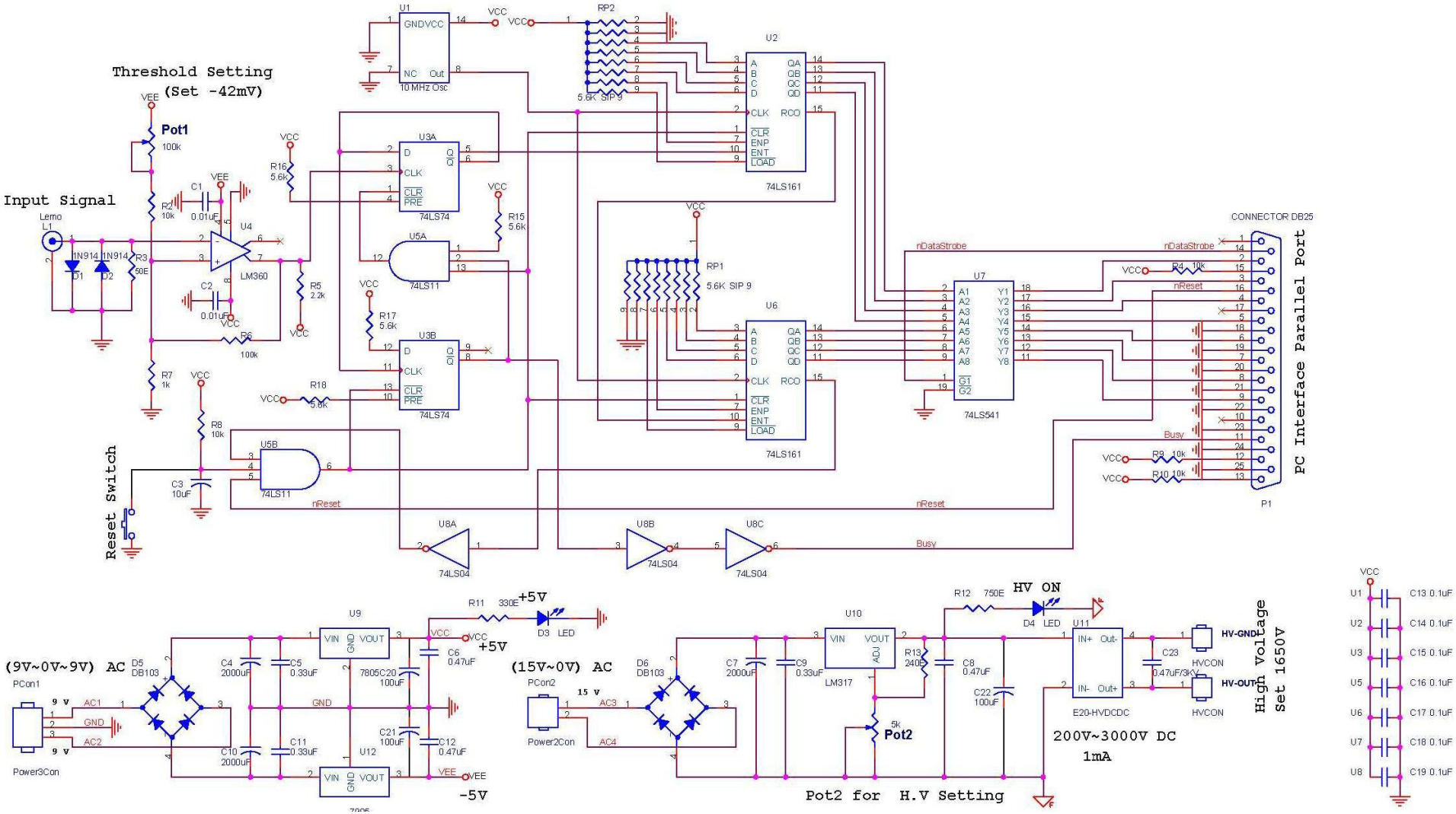
Cable delay chain



Delay chain with non-inverting gates



Counter-type TDC



December 18, 2012

LECTURE-20

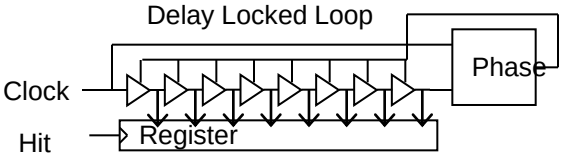
SURESH UPADHYA

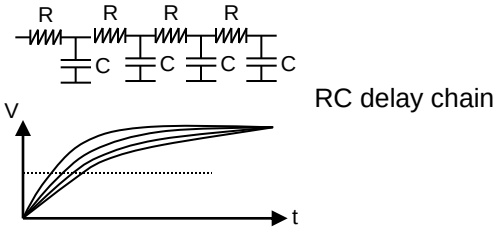
December 20, 2012

LECTURE-21

Basic TDC types - II

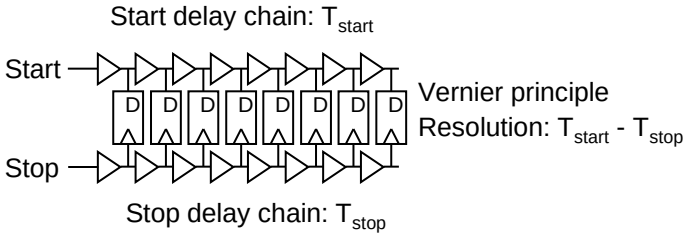
- Single Delay chain type (Contd …)
  - Delay locked loop
    - Self calibrating using external frequency reference (clock)
    - Allows combination with counter
    - Delicate feedback loop design (jitter)
  - R-C delay chain
    - Very good resolution
    - Signal slew rate deteriorates
    - Delay chain with losses; so only short delay chain possible
    - Large sensitivity to process parameters (and temperature)

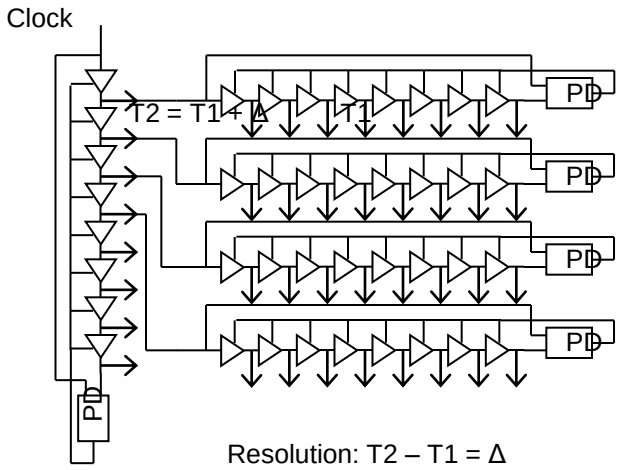




Basic TDC types - III

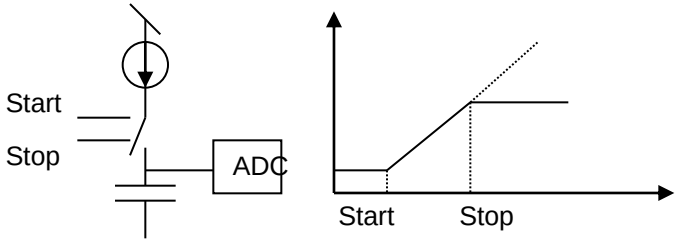
- Multiple delay chain type
  - Vernier delay chain types
    - Resolution determined by delay difference between two chains. Delay difference can be made very small and very high resolution can be obtained.
    - Small dynamic range (long chains)
    - Delay chains can not be directly calibrated using DLL
    - Matching between delay cells becomes critical
  - Coupled delay locked loops
    - Sub-delay cell resolution (¼)
    - All DLLs use common time reference (clock)
    - Common timing generator for multiple channels
    - Jitter analysis not trivial

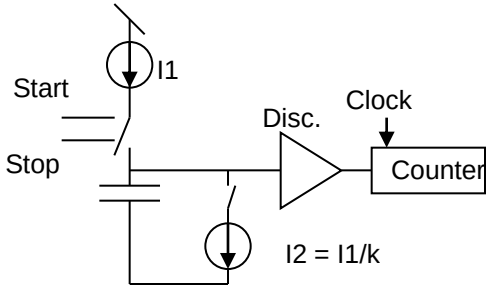


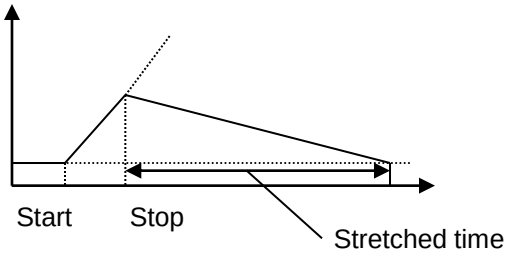


Basic TDC types - IV

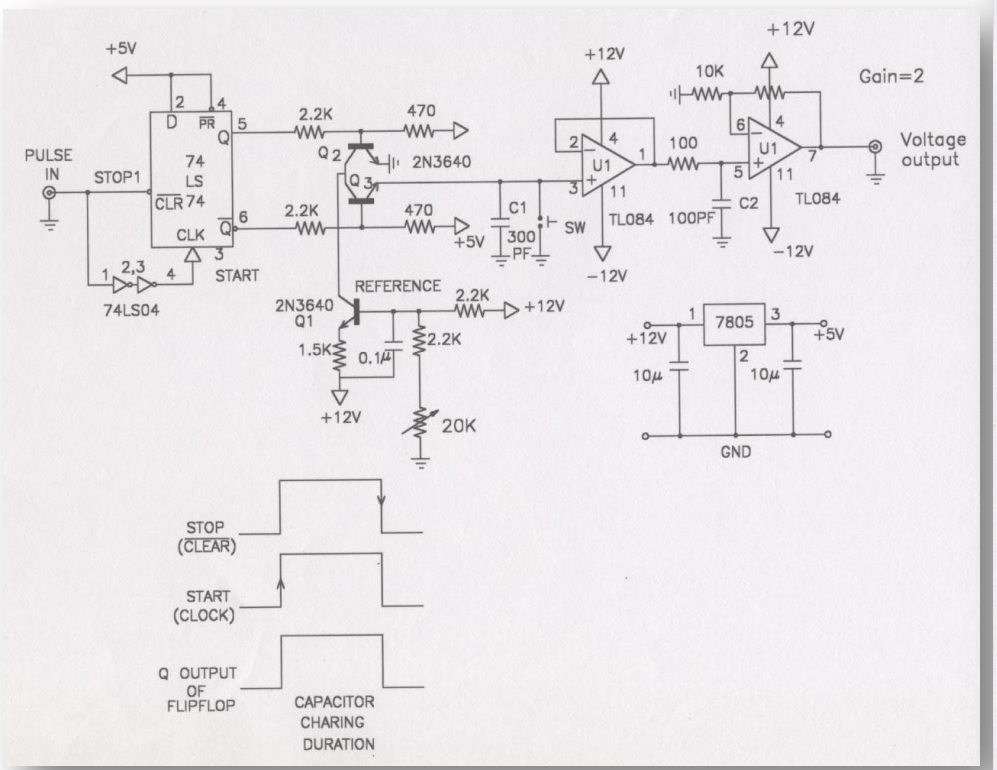
- Charge integration
  - Using ADC (TAC)
    - High resolution
    - Low dynamic range
    - Sensitive analog design
    - Low hit rate
    - Requires ADC
  - Using double slope (time stretcher)
    - No need for ADC (substituted with a counter)
- Multiple *exotic* architectures
  - Heavily coupled phase locked loops
  - Beating between two PLLs
  - Re-circulating delay loops
  - Summing of signals with different slew rates

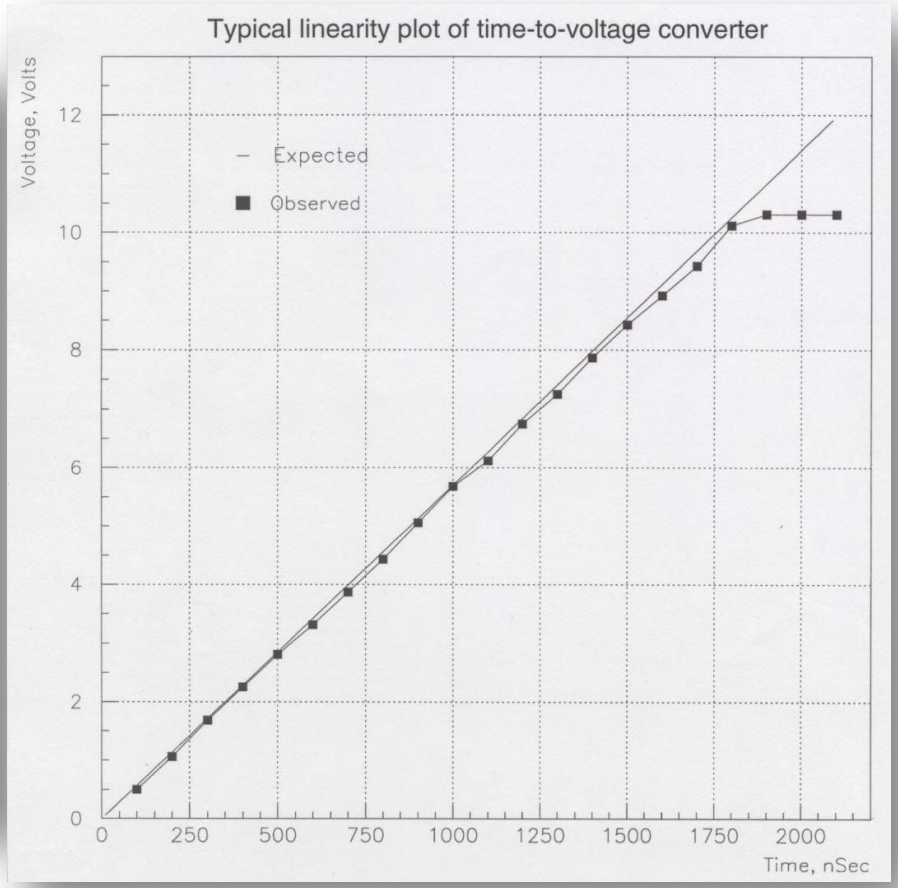




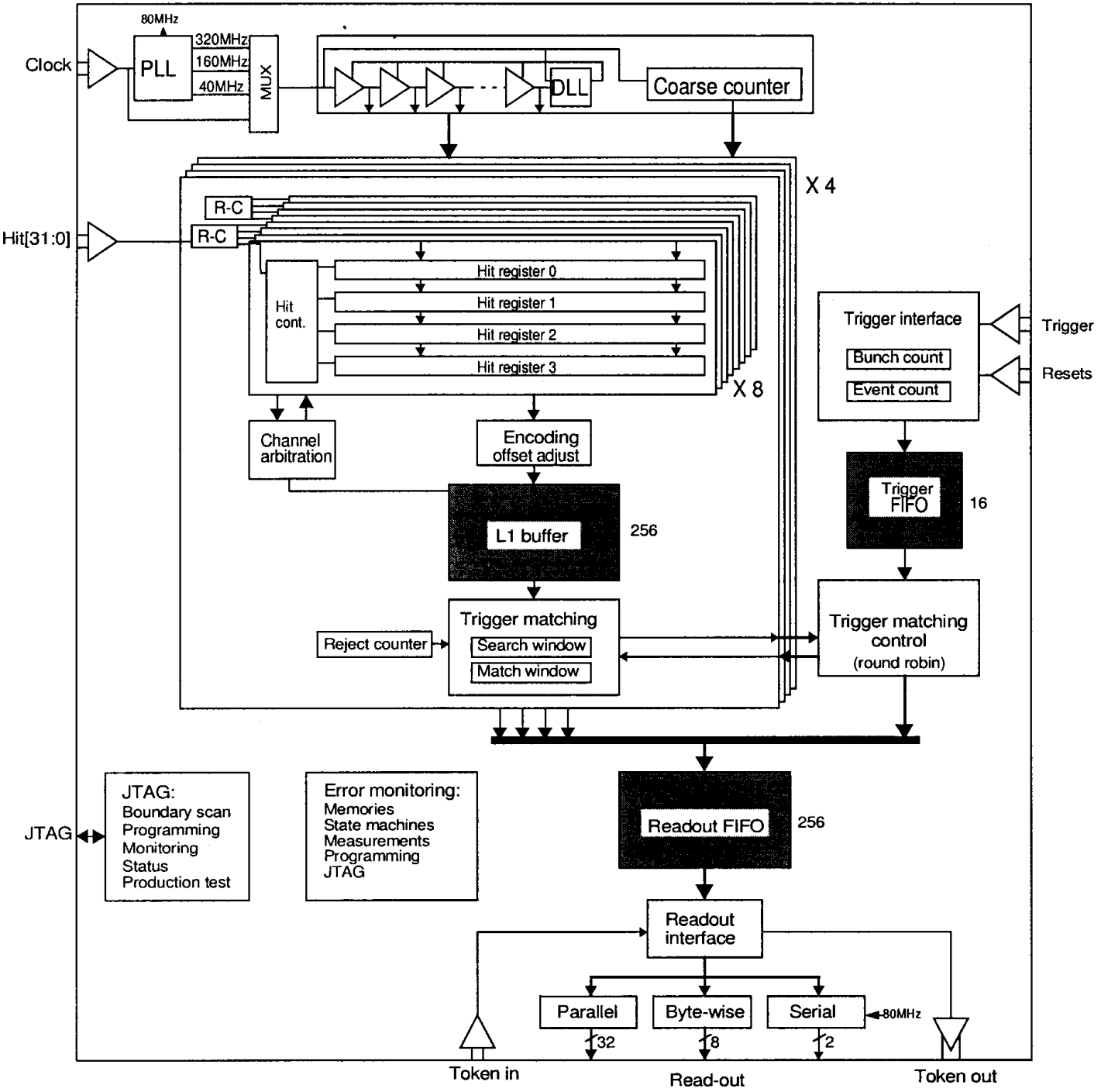


Time-to-Amplitude Converter(TAC)



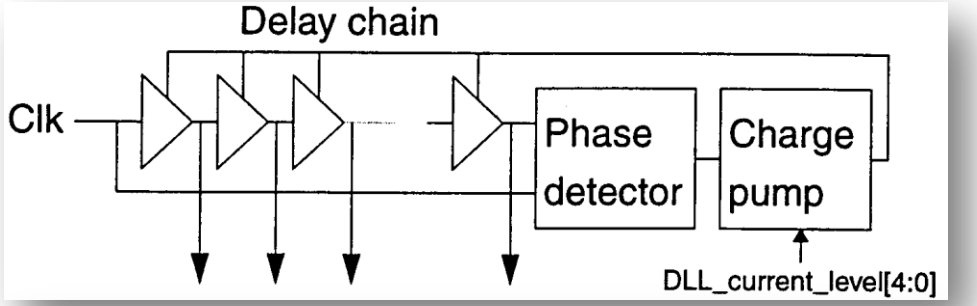


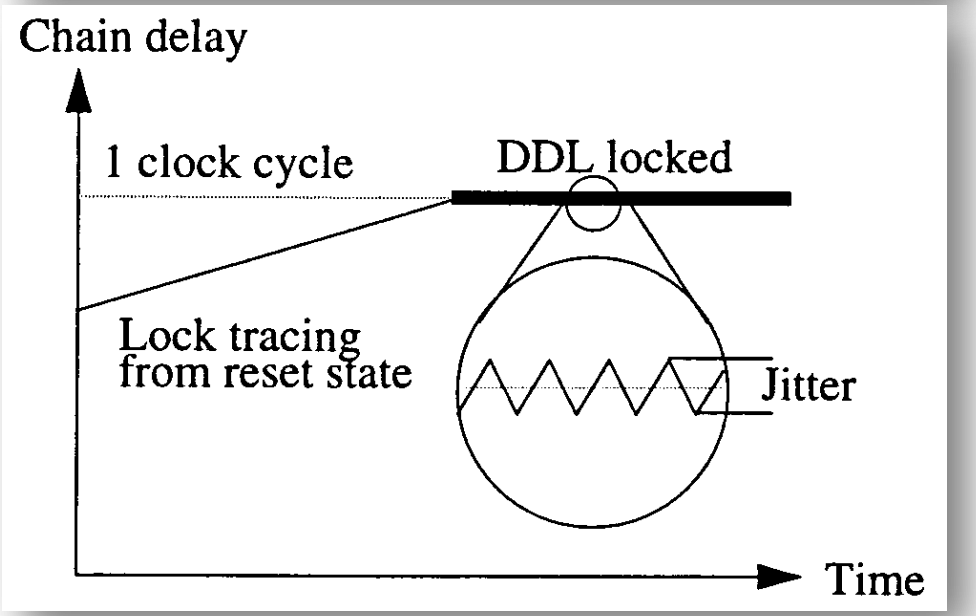
Architecture of HPTDC (ALICE TOF)



Delay Locked Loop (DLL)

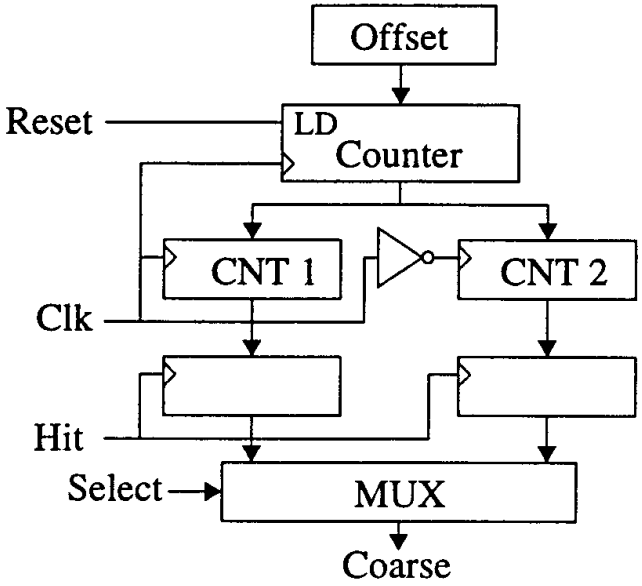
- Three major components:
  - Chain of 32 delay elements; adjustable delay
  - Phase detector between clock and delayed signal
  - Charge pump & level shifter generating control voltage to the delay elements
- Jitter in the delay chain
- Lock monitoring
- Dynamics of the control loop
- Programmable charge pump current level

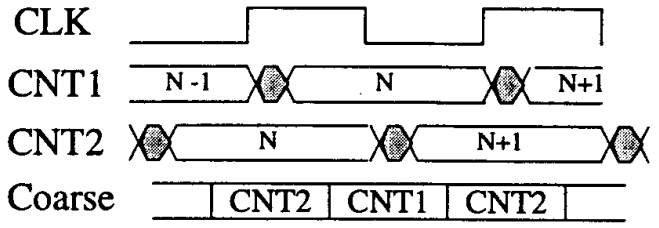


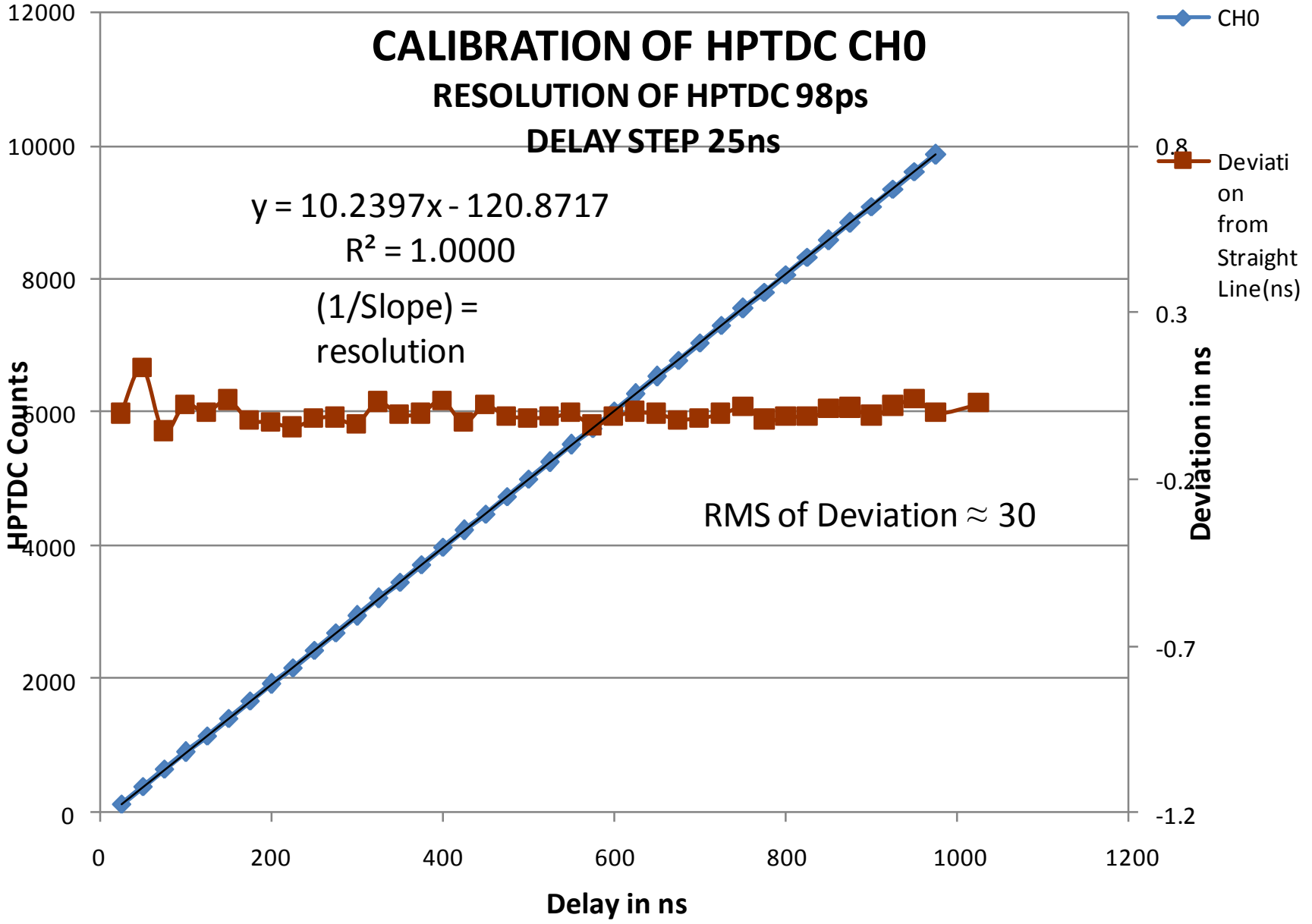


Coarse time count

- Dynamic range of the fine time measurement, extracted from the state of DLL is expanded, by
- Storing the state of a clock synchronous counter
- Hit signal is synchronous to the clocking, so
- Two count values, ½ a clock cycle out of phase stored
- At reset, coarse time counter loaded with time offset



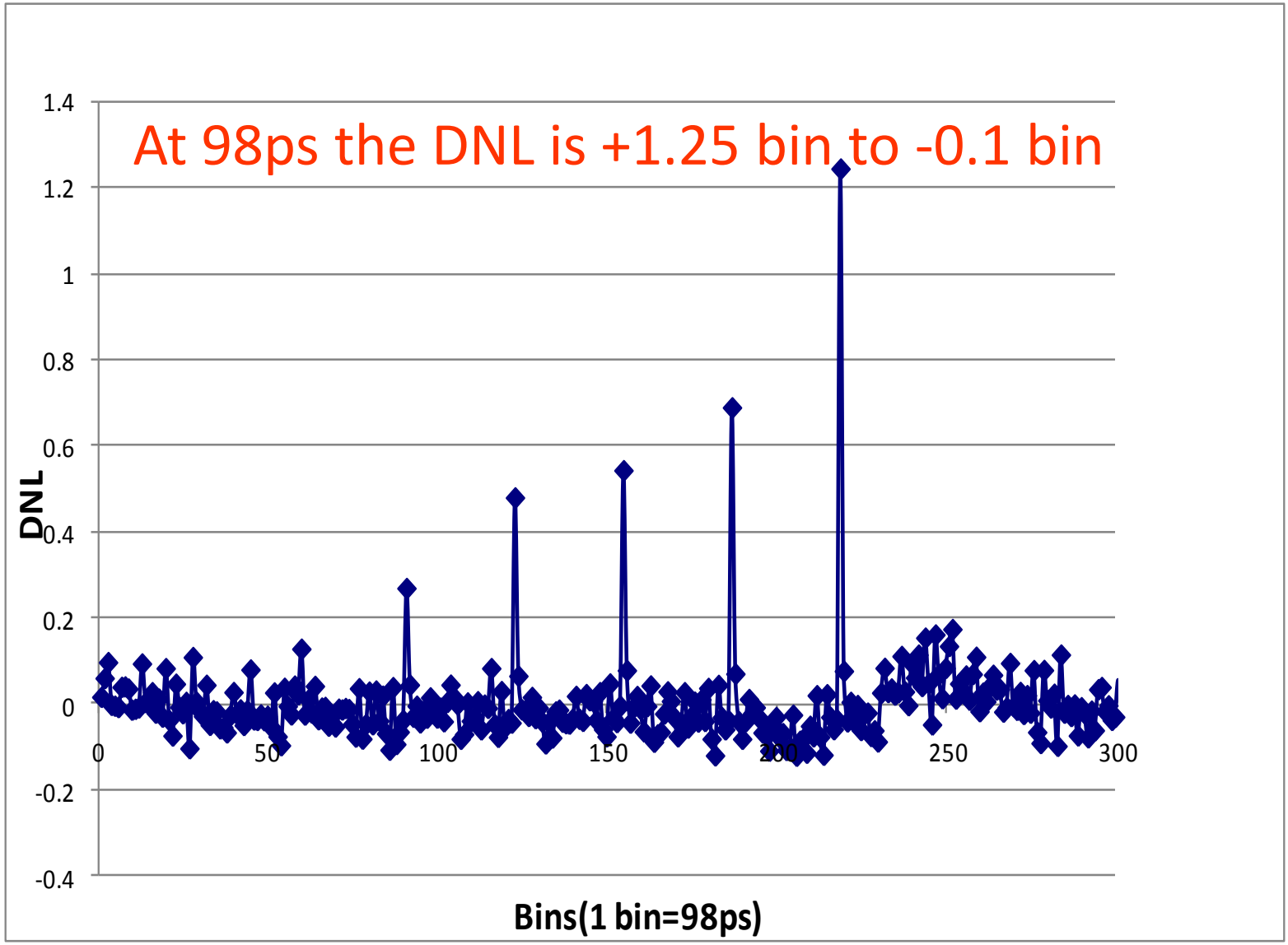



CALIBRATION OF HPTDC CH0
RESOLUTION OF HPTDC 98ps
DELAY STEP 25ns
y = 10.2397x - 120.8717
R² = 1.0000
(1/Slope) = resolution
RMS of Deviation ≈ 30
HPTDC Counts
Deviation in ns
Delay in ns
CH0
Deviation from Straight Line(ns)
12000
10000
8000
6000
4000
2000
0
0.8
0.3
-0.2
-0.7
-1.2
0
200
400
600
800
1000
1200

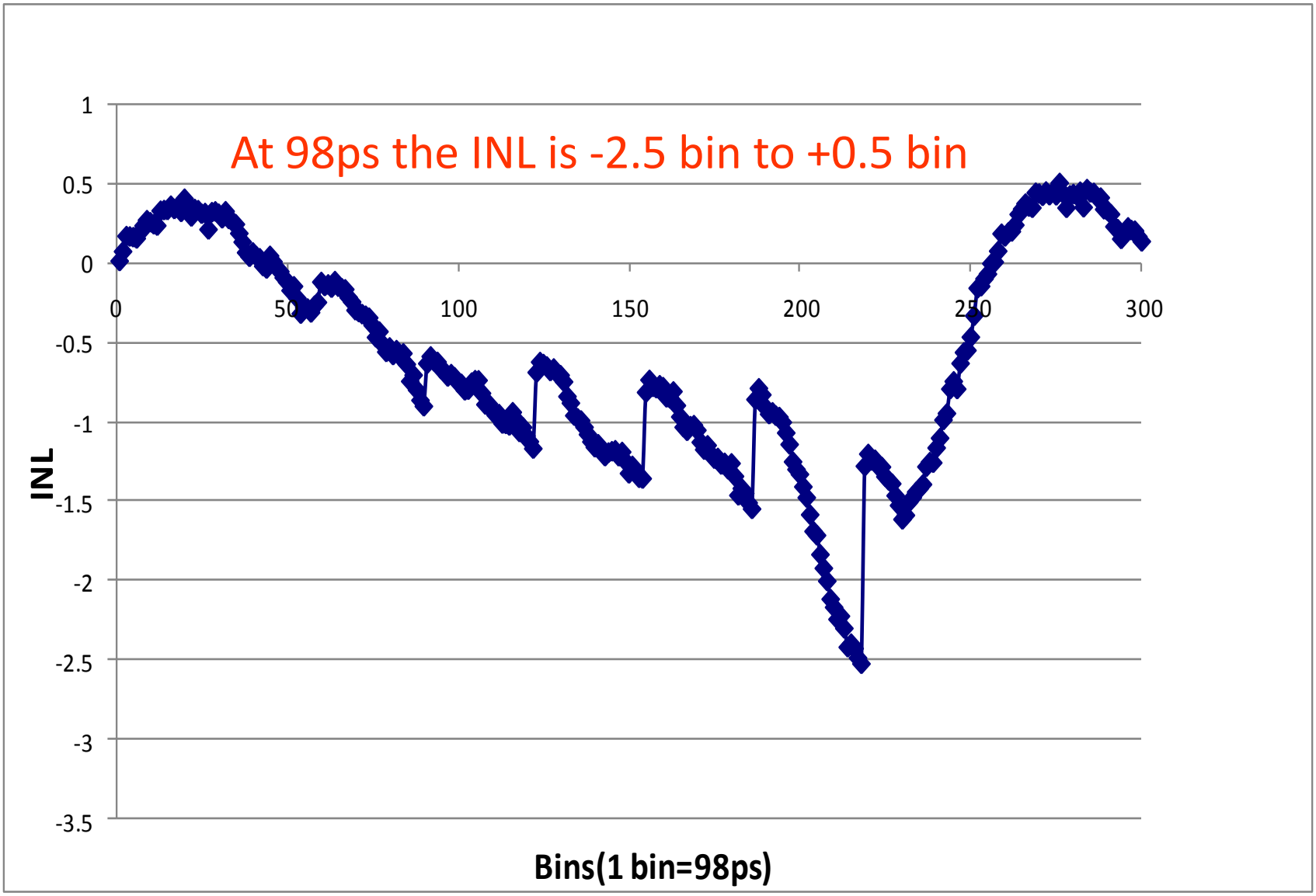
HPTDC's DNL and INL

- Differential Non-Linearity(DNL) is defined as the variation of any code from an ideal 1 LSB step.
- DNL(n) = (Actual(n)/Expected(n)) – 1.
- Integral Non-Linearity (INL) is the deviation of the transfer function from a reference line measured in fractions of 1 LSB using a best straight line. INL is simply the integral of the DNL.
- So if we can get the DNL then we can compute the INL.
- In HPTDC the base clock is 40 MHz i.e. 25ns so the DNL pattern repeats every 25ns.

HPTDC's DNL test result



HPTDC's INL test result



HPTDC's DNL/INL data correction

- The fixed pattern in the INL is caused by 40 MHz cross talk from the logic part of the chip to the time measurement part .
- As this crosstalk comes from the 40MHz clock, which is also the time reference of the TDC, the integral non linearity have a stable shape between chips and can therefore be compensated for using the LSB bits of the measurements.

Test Condition	Effective resolution (RMS)
98ps resolution	64ps
98ps resolution after INL correction	34ps
24ps resolution	58ps
24ps resolution after INL correction	17ps

December 28, 2012

LECTURE-22

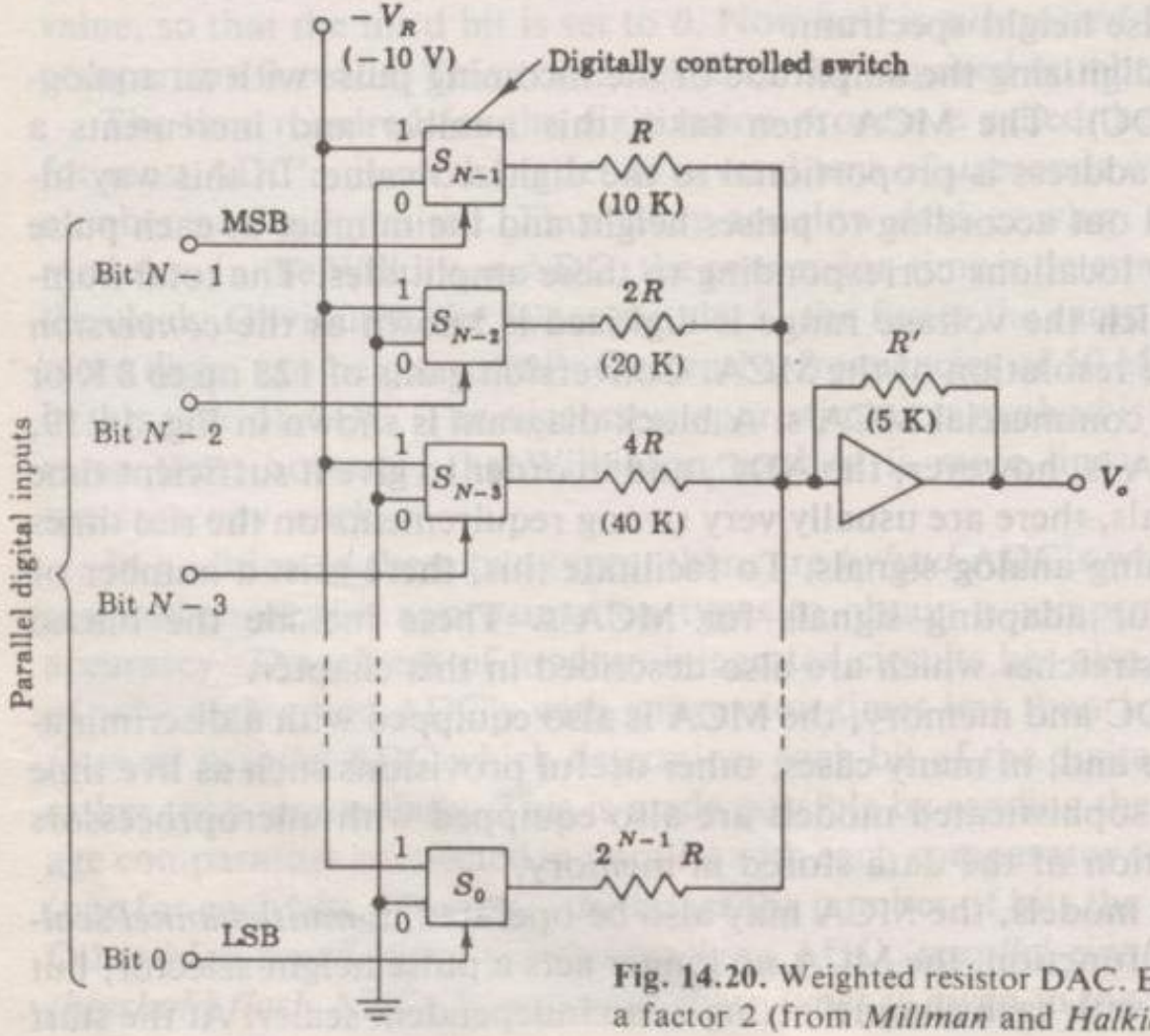


Fig. 14.20. Weighted resistor DAC. Each resistor value increases by a factor 2 (from *Millman* and *Halkias* [14.1])

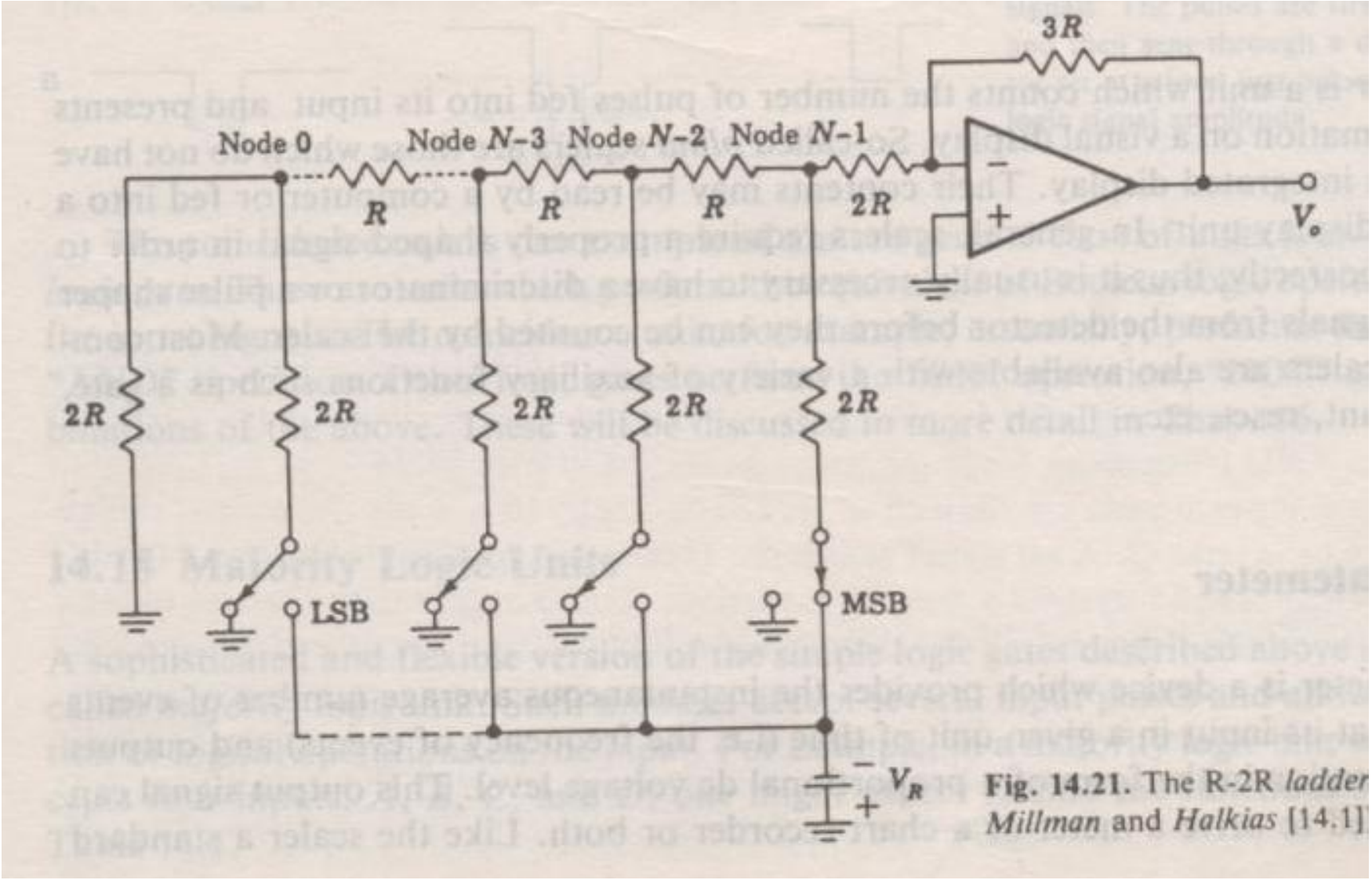
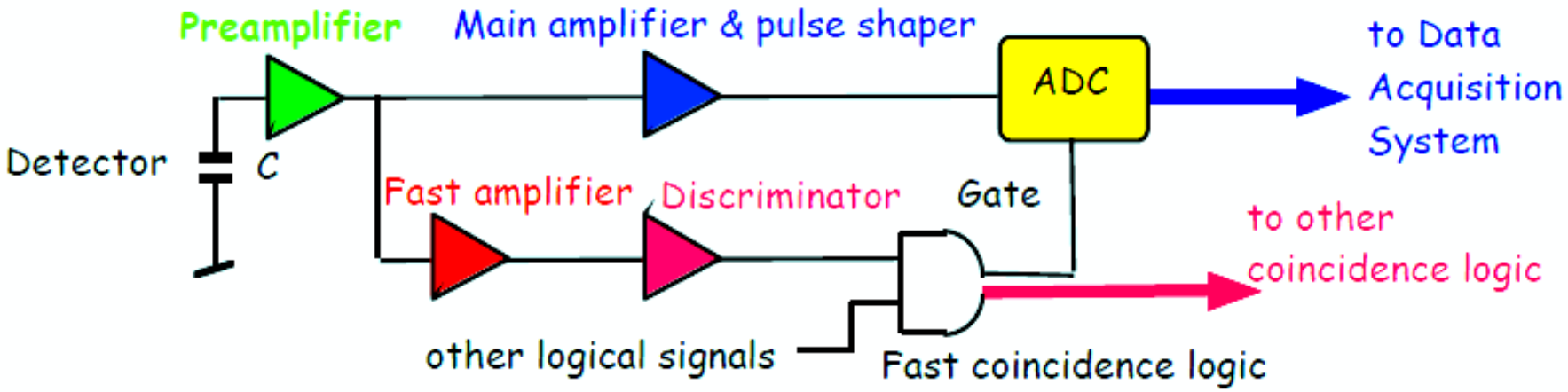


Fig. 14.21. The R-2R *ladder*
Millman and *Halkias* [14.1]

Amplifier systems for spectroscopy

- typical application - precise measurements of x-ray or gamma-ray energies



- pre-amplifier *first stage of amplification*
- main amplifier - *adds gain and provides bandwidth limiting*

  ADC - analogue to digital conversion - *signal amplitude to binary number*

- fast amplifier and logic -

  start ADC ("gate") and flag interesting "events" to DAQ system

  - most signals arrive randomly in time.

  Other logic required to maximise chance of "good" event, eg second detector

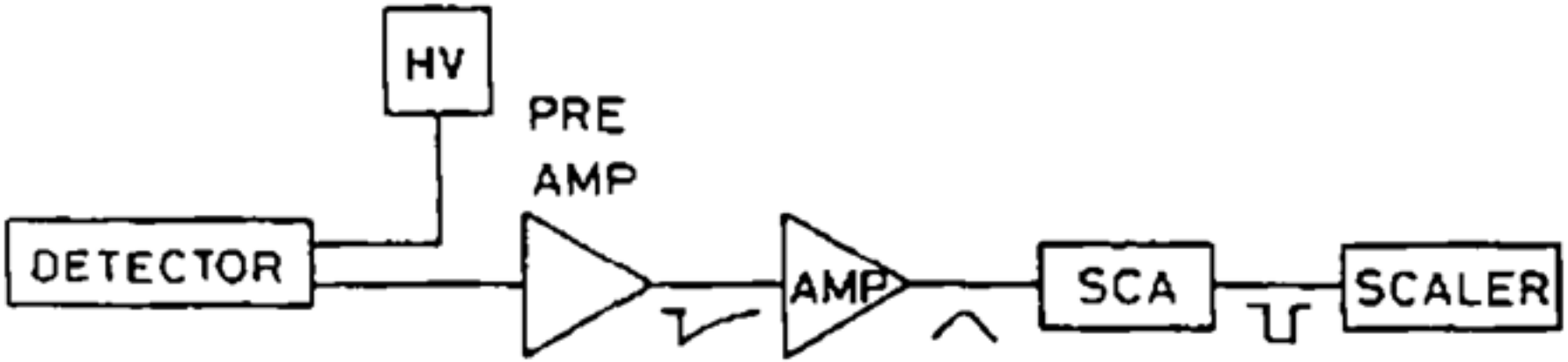
MCA Vs MCS

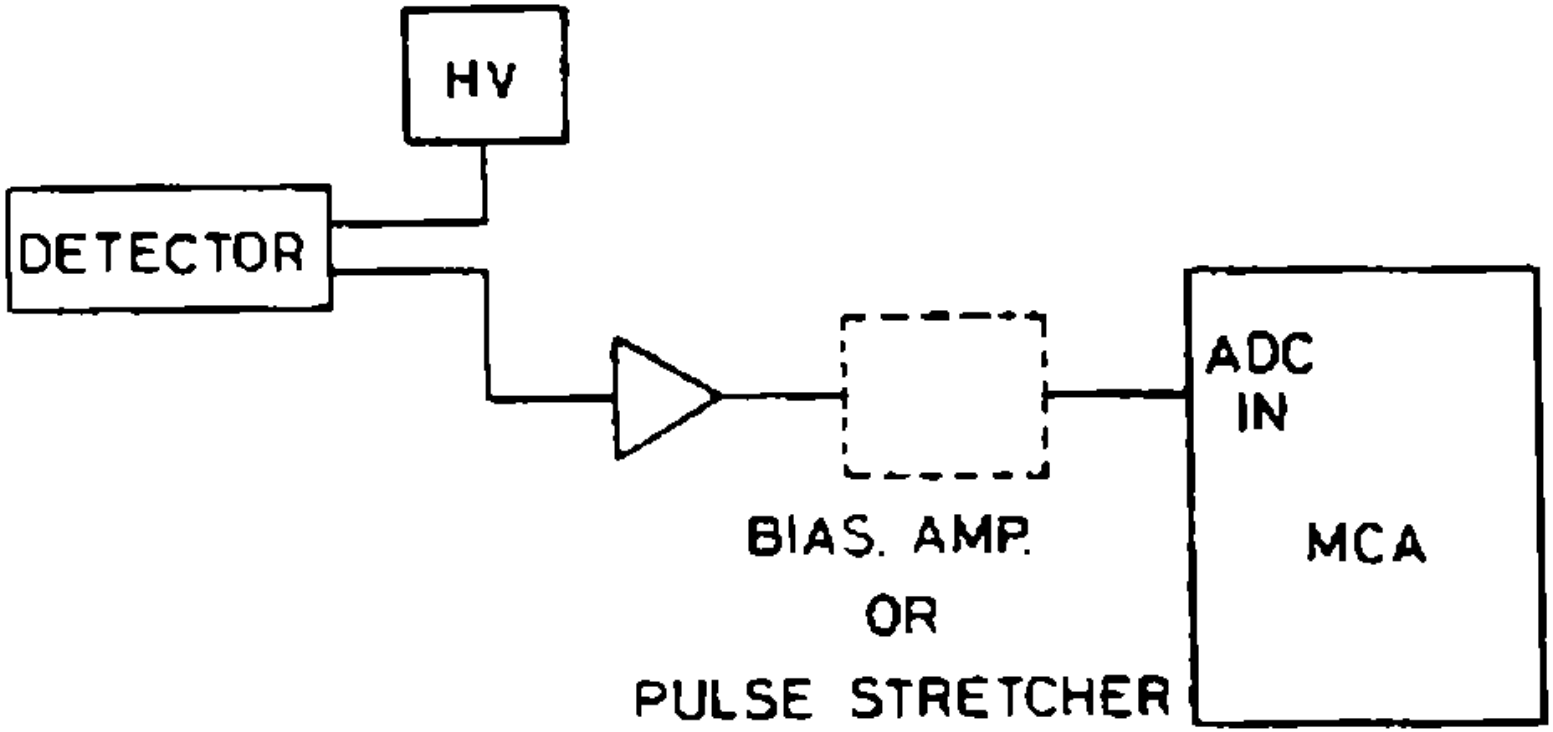
MCA

- Multi Channel Analyser
- Uses ADC
- Sorts incoming pulses according to their pulse heights
- Channel represent pulse height
- Total channels → Conversion gain
- Application: Spectroscopy

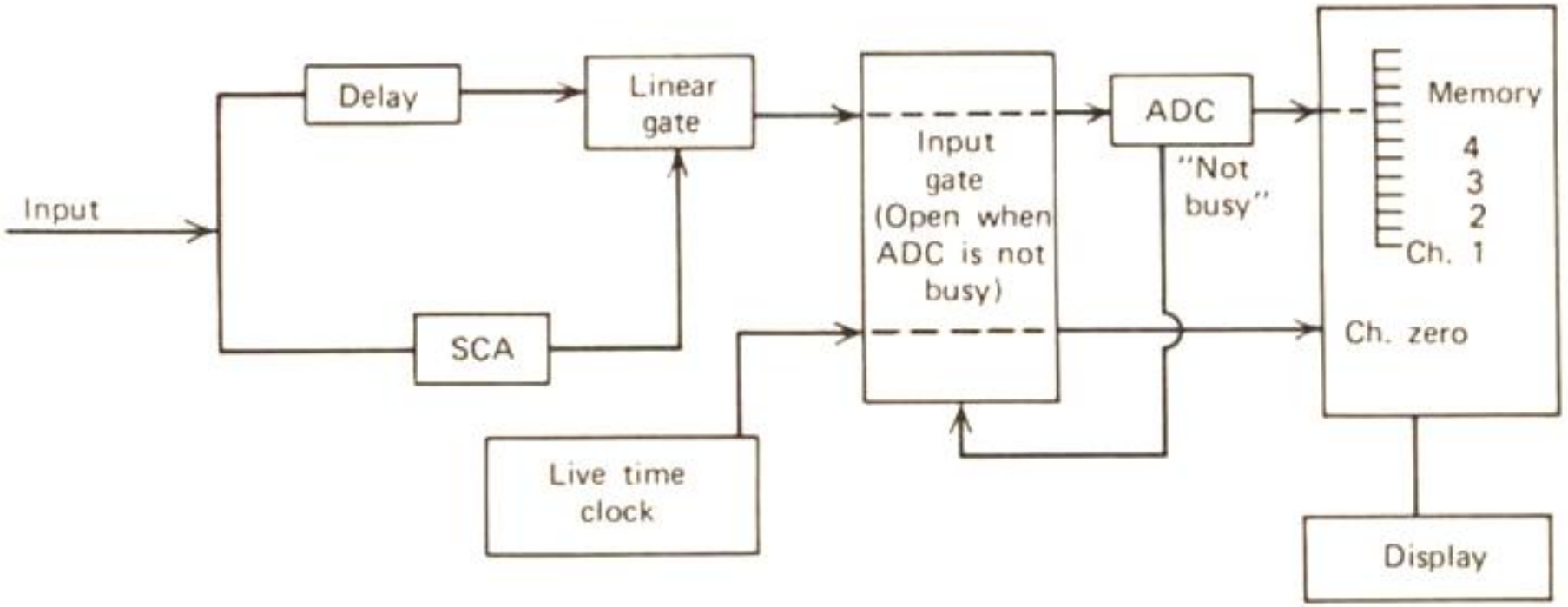
MCS

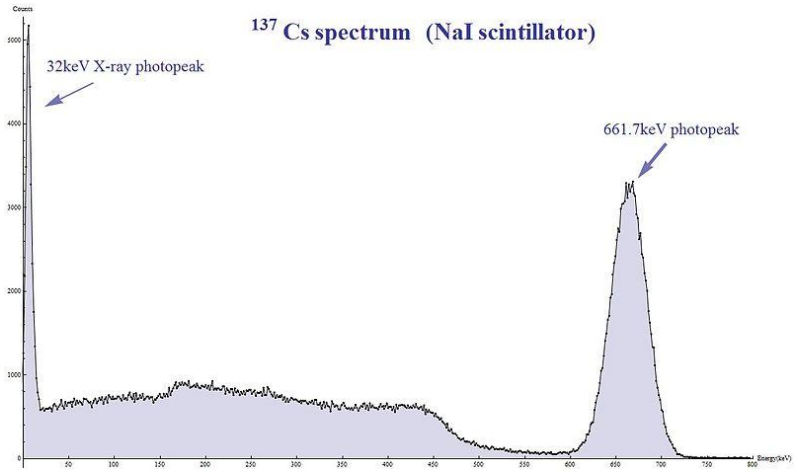
- Multi Channel Scaler
- Uses comparator and counter
- Counts incident pulse signals (regardless of amplitude) for a certain *dwell time*
- Channels represent bins in time
- Application: Decay curves of radioactive isotopes


HV
PRE
AMP
DETECTOR
AMP
SCA
SCALER

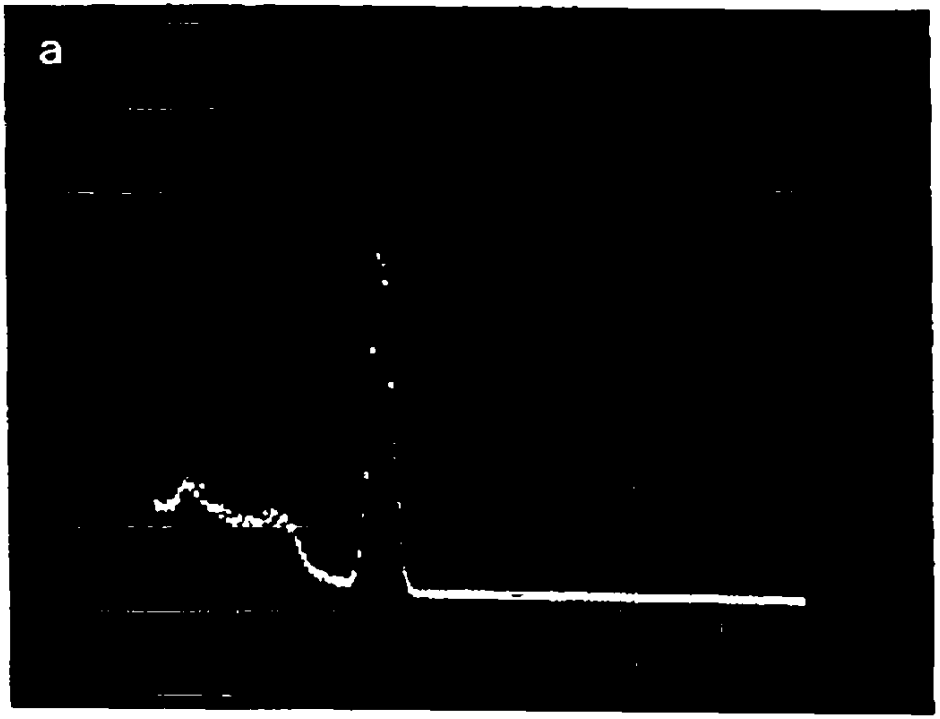

HV
DETECTOR
ADC
IN
MCA
BIAS. AMP.
OR
PULSE STRETCHER

Functional block diagram of a MCA





Two gamma rays with energies of 1.17 and 1.33 MeV



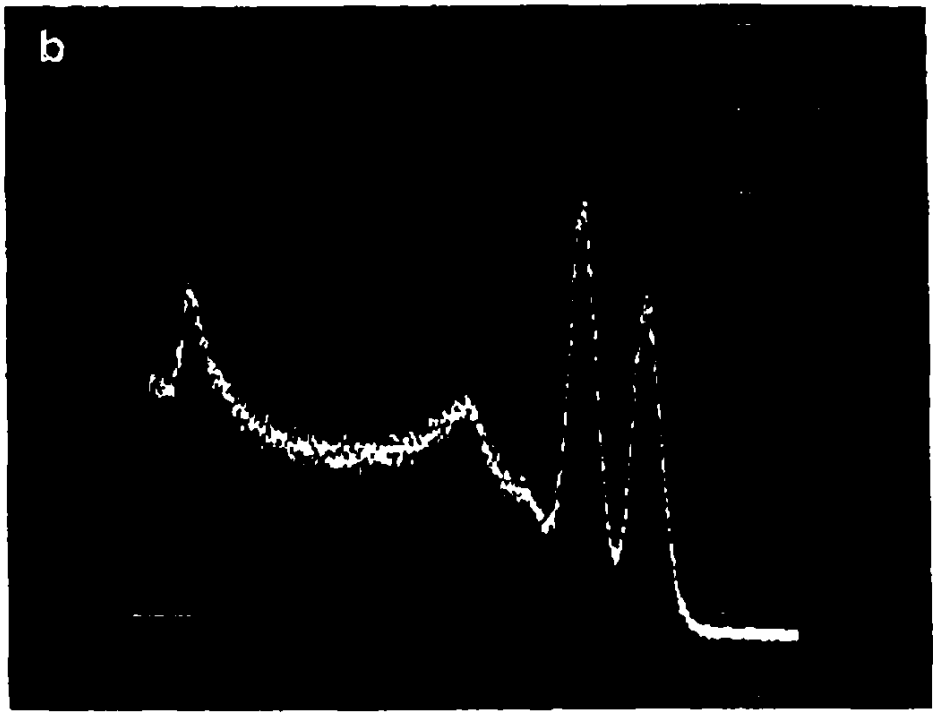


Fig. 15.6. Sample MCA pulse height spectra from a NaI detector: (a) ^{137}Cs, (b) ^{60}Co