Personal computer controlled data acquisition systems for Proton Decay experiments*

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Abstract

Proton Decay experiments are being conducted at a depth of about 2000 metres below surface in the gold mines situated at Kolar Gold Fields for the last seven years. In these experiments data acquisition system has to handle simultaneously about 4000 signals and the data collection should be completed with as little dead time as possible. This required a carefully planned system approach. This has been accomplished by means of a Z-80 based standard Personal Computer which controls a number of higher-end clusters that are arranged in a parallel processing configuration and having autonomous control status. These clusters are implemented by microprocessor based (slave) systems, which have under their control several front-end modules with distributed functions and simple controls. Along with control and local resource management functions, slave processors take responsibility of on-line monitoring of the parameters of transducers as well as the functions of circuits under their control.

An indegenously designed parallel communication link between the higher-end clusters and the host PC is discussed. Communication interface modules, communication line characteristics, network specifications and general data transfer protocols are out lined. General control and

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central resource management functions such as controlling and monitoring the functions of slave processors, data storage in bubble cassette and floppy disk are presented. Additional responsibilities which include acting as an interface between the user and slave processors, decision making and other auto-functions, real time clock support, reference data maintenance and log book keeping are discussed in detail. Several off-line utilities like preliminary data analysis and customised file management are mentioned briefly.

Software characteristics such as speed, modularity, flexibility, friendly user interface and error handling capability are briefly discussed.

Finally a critical evaluation is made of the PC used by us in terms of (a) builtin facilities, (b) operating system support, (c) many software modules that are transparent to user and (d) limitations encountered during the design of the system and its operation over a period of few years.

Introduction

Experiments are being conducted at a depth of about 2000 metres in the gold mines situated at Kolar Gold Fields over the last seven years to search for nucleon decay events, magnetic monopoles, Kolar events etc.[1,2].

Detectors built for these experiments comprise several thousand channels and the data acquisition systems (DAS) have to handle signals from all the channels simultaneously. Design criterion of these DAS is that they have to carryout several functions concurrently with minimum dead time. To accomplish this effectively a *multiprocessor network system concept* is adapted with a personal computer configured as system manager.

1 Brief description of the detector

The detectors are configured as fine-grain calorimeters comprising an array of proportional counters. These are arranged in horizontal layers, stacked one above the other, with the consecutive ones orthogonal to each other. The proportional counters, the basic units called channels hereafter, are prepared from sealed iron pipes of cross-section 10cm X 10cm and filled with special gas mixtures. They are activated by applying a DC voltage of 3 KV on the central anode wire. The first detector, built in 1980, had 1400 channels; the second one built in 1985 has a central detector surrounded by a veto-jacket comprising a total of 4000 channels. The third detector, now under construction, has 1500 channels out of which 500 are made with counters of smaller cross-section.

Each counter is separately instrumented to obtain pulse height (ionisation) and timing information on the passage of a charged particle through it. The data acquisition system (DAS) has to handle all channels simultaneously to record, store and retrieve data. The DAS employed in these experiments have evolved with time using the state-of-the-art technology in semiconductor devices, computers and data readout fields. While the electronics for the first detector was completely hardwired except for some monitoring chores, an 8-bit PC based system is developed indegenously to facilitate several aspects of data handling in the later detectors.

2 Guide lines for the DAS design

The DAS employed for the experiments are designed on the following special guide lines because of which they posses many special features, besides more common characteristics of any system.

1. Various parameters of the transducers and various functions of DAS modules should be monitored thoroughly. This job has to be carriedout concurrently with event data recording.
2. Monitor cycle time should be kept to a minimum.
3. Since the detectors are operated continuously and unattended, necessary auto, watchdog, interlocking, fault-tolerant and simple decision making functions should be incorporated in DAS design.
4. Since the detectors are operated in hostile underground environments, data storage media chosen has to be highly reliable and suitable otherwise.
5. Necessary service aids should be provided to the user for solving simple problems as well as analysing the data roughly at the experiment site.

The following sections outline the hierarchy of circuit modules in the DAS that are being employed for recent experiments.

3 Front-end readout modules

The pulses given by the proportional counters on incidence of charged particles are usually a few mv in amplitude with a rise time of about 500ns. These pulses are amplified with a gain of about 80 and their fall-times are adjusted to 10 micro seconds. These amplified analog pulses (*linear pulses*) are converted to TTL compatible pulses (*log pulses*) whose widths are proportional to logarithmic values of pulse heights. This is achieved by a feed back comparator (discriminator) with a bias of 100 mv and hysterisis (used for discriminating noise) of 18 mv. The log pulses are driven to front-end digital data acquisition modules (FEDDAMs) as bunches of 8 channels (*box*). Analog pulses of a box are multiplexed and are driven to front-end analog data acquisition modules (FEADAMs) (Fig. 1).

Each FEDDAM contains 58 units of log pulse processing modules for a layer required for event recording, log pulse monitoring and trigger generation, in addition to pulse receivers and drivers. Log pulse profiles are digitised in dedicated static RAMs with an universal clock of 5 MHz frequency supplied by *trigger generator*. These RAMs are refreshed with new data with a cycle time of about 205 ms. *Trigger pulse* which initiates data collection from the static RAMs vetoes this refreshing cycle and freezes the log pulse for further processing. As far as log pulse monitoring is concerned, channel identification and signal selection is done on FEDDAMs. Pre-trigger generator which is also included in FEDDAMs contain several pre-programmed chips, which generate pre-trigger pulses (Fig. 2).

On the other hand, FEADAMs contain preparatory analog pulse processing modules for a layer, necessary to record and monitor the linear amplitudes. Each FEADAM contains two sets of peak holder and sample-hold chains (one for event data recording and the other for linear pulse monitoring) in addition to some local control electronics.

4 Higher end clusters

These are Z-80 based, single board computer like systems. In the experiment each of these clusters manages general control, event data recording and monitoring functions for 8 layers of the detector. The higher end clusters work independent of each other except during the time of communication with the system manager to receive commands and request the usage of centralized resources and data transfers. Thus they are intelligent enough to take *minor* decisions while executing their functions (Fig. 3).

Higher-end clusters are so designed that they are highly modular in both hardware and software aspects. Each unit is realized on a pair of PCBs. The card # 1 is a general purpose single-board computer which contains the CPU, buffers, memory, communication interface and a parallel I/O interface. This board alone or with necessary interfaces can be used in the network for any application. in fact, one such board is used as the trigger generator controller.

A higher-end cluster operates at 4 MHz clock and has 64 K memory on-board. System monitor is programmed in an 8Kb EPROM. About 32Kb RAM space is used for monitor data storage and the remaining area is used for event data buffers, work area etc. A parallel I/O interface (designed as of general purpose) is used in the experiment to interface higher-end cluster to analog data controller.

Card # 2 is exclusively designed for some specific system requirements. This card includes control circuitry for preliminary data storage in FEDDAMs and for data collection after receiving a trigger pulse. This card also contains control clusters and pulse width measurement counters for log pulse monitor. A general purpose monitor execution timer is also provided on this card.

Analog data controller is designed with the concept of *extended CPU bus*. This is equivalent to higher-end cluster as far as system component hierarchy is concerned. Higher-end control for analog data recording and monitoring, analog to digital converter and the accessory circuits are included in the analog data controller module.

5 Trigger generator

This is one of the important components of the DAS. Depending on the aims of the experiment and topology of the detector, several sets of *trigger conditions* are laid out. These conditions are formulated keeping in mind, several phenomenon and characteristics regarding a variety of signals inside and outside of the detectors. Trigger conditions are programmed in trigger generator modules. Trigger generator will have a constant *vigil* on the detector, and generates *trigger pulse* on detecting coincidence of any set of trigger conditions. Trigger pulse is sent to all higher-end clusters to initiate event data collection from front-end data acquisition modules and is also sent to system manager to commence data storage and log book updating (Fig. 4).

In addition to the generation of trigger pulse, trigger generator has additional duties like providing an *universal clock* to all higher-end clusters for data synchronisation, identification of the type of trigger and monitoring the pre-trigger rates.

Shaped pulses of a layer are used to generate pre-trigger pulses on the FEDDAM. Pre-trigger signal buses carry these signals from all FEDDAMs to trigger generator modules where the final *trigger pulse* is generated. Operations of trigger generator are locally controlled by a higher-end cluster (*Trigger generator controller*). System manager sets the trigger conditions and controls *main gate* for trigger pulse.

6 Network

The higher-end clusters which operate autonomously, are linked to the system manager through an indegenously designed network (Fig. 5). Each cluster characterised by a unique address is connected in the network as one of the stations having talker and listener status.

Identical network interface circuits are built on system manager (network controller) and clusters using standard TTL and Schottkey compatible drivers and receivers. A 25-signal twisted pair cable is used to interconnect various stations of the network in *star* arrangement; total transmission path length over the interconnecting cables is about 50 metres. The network is designed to accommodate 16 stations, but can be modified easily to include more.

Basic characteristics of the network are :

1. Data transfer rate between the station (cluster) and the controller is about 30 Kbyte/sec.
2. Data is transferred in byte-serial, bit-parallel, asynchronous mode using interlocking 4-wire hand shake technique.
3. There is only one network controller, ie the system manager. But flexibility is builtin to increase the number of controllers.
4. Data transfers can be accomplished between only one station and controller at a time.
5. Data transfers are not allowed between any two clusters.

The network bus contains several kinds of lines (Fig. 6); 8 bidirectional lines are used for data bus; cluster address bus consists of 4 lines and 4 lines carry handshake signals used for data transfers. *Look at me (LAM)* which is a *wired-OR* line is used for carrying request from any cluster for data transfers. Active state on the *flag* line indicates that data transfer is in progress. In addition to these common communication lines, the network bus carries some special function lines. These include a line for carrying *main gate* to trigger generator system, a line for issuing an artificial trigger pulse, a line for sending a device (cluster) clear, a line to bring any channel's log pulse into the network controller room etc.

7 System manager

A standard personal computer is configured as the system manager (Fig. 7). Basic specifications of the PC used are summarised in Table 1 [3]. Main functions of the PC include network and cluster control, data storage, real time and live time support, user cluster interface, reference data maintenance and log book keeping.

System manager can issue a device clear, to bring one or all clusters to a device dependent state. Thereupon it supervises the functions of each cluster. System manager sends various commands to a cluster to collect a particular kind of data or perform some special functions etc. It polls for any kind of request from clusters. All types of data transfers are done under system manager's control. Event data transfer is done sequentially from each cluster after the trigger command is issued and data collection is completed in all clusters.

Bubble memories are used for event data storage [4]. Since bubble memory devices do not contain any movable parts (as in the case of disk drives) they are well suited in the dusty environments. Also in this application where small amounts of data are written at a time, these devices proved to be faster Bubble cassettes of 128 Kbyte capacity (2048 pages of 64 bytes each) are employed. In addition to store data, bubble cassette is used to store some status information as well as for book keeping.

The PC has a built in realtime clock. This information is logged in whenever a trigger command is generated. A live time clock is also designed to provide the amount of time the experiment (*run*) is ON.

An important function of the system manager is to provide a user friendly interface with the user and higher-end clusters. Efforts have been put in to design a faster, modular, flexible and user friendly software for the system manager. The software is fully menu driven and possesses error handling capabilities.

System manager provides several facilities and tools for run control, monitor control, disk utilities, disk file management functions, I/O device control, quick check of the event and monitor data etc. To monitor the health of the basic transducers (proportional counters) and DAS, a variety of on-line monitors and tests are designed [5]. This include monitors for analysing pulse height and pulse width distributions, for monitoring the counting rates, pre-trigger pulse rates and the performance of the logarithmic converter as well as many other quick checks for daily maintenance. Simulation of trigger pulse, memory tests and check sums are some of the tests exclusively designed for evaluation of the DAS performance.

8 Conclusions

The system described in the paper is operating for more than two years. In general the performance of the system is very good. In particular the design of front-end and higher-end clusters proved to be perfect for the application. However, there are some inherent limitations as far as the system manager's performance is concerned. Firstly, since the PC used is based on an 8 bit microprocessor operating at 4 MHz clock, the overall system speed is low; system memory area is small. Also since the PC is supported by a non-standard operating system, more inhouse software development was necessitated. But these limitations donot affect the performance of the carefully designed DAS.

Now design work is in progress to configure the system manager with a 16 bit microprocessor based PC operating at 8 MHz clock and supporting MSDOS as well as the standard off-the-shelf tools and utilities.

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Caption for figures

1. Front-end readout
2. FEDDAM configuration
3. Higher-end cluster configuration
4. Schematic of Trigger generator
5. Schematic of network
6. Network bus signal layout
7. System manager configuration

Table 1. Specifications of the PC and the peripherals

System	
CPU	μPD 780C-1 (NEC) (Z-80A Compatible)
Clock	4 MHz
Operating Systems	N88-BASIC, CP/M
Memory	
System ROM	40K
User RAM	64K
Graphic VRAM	48K
Bank switching	32K units
Display	
Type	High resolution monochrome
Character display	80 X 25 chs
Graphic display	640 X 400 pixels
Printer	
Type	Centronix standard parallel
No. of Columns	80
Buffer capacity	64K
Disk drives	
No. of Units	2
Total capacity	327K X 2
Interface	
RS-232C	
Expansion slots	3
Calendar clock	
Backed by NICAD battery	