Feedback and clarifications on ICAL TDC device specifications

Point 4 stating no of bits need not be specified by the user. That should be decided by the designer as per his scheme. Remaining looks very safe specifications.

Upadhya

Answer: You may be right. I just tried to be a little more explicit.

Rate at which you expect to use the SPI interface? I think it will be quite low, but you have to think of all the strips and check what rate data will get dumped onto the main communication. Rest looks good.

Anil

*Answer: As per the specs that I wrote down, maximum TDC data size/event is 128 words = 16 channels * 8 hits (for multi-hit TDC). If we clock out data on SPI at 10MHz, the data transfer time is about 250µS for this worst case scenario (in terms of data size, 18-bit TDC words assumed). In the overall picture, this speed may not be enough. I understand that in principle we can run SPI at any speed – there no standard speed! In this case, we must aim for the "maximum achievable" speed at the TDC side. We of course will have to work later, on these specifications at the controller level.*

Given the above, can you comment on the maximum speed that we will/should fix for the TDC chip?

I looked into the specifications and it seems ok with me. Maybe other experts can suggest something different. Your note is quite clear. As an R&D project for the XII plan this should be ok.

Sudeb

Thanks, Finally It is there. The 128 bit memory is for each channel or total? I feel its total. Things seems to reasonable, but power budget is not there good. Kindly process the 0.18um & farady papers so that thing keep moving on TDC. We will try to meet the specs even if they are desirable hope so!

VBC

*Answer: 128 words = 16 channels * 8 hits (for multi-hit TDC). I intentionally did not mention the power budget. I do not have an estimate; mentioning a number based on literature might not make sense. I am sure you will strive to keep this to a minimum.*

---

1. Number of channels 8 or 16
Fine. 16+1 LVDS channels will make 34 input pins

Answer: So you are taking LVDS option.

2. Least count 200ps
OK. Does it matter if it is less, as long as the dynamic range is covered?

Answer: No problem, welcome, though the number of data bits will increase in this case.

3. Dynamic range 2µs (essential), 32µs (desirable)
OK. Trivial to increase.

Answer: Good.

4. Number of bits 14 (essential), 18 (desirable)
OK.

5. Type Common stop
OK.

6. Hits Single hit (essential), multi hit (desirable)
What is the minimum duration between hits if it is a multi hit one? 5ns? How long after the common stop signal must you start counting again? In addition to storing the final results, many buffers will be needed.

Answer: Double pulse resolution could be 5-10ns; I will add this as a spec. In principle, you can restart counting soon after transferring data into the buffer. Trigger system will not allow next trigger until data from the previous trigger is transferred to the backend. In this case, why will you need more buffers?

7. Readout buffer size 128 words (maximum)
OK.

8. Signal and control inputs LVDS or LVTTL
LVDS is OK for high speed inputs. By control do you mean the SPI signals as well? This is wasteful of pins and power. CMOS levels should be OK.

Answer: OK, I agree now.

9. DNL/INL 100ps (typical)
OK.

10. Power rail 3.0 to 3.6V (suggested)
OK. Does it matter if it is less (1.2V or 1.8V) and a regulator is placed outside?

Answer: Should be fine.

11. Control and readout interface SPI (essential), SPI + parallel (desirable)
Parallel seems wasteful of pins. With 16+1 LVDS channels, and 18 parallel output bits, a number of controls and a number of VDD/ground pins (essential for the high speed side), you are looking at up to 80 pins. This is easily doable, but the package will be larger than if you limited yourself to say 48pins. Better for high speed circuitry. Is there any particular need for parallel outputs?

Answer: Not particularly. I thought if the chip supports parallel bus as well, then it can find other applications. Of course, SPI being so simple interface, one could easily build the same on any board for control and receiving the data from the chip.

==========

Questions:

a) What is the system clock available for time reference? We have assumed 50MHz in our design.

Answer: Do we need to run this clock globally? 50MHz seems to a slow clock enough to transmit without serious problems. I am currently reading IEEE-1588 standard meant for clock synchronisation.

b) Is there a particular variant of SPI that you intend to use? I think there are simple and complex ones. We already have a module for the one used in AIC111 IC (datasheet attached). What is the serial data rate you prefer to have?

Answer: I answered this above.

c) How will the reset work? When should the next set of measurement start after the common stop signal? If it has to be before the TDC output is read out, one or more sets of buffers is required to avoid deleting the old data.

Answer: I answered this above.

16 channel TDC + LVDS input buffers + data storage will take quite a bit of area. We are planning on a single TDC, front end, analog memory tape-out now. If a multi channel TDC does become ready (by say, a miracle), is there a way to pay for its tape-out? I estimate ~ 14,000/- Euro.

Answer: This can possibly be answered by Prof. Mondal.

Nagendra

For the specifications which are marked 'desirable', it is needed to state (or to study and state) what will happen if it is NOT implemented.

In particular for the TDC to be multi-hit type, it is needed to study in more detail how much do we suffer if this is not available, for both normal (muon-type) and hadron events.

Answer: Soon after the ICAL electronics meeting held at SINP, I initiated this study. The values of 2µs and 32µs for the pre-trigger window in a multi-hit type TDC were arrived based on this study.

In most of the present day HEP experiments, wherever timing is used, it has become a regular practice to use multi-hit TDCs to get more accurate time information. While some of the reason may have to do with their being connected with accelerator timing also, for our case timing (rather, "precise timing") becomes important to distinguish various types of neutrino events and hence enhances the capability of ICAL manifold.

This needs more critical evaluation and probably may take some time as one has to go through simulation studies.

Viyogi

S. No.	Parameter	Suggested specs	TDC_1	Comments
1	No. of channels	8 or 16	8	As the location is not fixed, 8 looks to be better option *Answer: Location will possibly be fixed very soon.*
2	Least count	200ps	200ps	Jitter and skew in trigger arrival time at individual RPC_DAQ has to be better than this? How much? *Answer: We will arrive on it as part of trigger system specs soon.*
3	Dynamic range	2us(essential), 32(desirable)	2us	
4	No. of bits	14(essential), 18(desirable)	14	
5	Type	Common stop	Common stop	Only option possible? *Answer: Yes, in my opinion*
6	Hits	Single hit (essential), Multi hit (desirable)		Is the discriminator able to drive un-stretched output over cable to RPC_DAQ? *Answer: May be VBC can answer this question.*
7	Readout buffer size	128 words (maximum)	128 words	
8	Signal and control inputs	LVDS or LVTTL		Signal (and stop) can be LVDS. Other control signals which are driven on-board can be LVTTL to save pins and to save level translators. *Answer: Please see above.*
9	DNL/INL	100ps (typical)	100ps	
10	Power rail	3 to 3.6 V		3.3V appears to be a natural choice
11	Control and readout interface	SPI(essential), SPI+parallel(desirable)		Parallel interface will need many pins. I think SPI should be adequate *Answer: Please see above.*

Suggestion: instead of specifying parameters as essential and desirable, can we specify two sets of parameters targeted for two types of TDCs? for ex: (8 ch, 2us, single hit, 14bit) and (8 ch, 32us, multi hit , 18bits)

Anita