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For and on behalf of ICAL detector, electronics and DAQ teams

STATUS SUMMARY ON ICAL DETECTOR, ELECTRONICS AND DAQ SYSTEMS

Setting up of RPC labs

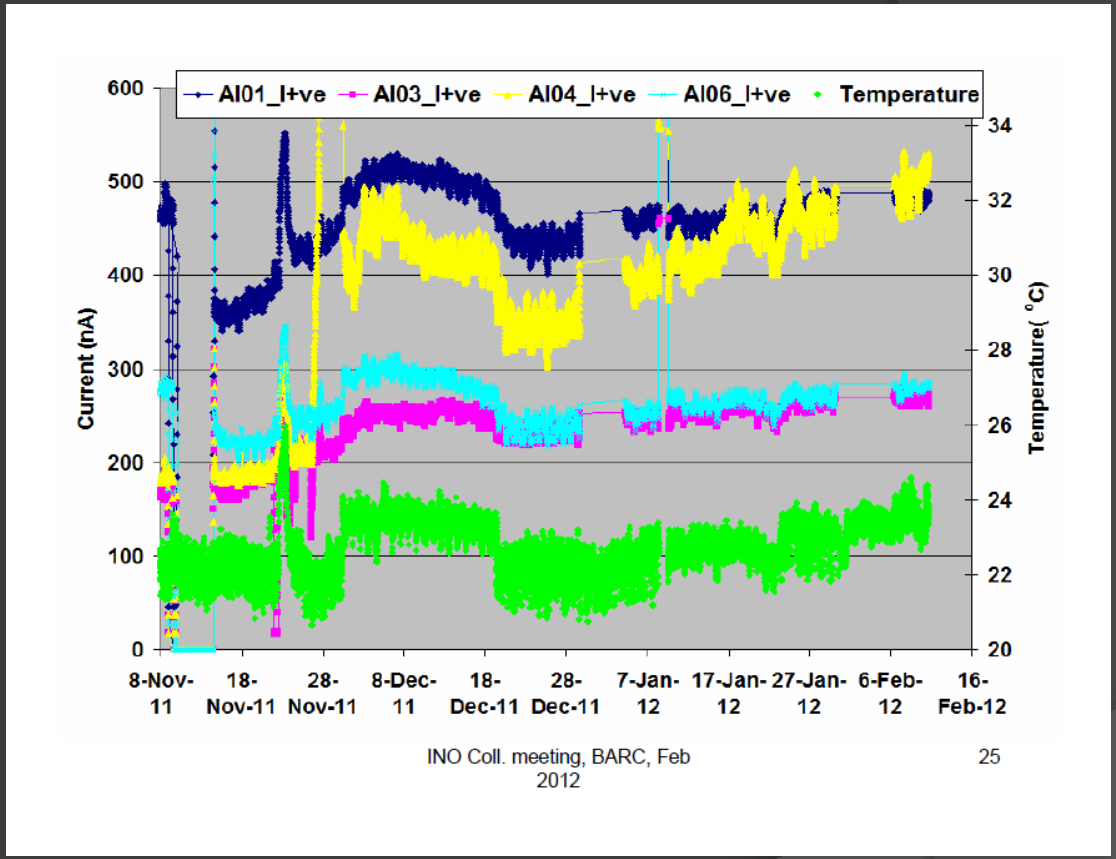
- RPC labs were setup or being setting up at:
  - BARC (Varchaswi), PU (Bhandari), IITM (Raveendra), DU (Sunil), AMU, BHU etc. apart from TIFR, VECC and SINP
- Shouldn't there be uniformity among them in terms of the electronics and DAQ software etc?
  - May be yes; easier to support
  - Is already the case gas systems, DAQ hardware, paddles etc.
- Getting equipped/trained for QC of RPC production
- Common requirements:
  - Spacers/nozzles, paint, pickup panels, front-end electronics
  - MOQs high, pooling of requirements is a solution
  - Good case for ECIL's role in case of electronics

What is the QC scheme for the RPCs?

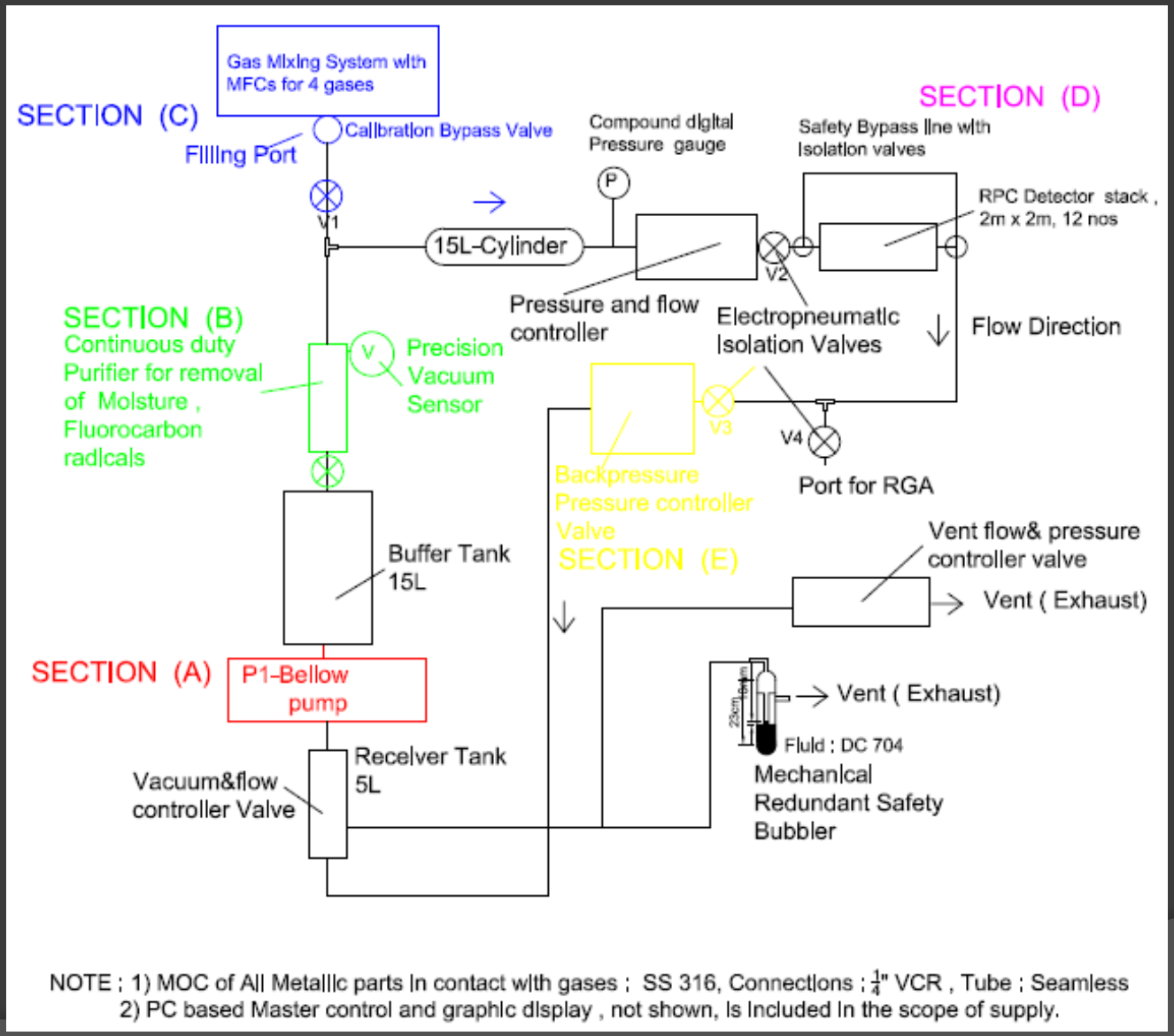
- No serious thinking on this yet on:
  - the parameters to be tested, procedures to be followed etc.
  - Long-term tests on a sample of production
- Multiple stations, high throughput needed
  - For example: 10000 RPCs, 200 days/year, 2 years, 3 stations → ~10 day/station
- Cosmic tests even with RPC stack might be too slow
- Radioactive scanners is a solution
- Opportunity to contribute, design and production of multiple units

Gas optimisation studies

- Gas flow for five RPCs (2m×2m) in new lab is reduced to 0.29 SCCM (1 volume change per 19 days).
- Long-term performance studies on these RPCs is in progress.
- At present, gas flow for the RPC (1mx1m) stack in C217 lab is 2.25 SCCM (1.6 volume change per day) i.e. 1 volume change per 0.62 days.



Closed loop gas system



- Performance of close loop recirculation depends on:
  - Maintaining pressure balance
  - flow rate
  - efficiency of purification process
  - leak integrity of RPC

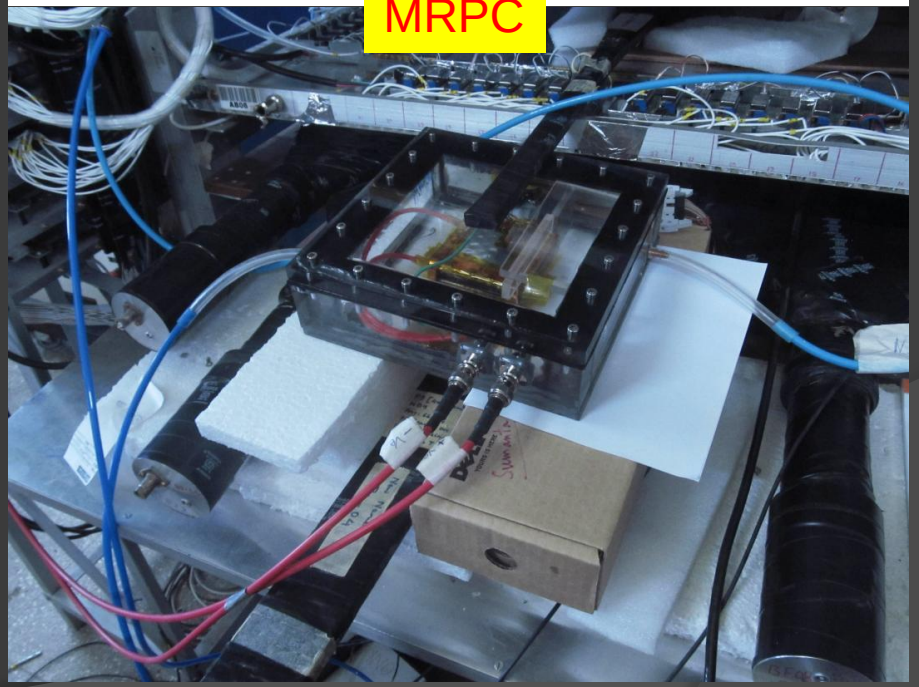
Industry, academia interface

- Glass, RPC production: Asahi India Glass, Asahi Architectural and Auto Industry
- Graphite coating: Grafica Flextronica
- Gas Systems: Alpha Pneumatics
- RPC fabrication, automation tools: Global Engineering Technologies Packaging
- Development and detailed engineering design report on industrial production of RPC, vendor development: Walchand Industries
- Gas distribution system and flow dynamics of RPC, Gas Purification System in RPC system for INO: ICT
- Tata Consultancy Engineers
- ICAL building: Plazma Industries
- RPC production, electronics design and fabrication, power supplies: ECIL

R&D and studies with RPC

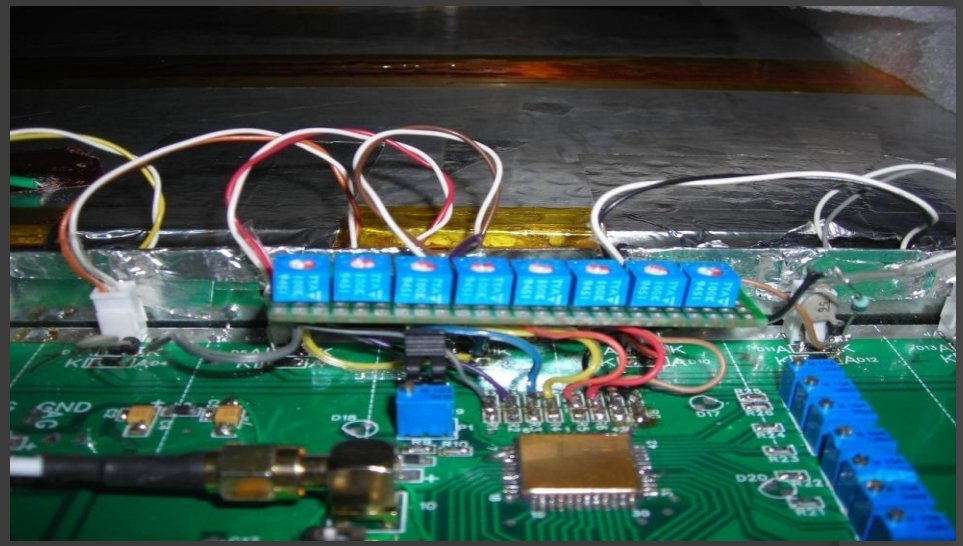
- Development of 6-gap MRPC: Moon Moon Devi
- Study of angular distribution of cosmic ray muons, directionality and measurement of integrated flux: Sumanta Pal
- Simulation studies on the Effect of SF_6 in the RPC gas mixture: Salim Mohammed
- Bakelite surface tomography studies: Nayana Majumdar
- Background radiation studies using demo RPC: R.R.Shinde

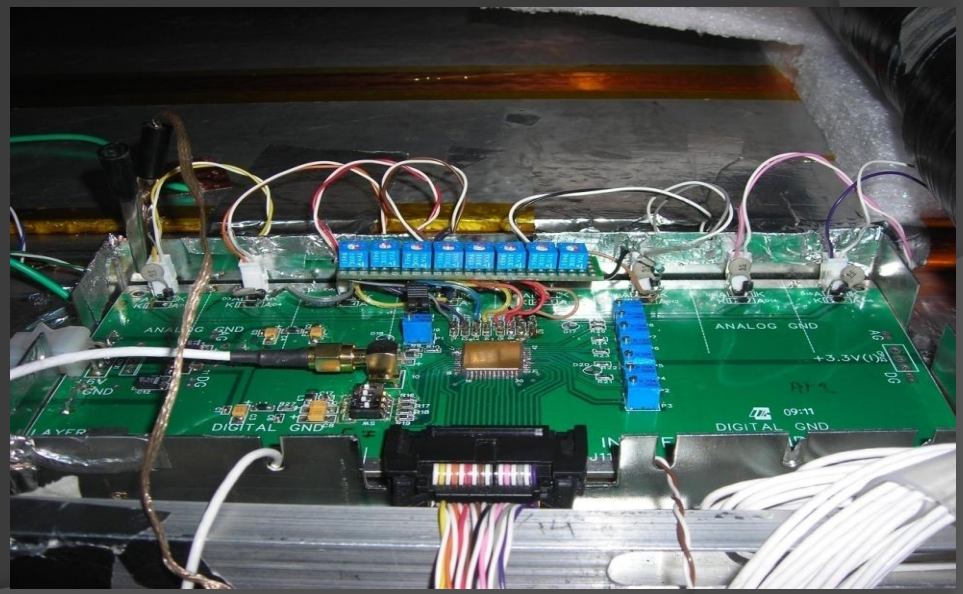
MRPC

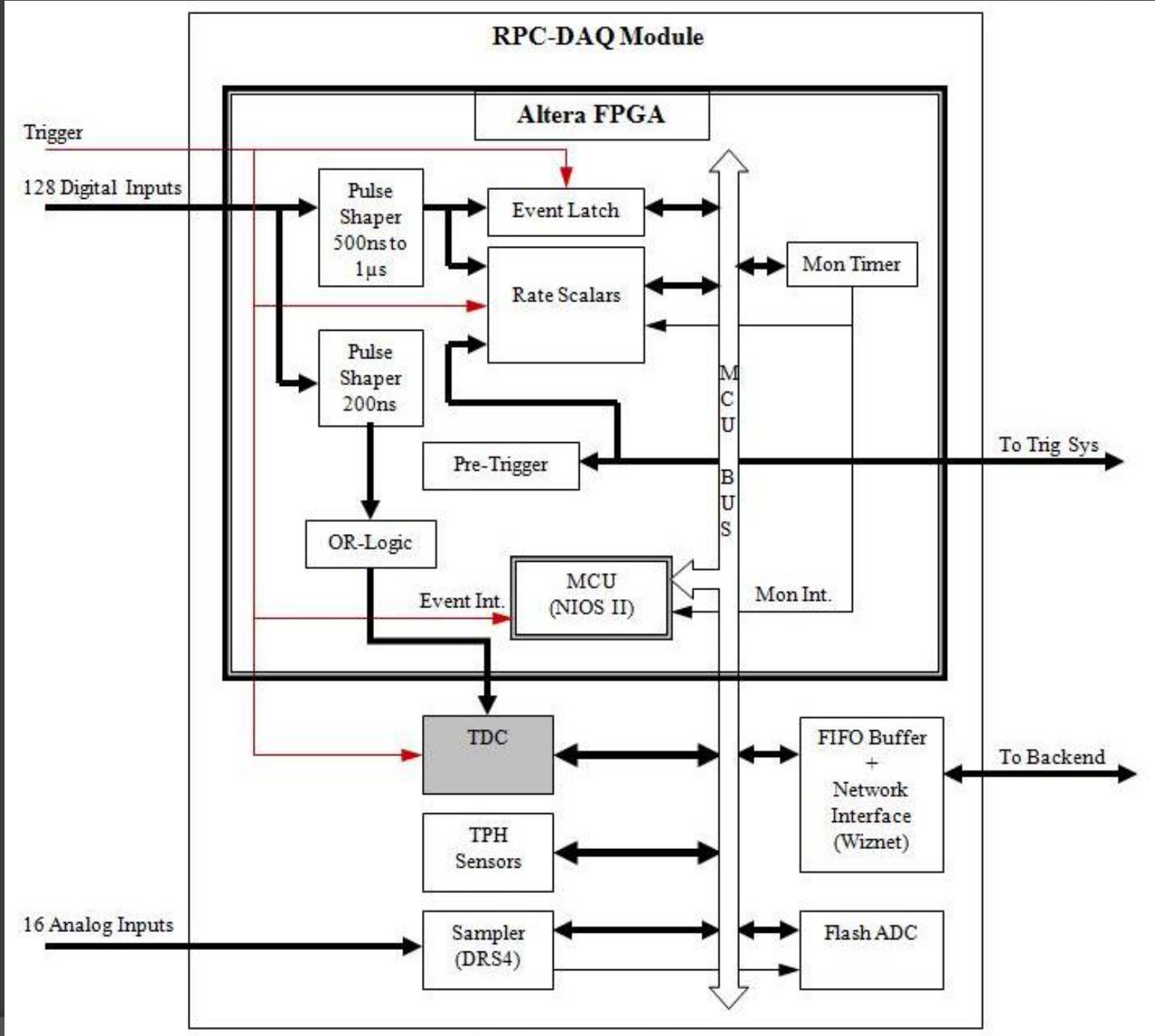


Testing of FE ASIC on RPCs

- Minimum threshold values possible with AP2 and AP1 boards is at V_{38}=1.650V. So the effective threshold is ~250mV.
- Obtained stable noise rates with both boards.
- Noise rates with HMC based preamplifier is double to those obtained with AP2.
- Efficiency with AP2 board is about half compared to what was obtained with HMC based board.
- Operating gain 4mV/μA as against the design value 8mV/μA due to instability problem while the multiplexer is turned on
- Design revisions by the CMEMS group
  - Gearing for a second iteration production
  - Separate chips for positive and negative inputs as well as amplifier and discriminator might anyway solve this problem





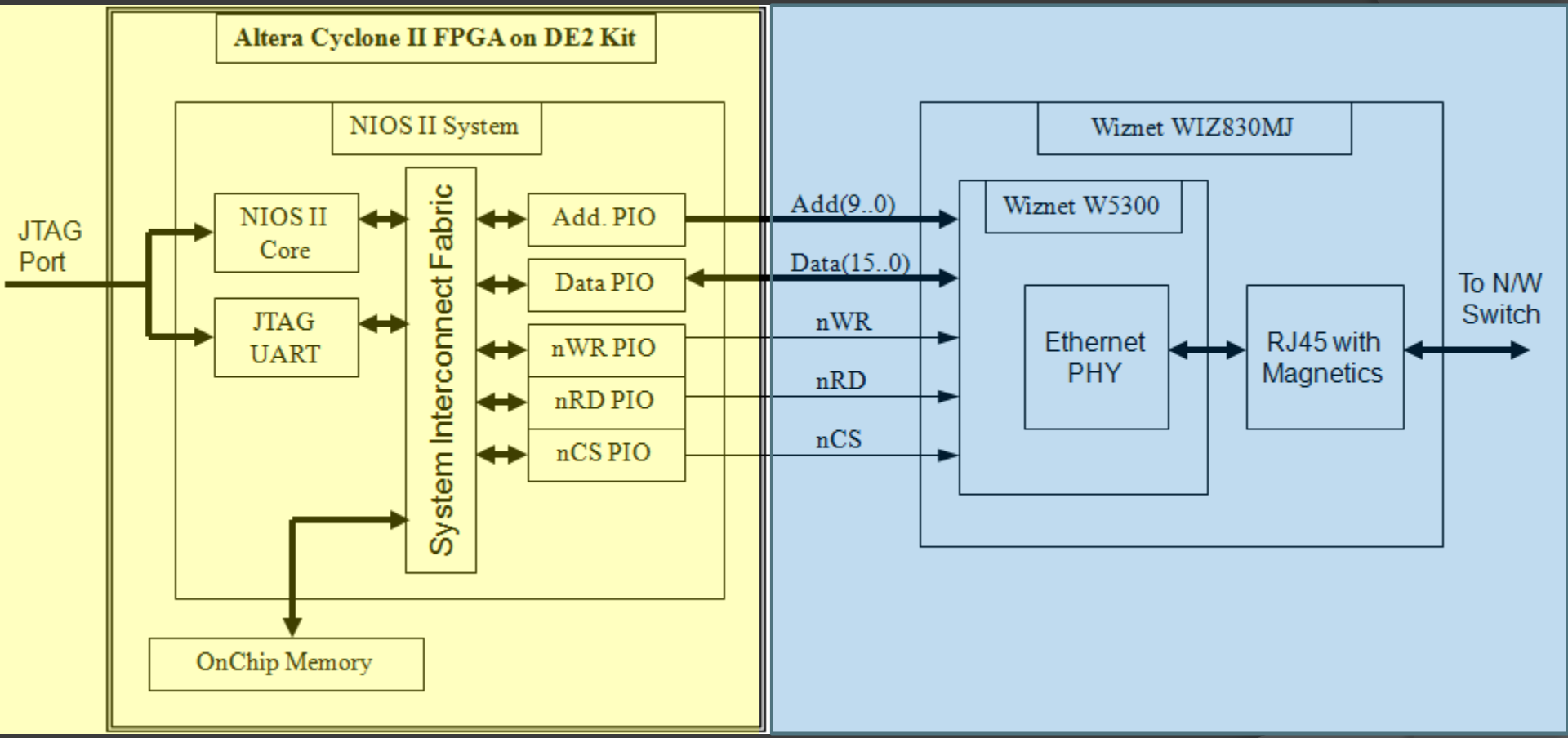


RPC DAq Block Schematic

Networked DAQ scheme

- Alternate to the “conventional” VME backend scheme
- The idea:
  - RPC module gets the capability to “acquire” and store its own data. Call this “Level 0” data
  - One “data concentrator server”, (one per N number of RPC's) collects RPC data, by either push or pull method, on master trigger. Call this “Level 1” data
  - One higher “Level 2” machine reads all “level 1” data
- Benefits:
  - Simple, standard, cheaper, hierarchical scheme
  - Software development is easier
  - Simpler data cabling (because terminated on local hubs)
  - Interrupt driven data acquisition (level 0), client-server based DAQ (level 1), monitoring and slow control are all handled this way
  - Complete testing of RPC with a laptop and a HV/LV supply

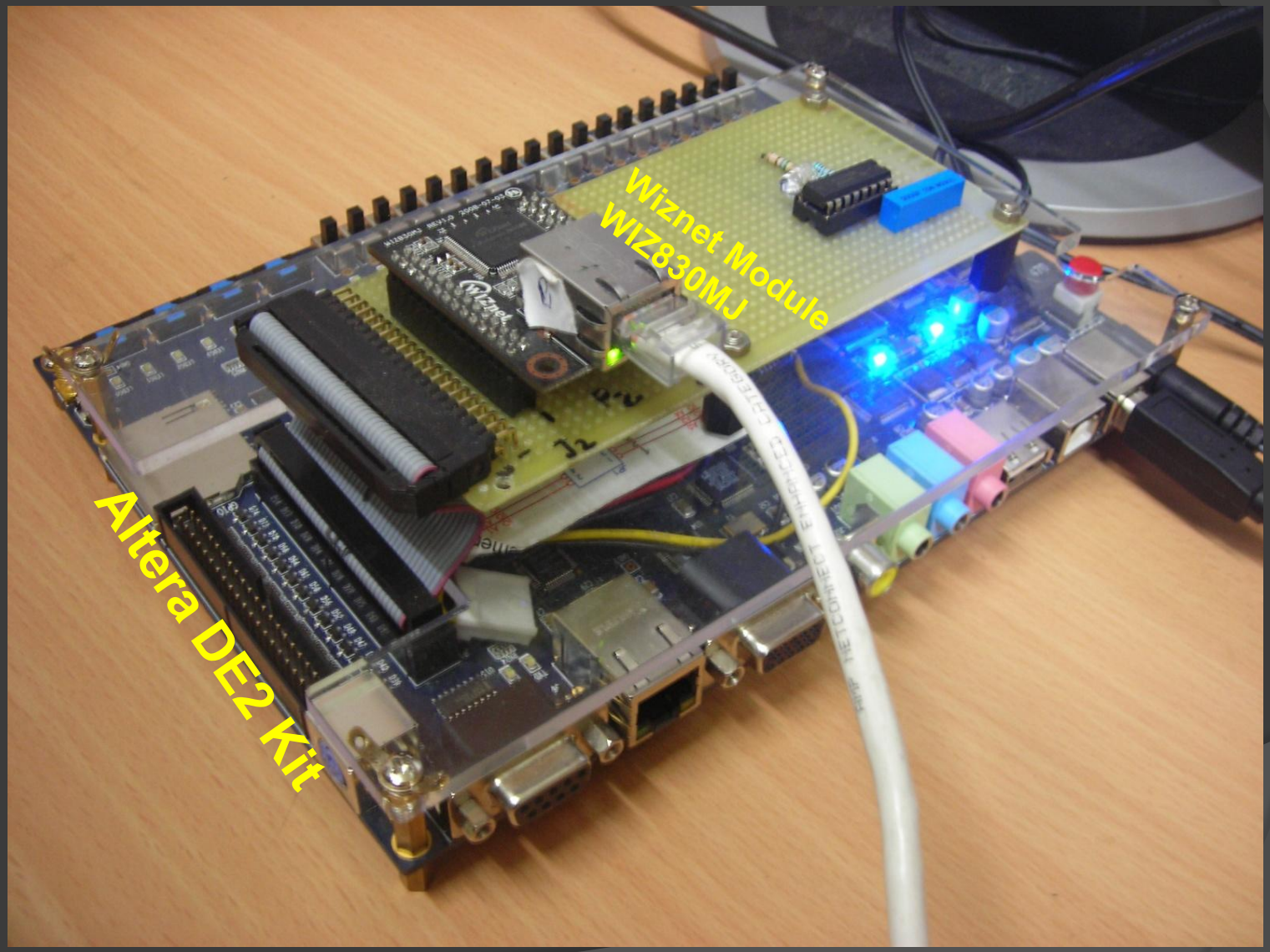
Wiznet to FPGA Interface



Current work on data interface

- Altera DE2 kit with Cyclone II EP2C35 FPGA
- FPGA configured with NIOS II system using SOPC Builder a part of Altera Quartus
- Wiznet W5300 interfaced to NIOS II in port mapped I/O mode
- Software developed in NIOS II EDS IDE in C
- Established two way communication between PC and Wiznet test setup.

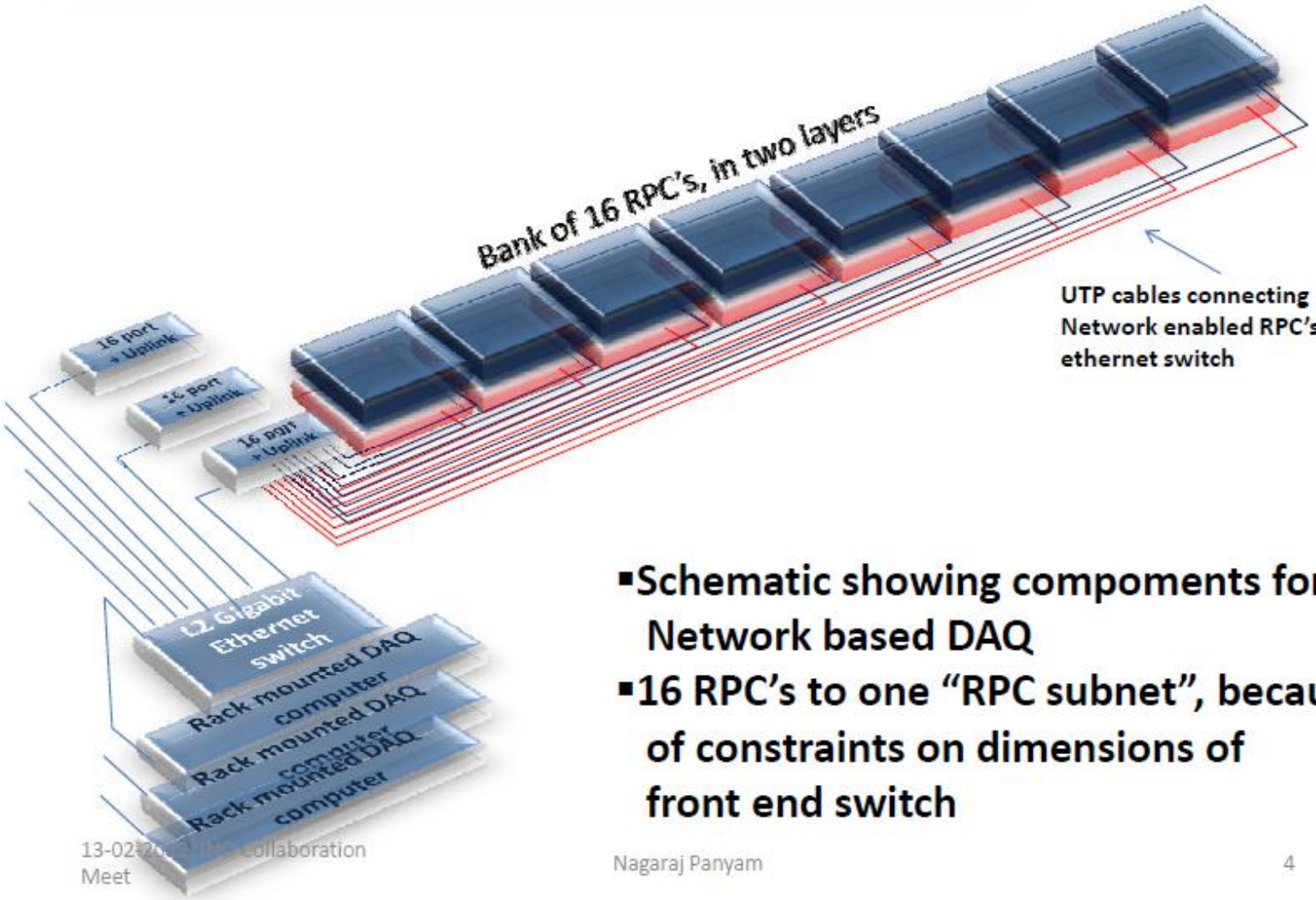
Wiznet to FPGA Interface



ARM9 Development kit

- Likely candidate for CPU to go on RPC: ARM9
- One development kit ARM9 (Samsung make),
  - 64MB memory,
  - 1GB storage (NAND Flash),
  - 34 GPIO pins
  - User input pins, interrupts
  - Serial console
  - 100BaseT Network Interface
- Runs Linux 2.6

Alternative, Network based DAQ for INO ICAL

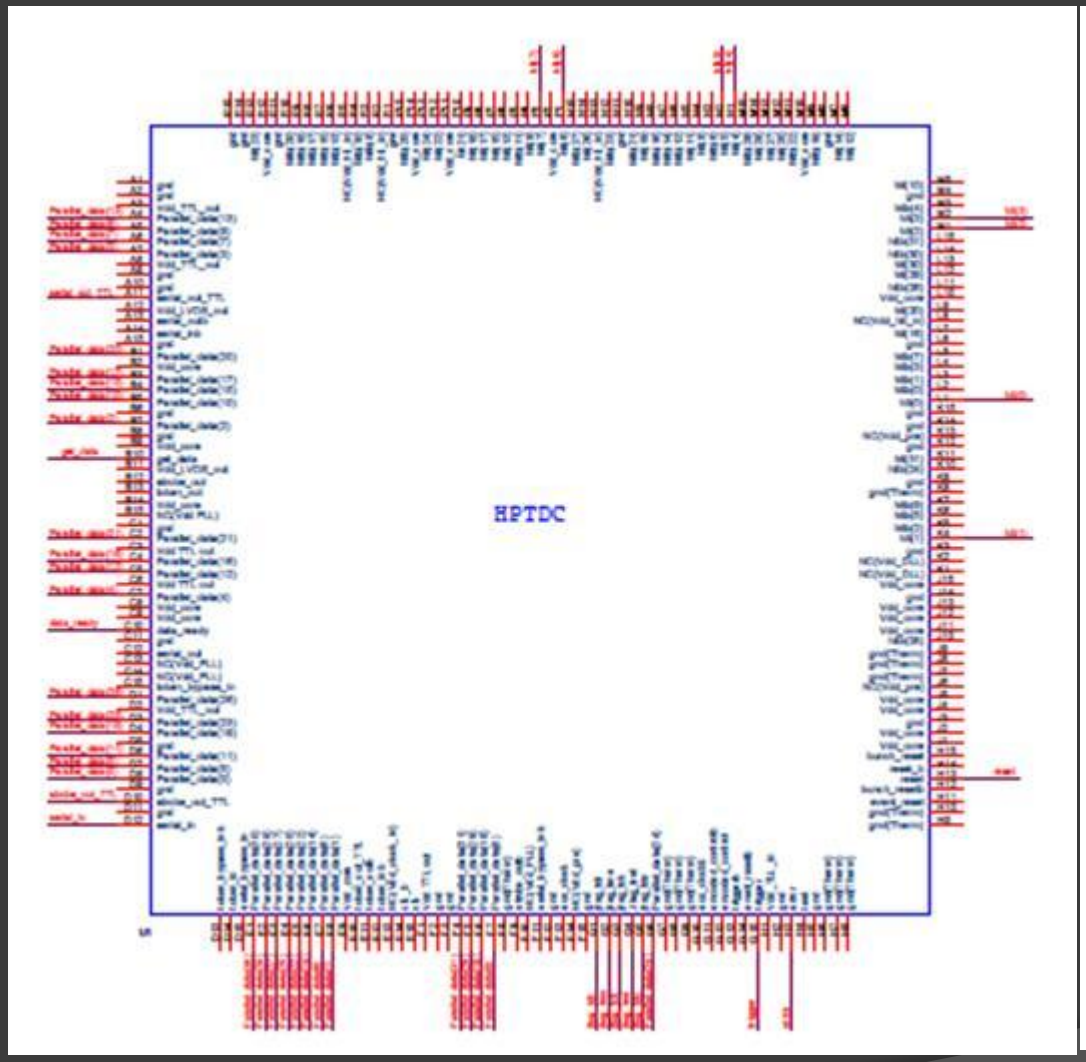


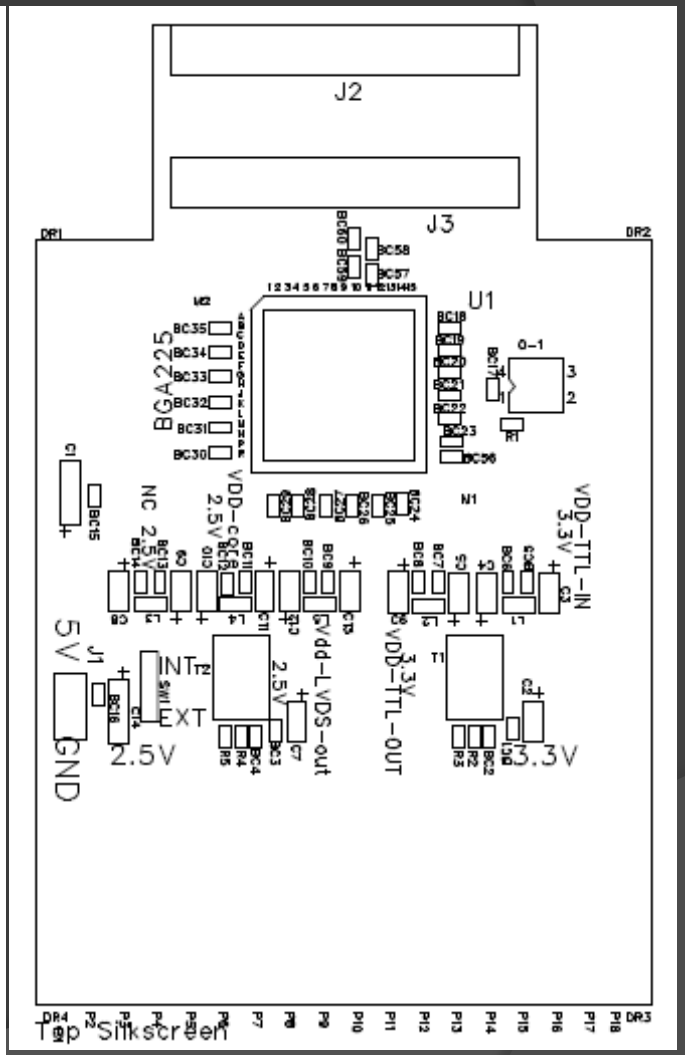
- Schematic showing compoments for Network based DAQ
- 16 RPC's to one "RPC subnet", because of constraints on dimensions of front end switch

Specifications of the ICAL timing device

Parameter	Specification
1. Number of channels	8 or 16
2. Least count	200ps
3. Dynamic range	2μs (essential), 32μs (desirable)
4. Number of bits	14 (essential), 18 (desirable)
5. Type	Common stop
6. Hits	Single hit (essential), multi hit (desirable)
7. Double hit resolution	5-10ns
8. Readout buffer size	128 words (maximum)
9. Signal and control inputs	LVDS and LVTTL respectively
10. DNL/INL	100ps (typical)
11. Power rail	3.0 to 3.6V (suggested)
12. Control and readout interface	SPI (essential), SPI + parallel (desirable)

Place-holder for TDC on RPC-DAQ prototype





Integrated Circuits for the INO (Nagendra)

- Time to digital converter(TDC)
  - Taped out: Jan 16th
  - Expected: mid-May
- Front end amplifier
  - DC gain of 41.5 dB
  - Bandwidth of 513 MHz
  - Power 0.2 mW power.
  - Technology UMC 0.13 μm CMOS process.
  - Schematic design complete
  - To do: Layout, post-layout simulations
- Analog memory+backend ADC
  - Preliminary schematic design done
  - To do: Complete design and integrate with the ADC
- Technology used: UMC 0.13μm CMOS

IITM TDC specifications (Nagendra)

- The design is implemented in 0.13 μm CMOS process.
- The TDC has a resolution of 125 ps
- Dynamic range of 131 μs.
- It occupies 0.24 mm^2 area and consumes negligible static power.
- The DLL occupies 0.12 mm^2 area and consumes a power of 2 mW.

Role of waveform sampler for ICAL

- Walk correction of TDC data
- Leading edge discriminator
- Time over threshold information
- Pulse profile, height and width monitoring
- Remote display of RPC signals

Consolidation of its function

- Better understood DRS4 – thanks to the *demo RPC* project!
- Not sure though, if we understood the exact role and hence its exact operation scheme ICAL electronics
- Do we use in both event and monitoring modes?
- The above required different front-ends for the analog front-ends
  - Multiplexed analog signal
    - Easier to implement?
    - Timing problem in event mode
  - Summed/ORed analog signal
    - Relatively difficult to implement?
    - No timing issue, hit channel id could be inferred
- Where is the chip?

Event data rates

- Event Data per Trigger is as follows: (64 strips on each plane of RPC)
- TDC data = 1 channel for 8 strips and both the edges per hit, up to 4 hits per channel per event = 16 channels x 2 edges x 4 hits x 16 bits = 2048 bits
- Hit data per RPC = 128 bits
- RPC ID = 32 bits
- Event ID = 32 bits
- Time Stamp = 64 bits
- DRS data = 16 channels x 1000 samples x 16 bits = 256000 bits
- (DRS data comes in event data only if we get summed analog outputs from the preamplifier)
- Data size per event per RPC
- With DRS data, D_R = 2048 + 128 + 32 + 32 + 64 + 256000 = 258,304 bits
- Without DRS data, D_R = 2048 + 128 + 32 + 32 + 64 = 2,304 bits
- **Considering 1Hz trigger rate, Maximum Data Rate at each RPC = 252.25 kbps**

- Total data size per event across 3 modules
- With DRS data, D_T = 258304 x 28800 = 7,439,155,200 bits i.e. 6.928 Gbits
- Without DRS data, D_T = 2304 x 28800 = 66,355,200 bits i.e. 63.28125 Mbits
- Considering 1Hz trigger rate, Maximum Data Rate at backend = **6.928 Gbps**

Monitor data rates

- Monitor Data per 10 seconds
- We require to monitor 1 pick-up strip per plane per RPC.
- Monitor Data per strip = 24 bits
- Channel ID = 8 bits
- RPC ID = 32 bits
- Mon Event ID = 32 bits
- Ambient Sensors' data = 3 x 16 bits = 48 bits
- Time Stamp = 64 bits
- DRS data = 1000 pulses (if noise rate is 100Hz) x 16 bits x 100 samples = 1600000 bits
- (DRS data comes in monitoring data only if we get multiplexed analog outputs from the preamplifier)

- Data size per 10 seconds RPC
- With DRS data = 24 + 8 + 32 + 32 + 48 + 64 + 2048 + 1600000 = 1,602,256 bits
- Without DRS data = 24 + 8 + 32 + 32 + 48 + 64 + 2048 = 2,256 bits
- **Max Data Rate for 10 second monitoring period per RPC = 156.47 kbps**

Trigger scheme for ICAL

- Validation of the trigger schemes; document in good shape
- Ready to go for implementation
- Integration issues
  - Segment trigger module positions
  - Pre-trigger signal driving issues
- Specifications:
  - Coincidence window: 100ns
  - Maximum trigger latency: 1us
  - Singles rate for RPC detector pickup strips: 250 Hz
  - The skew and jitter in arrival instant of the global trigger at different RPCs should be as low possible
- BARC team (Anita Behere *et al*) joined the trigger team for implementation
- Document on the implementation scheme is not yet place

Trigger implementation

- Trigger scheme developed and validated
- Layout of trigger scheme implementation
- Study of LVDS transmission
- Conceptual design of the trigger modules
- FPGA logic development
- Validation of design concept in FTM

Software components

- RPC-DAQ controller firmware
- Backend online DAQ system
- Local and remote shift consoles
- Data packing and archival
- Event and monitor display panels
- Event data quality monitors
- Slow control and monitor consoles
- Database standards
- Plotting and analysis software standards
- OS and development platforms

Software

- BARC team (Diwakar, Padmini *et al*) joined the software team
- Backend Data Acquisition and Monitoring System
  - Event Data Acquisition
  - Periodic Online Monitoring of RPC Parameters
  - Event Data Quality Monitoring
  - Control and Monitoring Console
  - Local and Remote Consoles
- Front-end firmware/software will be responsibility of the TIFR group
- Scope for more players (especially physicists)
- Technical document which will form part of the ICAL Electronics TDR initiated

Power Supply

- All components studied so far require only a single supply voltage
  - In fact this has to be design constraint, considering integration issues
- If the maximum voltage required by any component is 3.3V, then we can run a 5V bus around the system, and use onboard regulators to derive required voltages

Power Usage

- Power estimate for major components
  - FPGA: Roughly 1.5W
  - HPTDC: In low resolution low power mode, 40MHz clock and with TTL inputs: 0.45W
  - Wiznet W5300: Auto-negotiation of internal PHY: 0.825W
  - DRS4: @ 6GSPS: 0.35W
  - Total estimated power is less than 5W (3.125W), i.e. less than 2A @ 3.3V
- If we have a bus voltage of 5V, then regulators drop 1.7V and waste less than 4W of power
- Thus total power dissipated is less than 10W

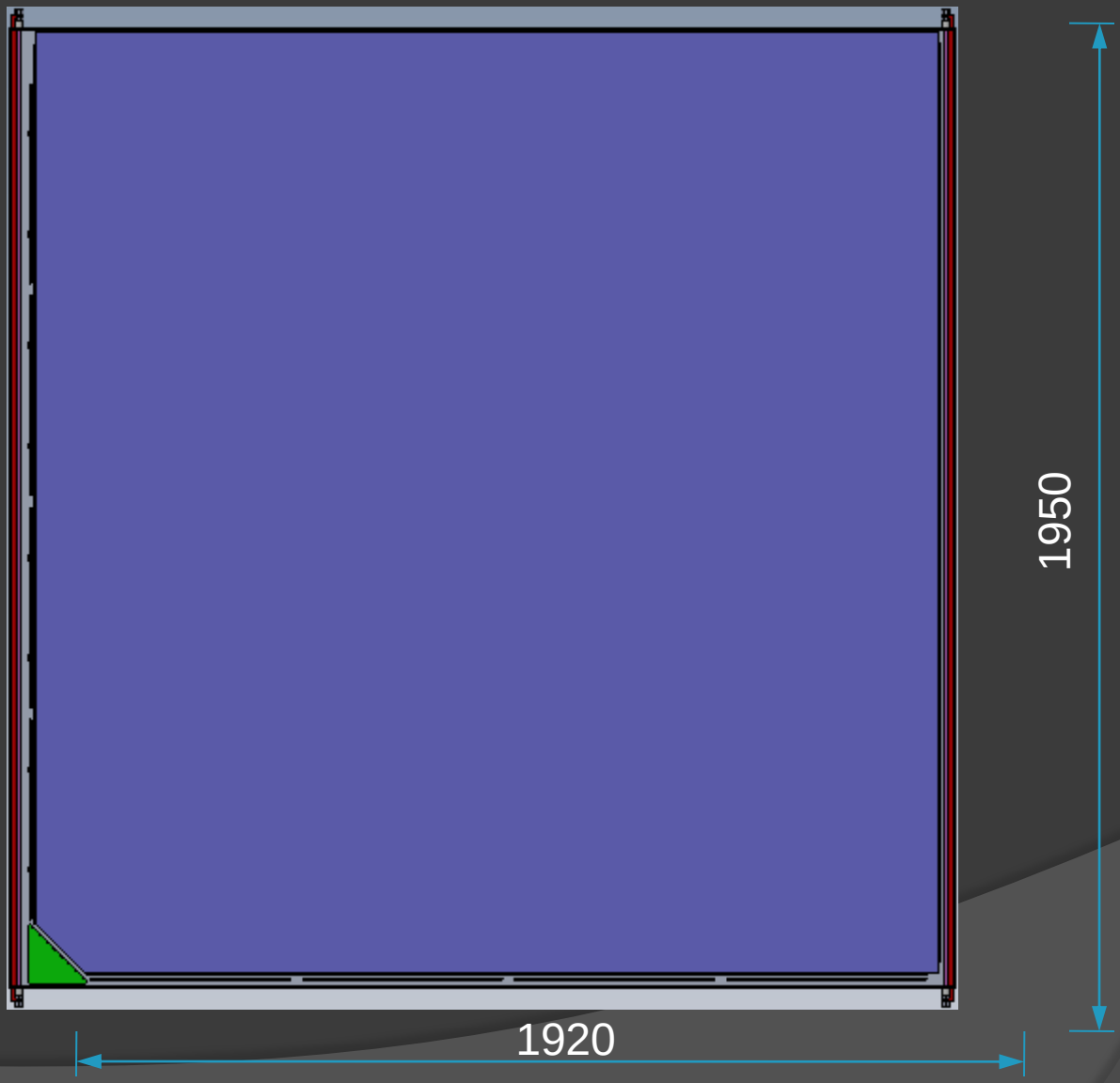
Power Usage/Dissipation

- Preamplifiers: 16W (spread across 4 mtrs)
- RPC-DAQ: 10W (from a small area)
- Total: 26W
- If supply is 6V, then current per RPC is 4.33A
- Current for 4 RPCs is 17.33A
- A 2 core power cable for 27A is 10.5mm thick

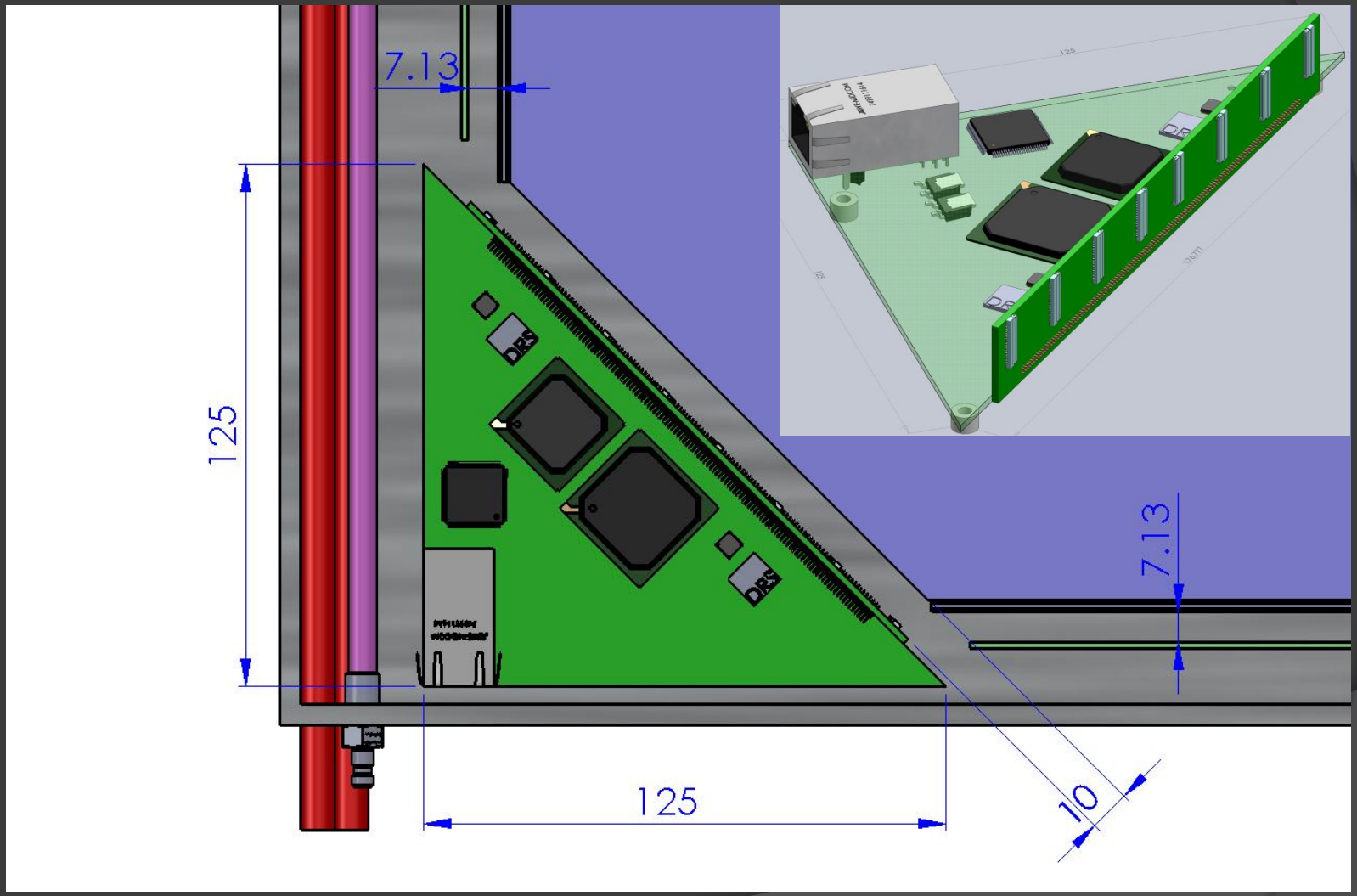
Power supply options

- High voltage (Central scheme)
  - Two options: a channel at 12kV or two channels at ±6kV
  - Consider powering 4 RPC with a single HV channel (10μA current)
  - Cable diameter an integration issues, connectors a cost issue
- High voltage (Distributed scheme)
  - DC-DCHV converters
  - Each RPC has to be identical to the others
  - Each RPC will have its own DC-HVDC converter for generating HV and LV
- Low voltage
  - Power budget 25W per RPC
  - How many low voltages?
- Space for DC-DC converters inside the RPC unit an integration issue
- Magnetic field
  - Fringe field mostly is below 100 Gauss
  - But some places between 100 and 1000 Gauss
  - Difference between 100 and 1000 Gauss is relevant for the design of the DC-HVDC

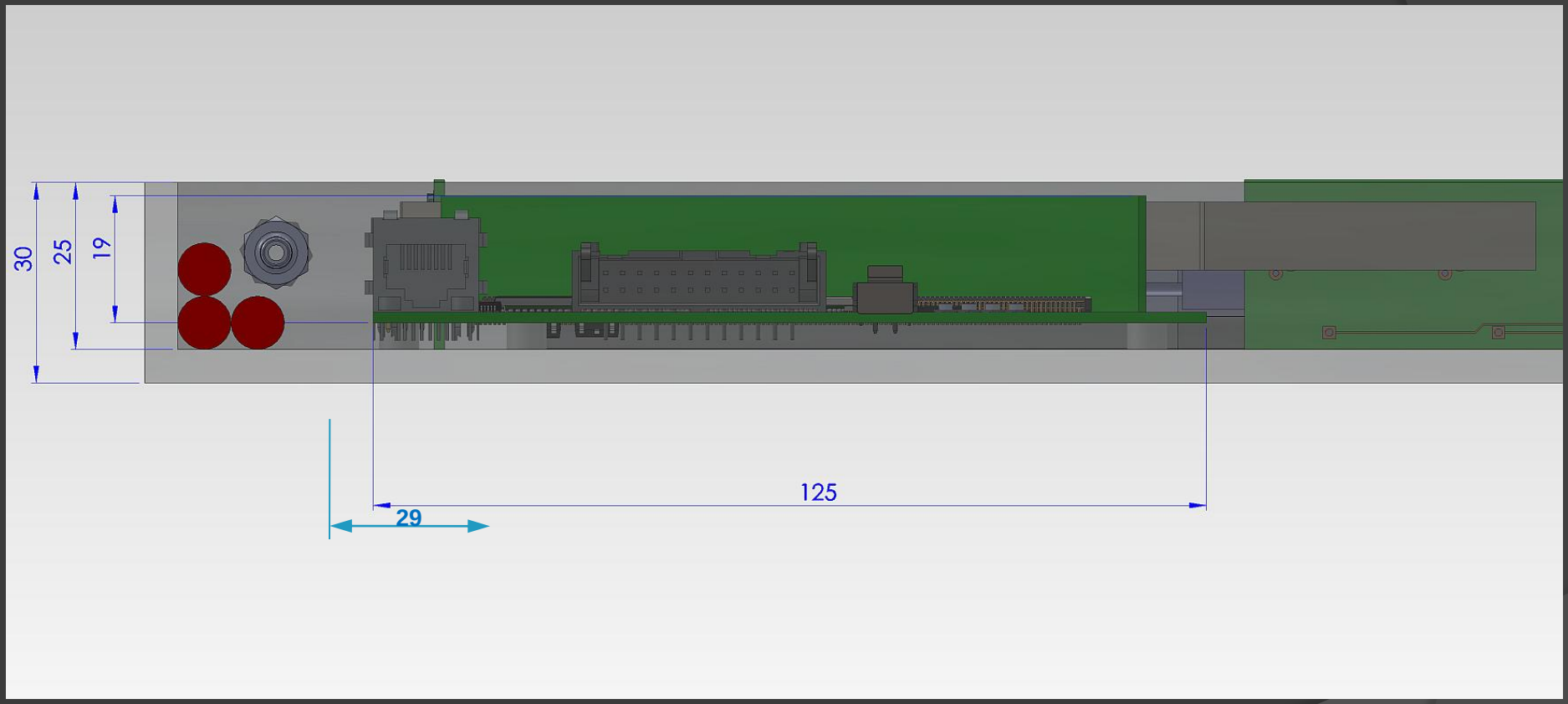
RPC Layout



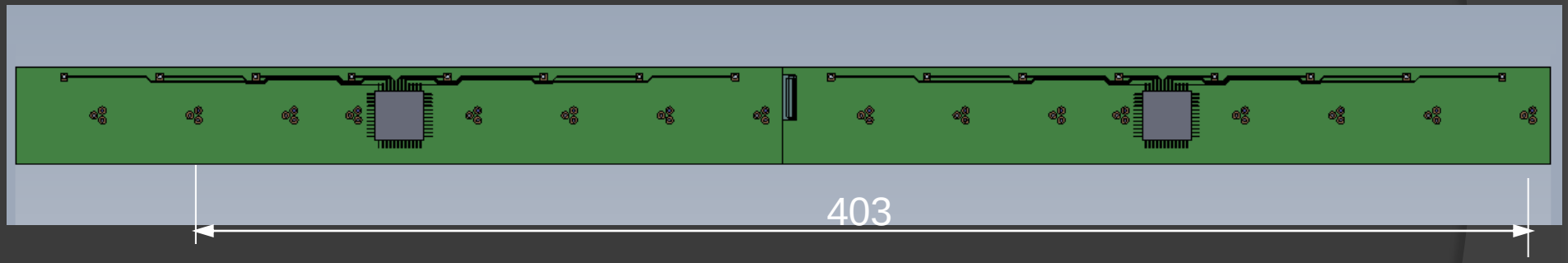
Fighting for an mm in a 132m×26m×20m cavern!



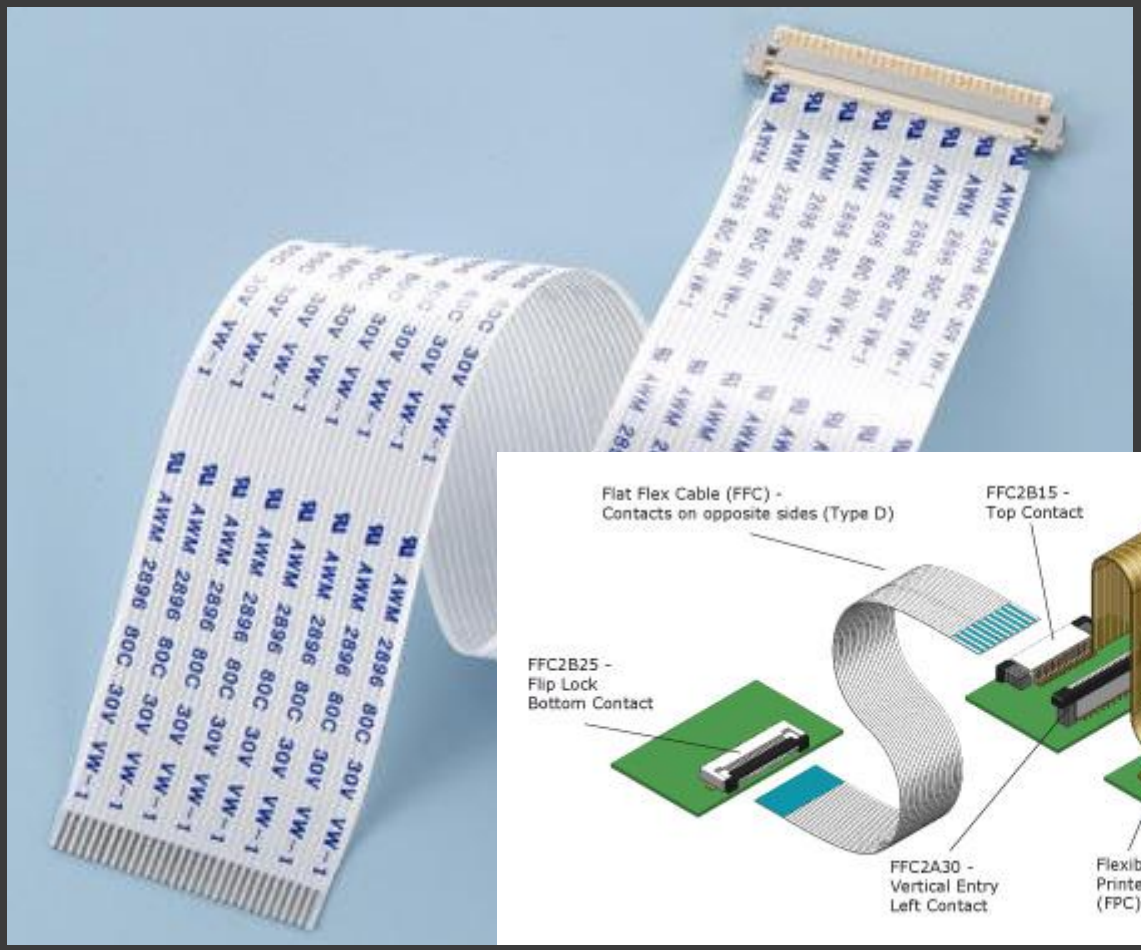
Front View

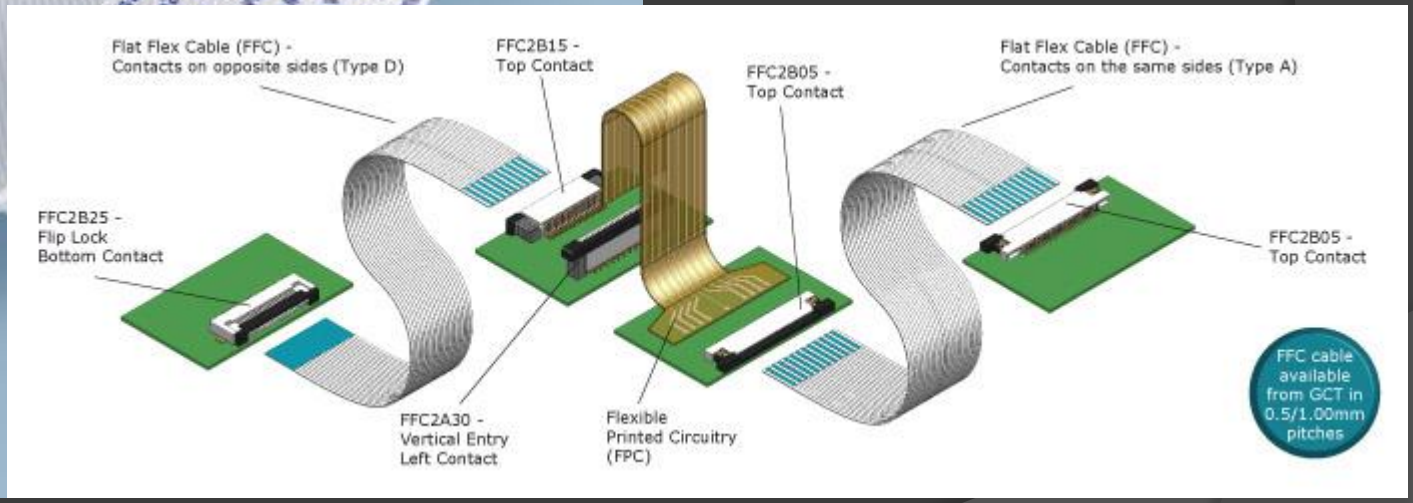


Preamplifier Board



Flat Flexible Cables





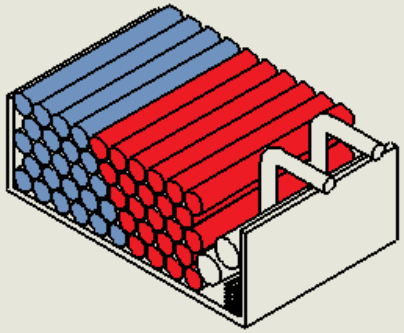
Issues continued..

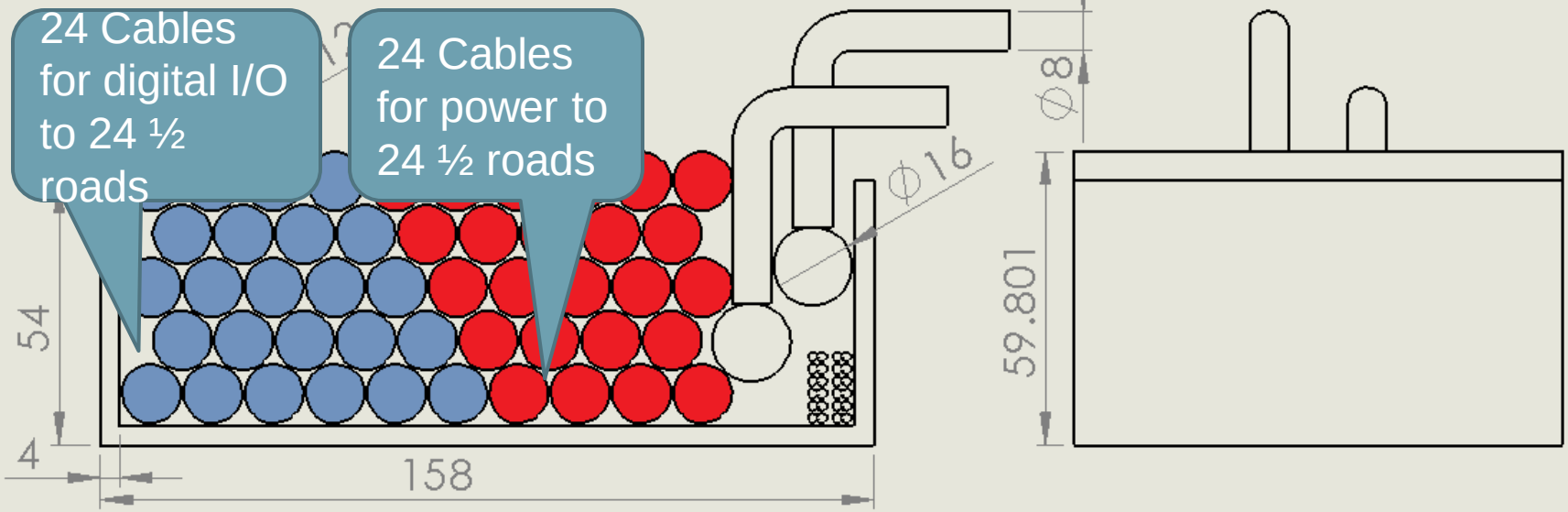
- Cable routing along the RPC
  - Following cabling from front-panel of RPC to back-panel
    - 3 Ethernet cables, i.e. 6 twisted pairs, dia. = 5.6mm
      - 2 RJ45 sockets, on front 16mm x 14mm (min size)
    - 36 pairs of digital I/O, overall dia. = 9.9mm
      - No suitable connector found
    - 2 core power cable rated for 15A, overall dia. = 8mm
    - 6 HV cables

Cables in the Cable Tray

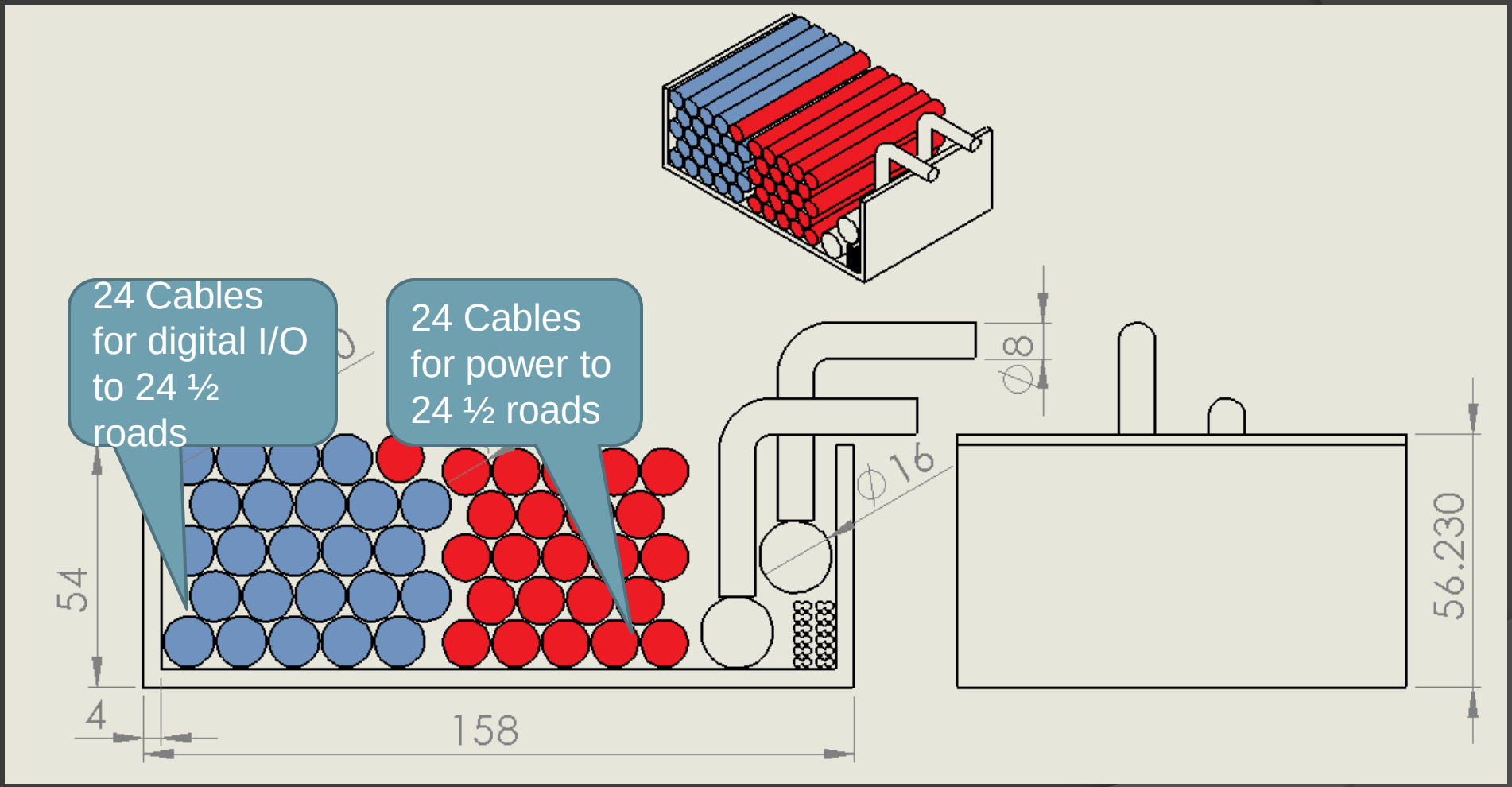
1. Power cables for the FE
   - 24 cables of 2 core wires rated at 20A, for 24 half roads
     - Finolex Flexible Cables, PVC insulation, dia = 10.5mm
2. Digital I/O from backend to FE
   - (4 pre-trigger out + 1 trigger in + 4 calibration + 2 clocks + 1 spare) x 4 RPCs = 48
   - 24 cables of 48 twisted pairs for 24 half roads
     - 3M Round, Shielded/Jacketed, Discrete Cable, 50 pairs, dia = 11.2mm
3. Network Connection from backend to FE for data
   - 12 cables of 2 core fiber optic cable, 4mm x 2mm
4. HV Connection
   1. 192 cables rated at 6kV, for dual HV supply of 96 RPCs

Populating the Cable Tray

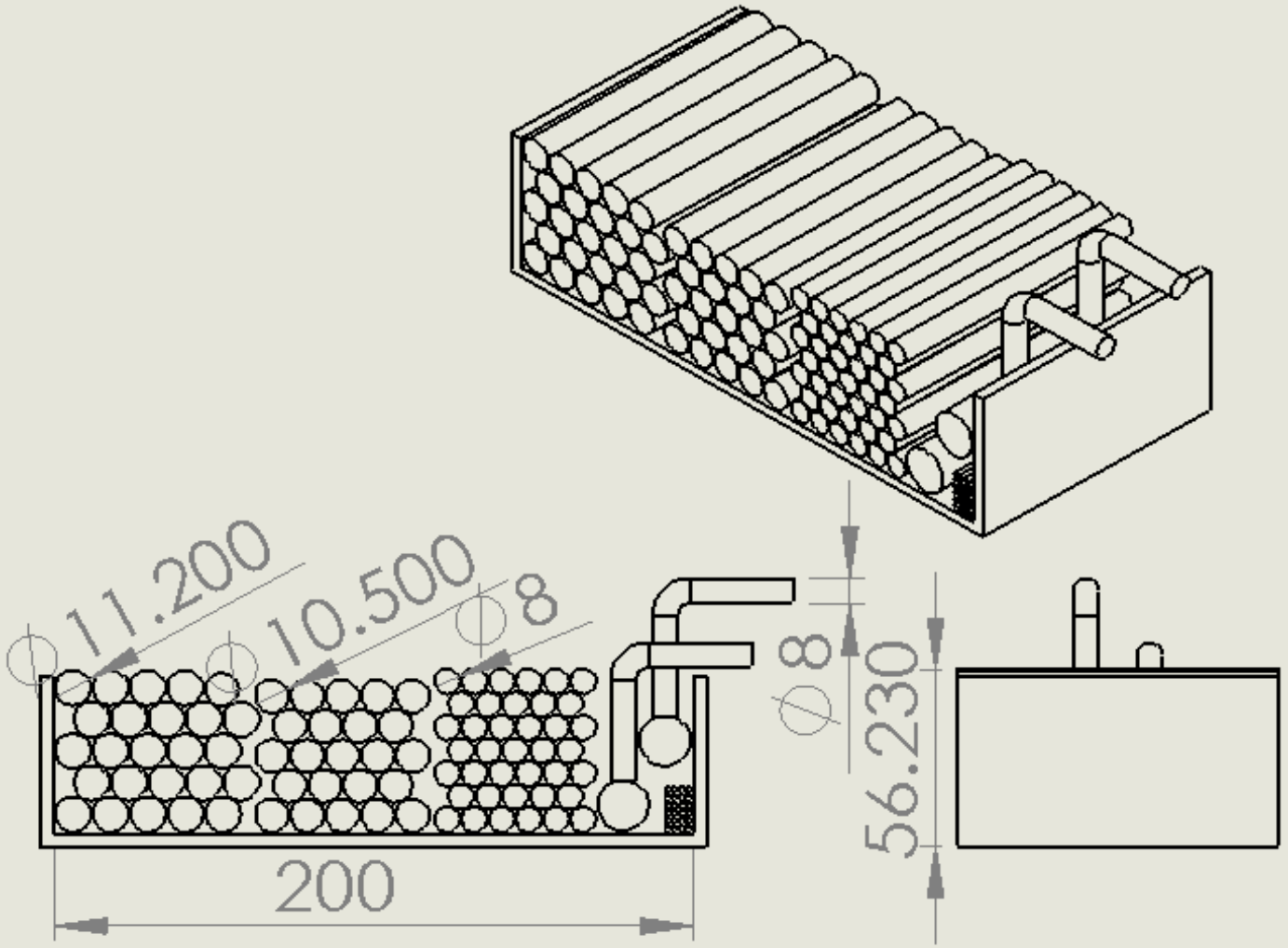




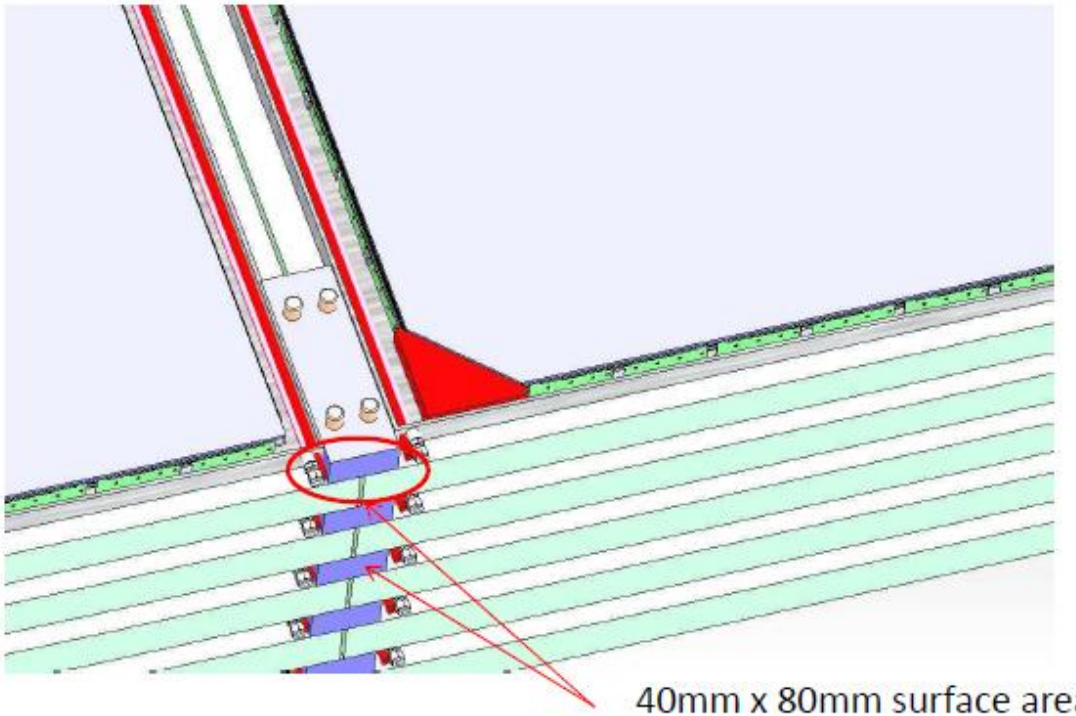
Populating the Cable Tray another way



Cable Tray with 200mm dimension



Place for switches – laying claim



Only place possible to mount "Front end switches", and with max. length of about 220mm

Requesting Integration group to note our claim!

Priorities and promises

- ICAL Electronics documentation
- Delays and Synchronisation scheme
- Timeline for the 8m×8m engineering model
- Location of components and their integration issues
  - For example, LTMs on the detector?
  - Anita's suggestion for trigger signal fan-out
- Chip selection, long-term availability, our policy
- Collision issues on the data network
- Discussion on data interface scheme (VME/LVDS, network scheme (MCU inside FPGA Vs Arm9 processor etc.)
- Power consumption, do we need multi-hit TDC?