Programme of Detectors, Electronics and DAQ sub-group meeting
Day-1 (13/02/2012), Venue – Room#4, New TSH Complex, Ground floor
Chair: V.B.Chandratre/B.Satyanarayana

## Detectors

| Name | Affiliation | Topic | Start | Duration | End |
|---|---|---|---|---|---|
| Sumanta Pal | INO student, TIFR | The performance of RPC Stack at TIFR – concluding remarks | 09:30:00 | 00:15:00 | 09:45:00 |
| Moon Moon Devi | INO student, TIFR | Status of the work on development of Multigap RPC in TIFR | 09:45:00 | 00:15:00 | 10:00:00 |
| Raveendrababu Karanam | INO student, IITM | The Development and Characterization of Cosmic Ray Paddles for INO activities in IITM | 10:00:00 | 00:15:00 | 10:15:00 |
| Salim, Mohammed | AMU | Simulation studies of INO RPC | 10:15:00 | 00:15:00 | 10:30:00 |
| Dogra, Sunil | DU | RPC R&D activities at Delhi Univ. | 10:30:00 | 00:15:00 | 10:45:00 |
| Varchaswi Kashyap | INO student, BARC | Characterizing the of cosmic hodoscope at NPD | 10:45:00 | 00:15:00 | 11:00:00 |
| | | Tea break | 11:00:00 | 00:15:00 | 11:15:00 |
| Nayana Majumdar | SINP | The effects of surface topography on charge induced in a Bakelite RPC | 11:15:00 | 00:20:00 | 11:35:00 |
| Manas Bhuyan | TIFR | RPC gas optimisation studies | 11:35:00 | 00:15:00 | 11:50:00 |
| S.D.Kalmani | TIFR | New gas recycling system | 11:50:00 | 00:15:00 | 12:05:00 |
| S.D.Kalmani | TIFR | Industrial interface and consultancy | 12:05:00 | 00:15:00 | 12:20:00 |
| Piyush Verma | TIFR | Integration issues | 12:20:00 | 00:15:00 | 12:35:00 |
| R.R.Shinde | TIFR | Background radiation studies using demo RPC | 12:35:00 | 00:10:00 | 12:45:00 |
| V.K.Bhandari | PU | Status of RPC work at PU | 12:45:00 | 00:15:00 | 13:00:00 |

## Electronics & DAQ

| | | | | | |
|---|---|---|---|---|---|
| B.Satyanarayana | TIFR | Overview and status | 14:00:00 | 00:30:00 | 14:30:00 |
| Sonal Dhuldhaj | TIFR | FE chip tests with RPC | 14:30:00 | 00:15:00 | 14:45:00 |
| CMEMS | BARC | FE chip upgrade work | 14:45:00 | 00:15:00 | 15:00:00 |
| Mandar Saraf | TIFR | RPC-DAQ module | 15:00:00 | 00:20:00 | 15:20:00 |
| CMEMS | BARC | Status of TDC design | 15:20:00 | 00:15:00 | 15:35:00 |
| B.Satyanarayana | TIFR | Report on IITM activities (Based on Nagendra's report) | 15:35:00 | 00:15:00 | 15:50:00 |
| Mandar Saraf+Piyush Verma | TIFR | Integration issues | 15:50:00 | 00:15:00 | 16:05:00 |
| | | Tea break | 16:05:00 | 00:15:00 | 16:20:00 |
| S.S.Upadhya+B.K.Nagesh | TIFR | Data interface schemes | 16:20:00 | 00:15:00 | 16:35:00 |
| P.Nagaraj | TIFR | Networking scheme | 16:35:00 | 00:15:00 | 16:50:00 |
| Sudeshna Dasgupta | TIFR | Trigger scheme implementation studies | 16:50:00 | 00:15:00 | 17:05:00 |
| B.Satyanarayana+Satyajit Saha | TIFR+ SINP | Power supplies | 17:05:00 | 00:10:00 | 17:15:00 |
| Deepak Samuel+BARC S/W group | TIFR+BARC | Software issues | 17:15:00 | 00:10:00 | 17:25:00 |
| ECIL group | ECIL | Status report | 17:25:00 | 00:10:00 | 17:35:00 |
| | | Discussion | 17:35:00 | 00:25:00 | 18:00:00 |

# News from RPC2012

## SPECIAL MENTION AWARD TO SUDESHNA DAS GUPTA

## for her paper titled

***PROPOSED TRIGGER SCHEME FOR THE ICAL DETECTOR OF INDIA-BASED NEUTRINO OBSERVATORY***

Let us congratulate her for her good work

# ICAL Electronics:

## *miles travelled; milestones to reach*

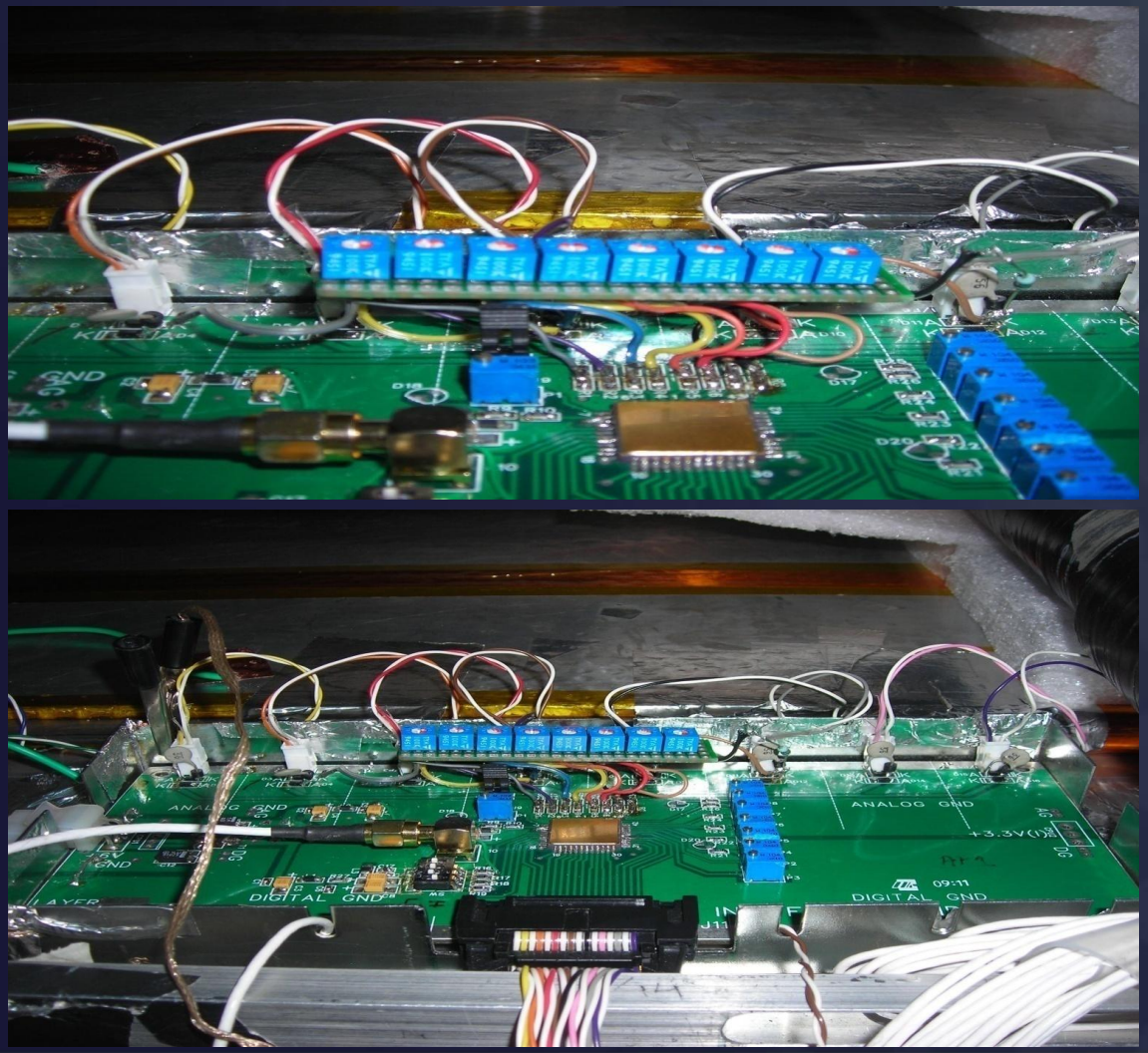
B.Satyanarayana [bsn@tifr.res.in], TIFR, Mumbai

INO Collaboration Meeting, BARC, Mumbai, February 13-15, 2012

# Work in progress and action plan

- Study of amplifier gain and buffer output signal linearity using external pulser
- Detailed study of threshold adjustment and its stability
- Try finer threshold adjustment by connecting a 100KΩ resistor to either side of *P2* trim-pot (which is100KΩ)
- Calibration of threshold for RPC using noise rate and efficiency parameters
- Integration of front-end board with RPC stack at TIFR
- Revision of the chip
  - Solve instability problem while the multiplexer is turned on
  - Separate chips for positive and negative inputs as well as amplifier and discriminator might anyway solve this problem

# Tale of two FE boards AP1, AP2



# Tests of two FE boards on RPCs

- Minimum threshold values possible with AP2 and AP1 boards is at $V_{38}$=1.650V. So the effective threshold is ~250mV.
- Obtained stable noise rates with both boards.
- Noise rates with HMC based preamplifier is double to those obtained with AP2.
- Efficiency with AP2 board  is about half compared to what was obtained with HMC based board.
- Operating gain about 4mV/μA as against the design value 8mV/μA?
- Design revisions by the CMEMS group; ready for a second iteration production?

# Presentations to follow

| | | |
|---|---|---|
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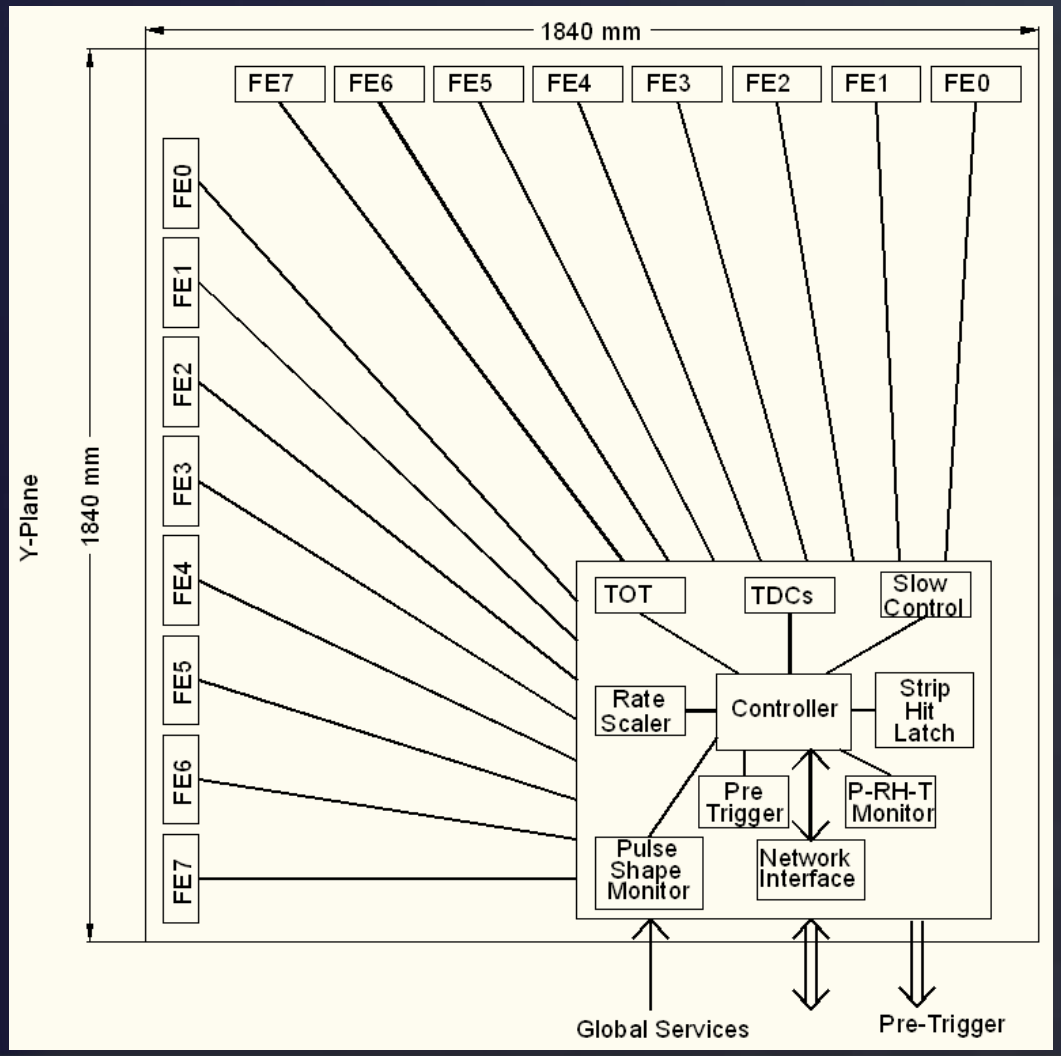
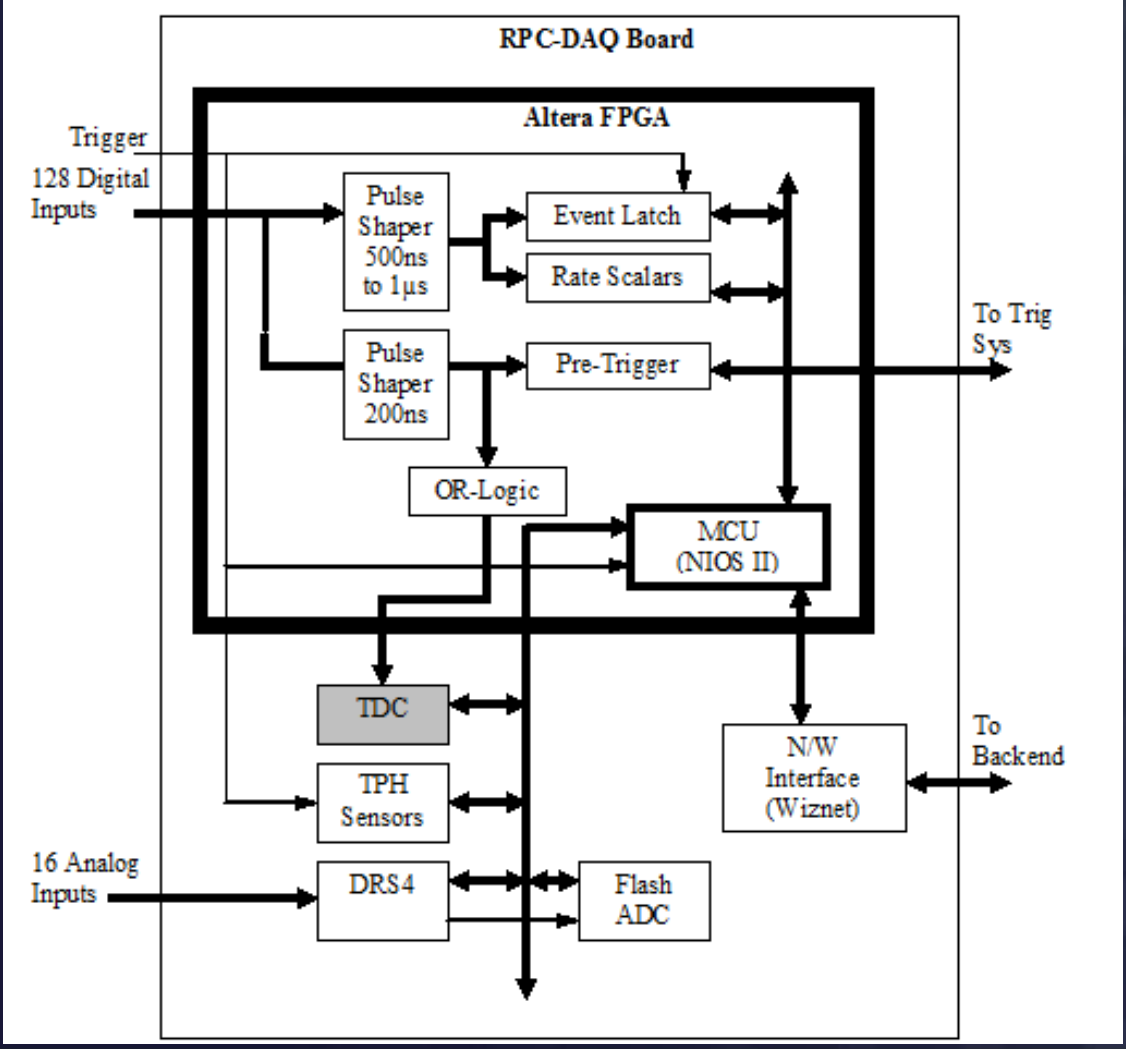
# Functional diagram of RPC-DAQ



# Functional diagram of RPC-DAQ



# Prototyping of RPC-DAQ module

- Using IITM designed MSP430 board
- Digital logic (rate scalers, latches etc.) in FPGA on a trainer kit
- SPI interface between the two
- Serial interface between the MSP board and the PC/host
- Appropriate signal translators for the existing system
- Will lead to a pilot RPC-DAQ board design

# Proof of principle effort (RPC-DAQ)

- Can be tested today on the RPC stacks
- Front-end board with the current board's form-factor, but using ASICs
- RPC-DAQ board with:
  - TDC
  - Waveform sampler
  - Strip-hit latch and rate monitor
  - Controller + data transreceiver
  - Firmware for the above
  - Pre-trigger front-end
  - TPH monitoring
  - Pulse width monitoring
  - Front-end control
  - Signal buffering scheme
  - and GP area or ports for accommodating new blocks
- VME data concentrator module
- Result: Complete readout chain is tested
- Can we use this for RPC QC test stands or what?

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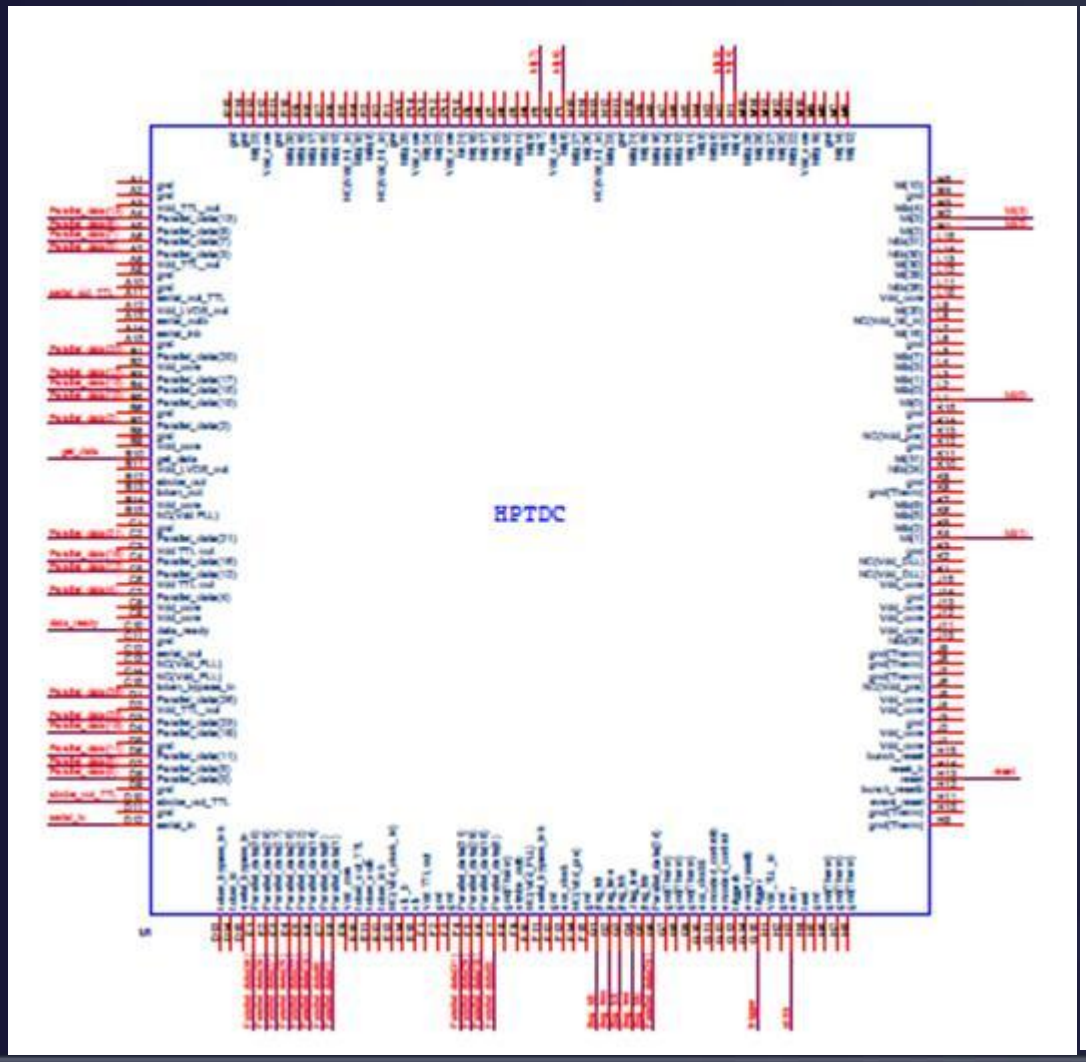
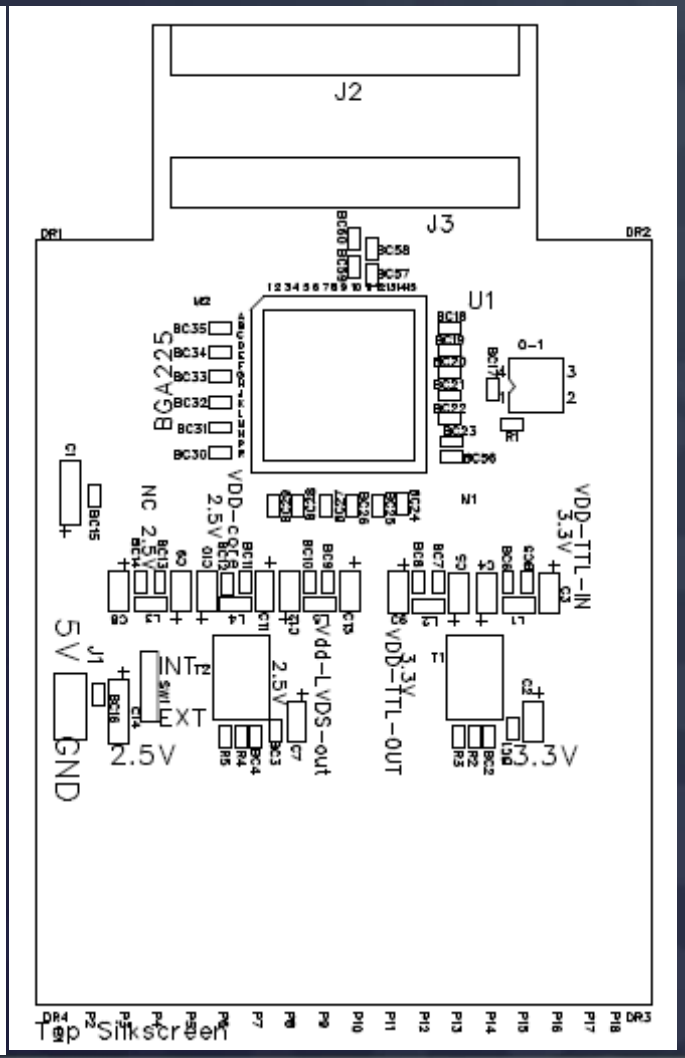
# Specifications of the ICAL timing device

| Parameter | Specification |
|---|---|
| 1. Number of channels | 8 or 16 |
| 2. Least count | 200ps |
| 3. Dynamic range | 2µs (essential), 32µs (desirable) |
| 4. Number of bits | 14 (essential), 18 (desirable) |
| 5. Type | Common stop |
| 6. Hits | Single hit (essential), multi hit (desirable) |
| 7. Double hit resolution | 5-10ns |
| 8. Readout buffer size | 128 words (maximum) |
| 9. Signal and control inputs | LVDS and LVTTL respectively |
| 10. DNL/INL | 100ps (typical) |
| 11. Power rail | 3.0 to 3.6V (suggested) |
| 12. Control and readout interface | SPI (essential), SPI + parallel (desirable) |

# Place-holder for TDC on RPC-DAQ prototype



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# Chip design activities at IIT Madras

- Front end amplifier (gain ~100, BW ~500MHz)
- Time to digital converter (delay line based, 50ps)
- Analog memory (64 samples, 2GSPS, 8-bit  10MHz ADC)
- More on these developments from Anil → Nagendra

# Harshit Vaishnav's thesis

In this project, design of a front end circuitry for neutrino detectors is presented. The system consists of a high speed front end amplifier and latching circuitry. A time to digital converter (TDC) is used to measure the time of arrival of the input with respect to a reference start. A delay locked loop is used to stabilize the delays against PVT variations. A phase locked loop is used to generate a high frequency clock from a low frequency input clock. A digital back-end is designed to process the data digitally and to output a serial data stream.

The design is implemented in 0.13 µm CMOS process. The TDC has a resolution of 125 ps and a range of 131 µs. It occupies 0.24 $mm^2$ area and consumes negligible static power. The DLL occupies 0.12 $mm^2$ area and consumes a power of 2 mW. The amplifier has a DC gain of 41.5 dB and a bandwidth of 513 MHz and consumes 0.2 mW power. The design will be sent for fabrication in the UMC 0.13 µm CMOS process.

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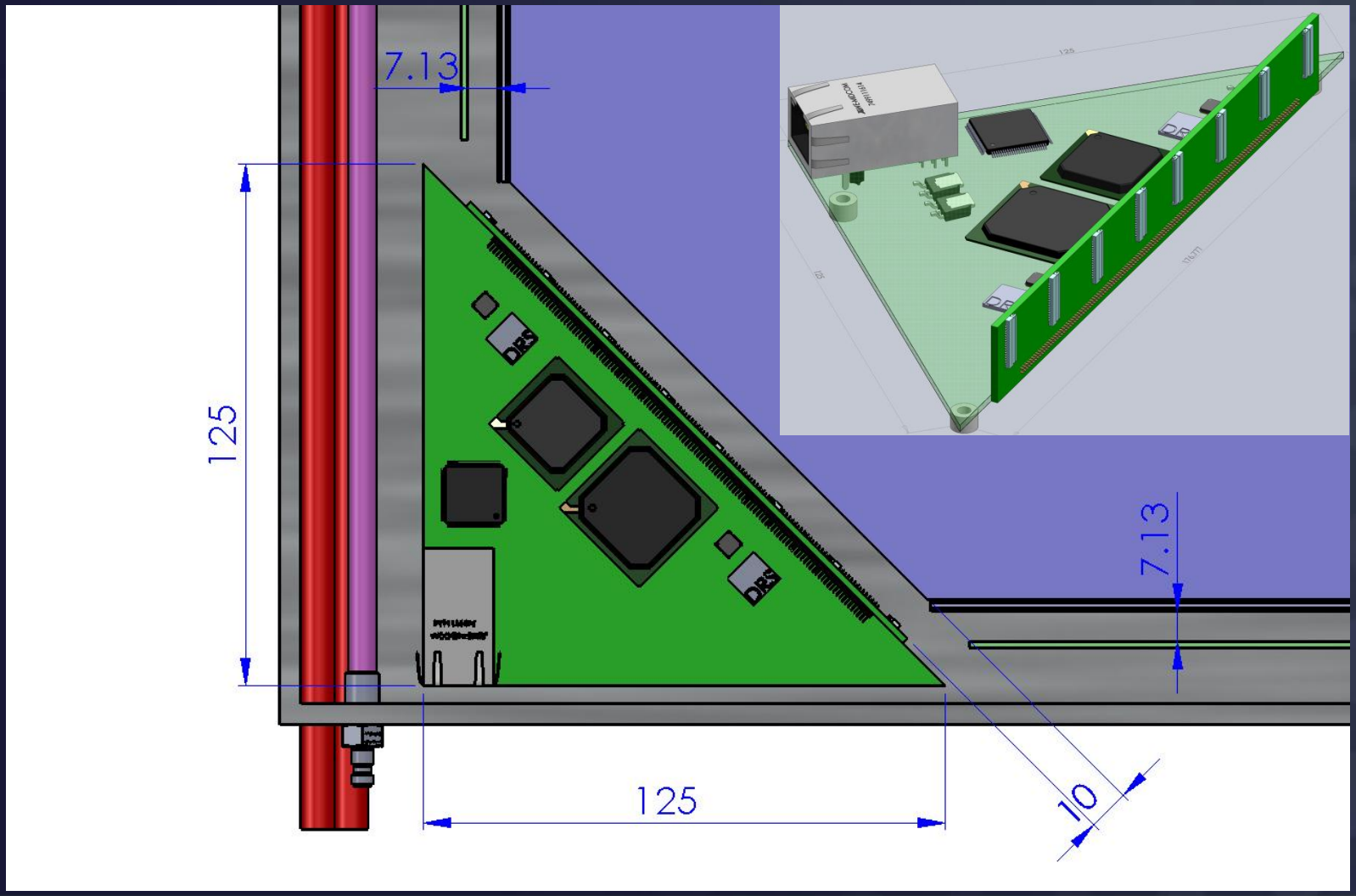
# Integration issues

- Mounting of electronics on top of RPC is not *liked* – wasting of space/volume
- Suggestion to mount on the sides
- Increase the shamperred areas on four corners of the RPC
- Mount DAQ for two planes (X & Y) and power supplies (LV, HV) in these areas
- Front-ends to be mounted along the planes
- Issue of pickup-strips to the front-end solved automatically!
- Modeling and prototyping in progress
- Industrial dimensions of glass is helping this scheme

# Fighting for an mm in a 132m×26m×20m cavern!



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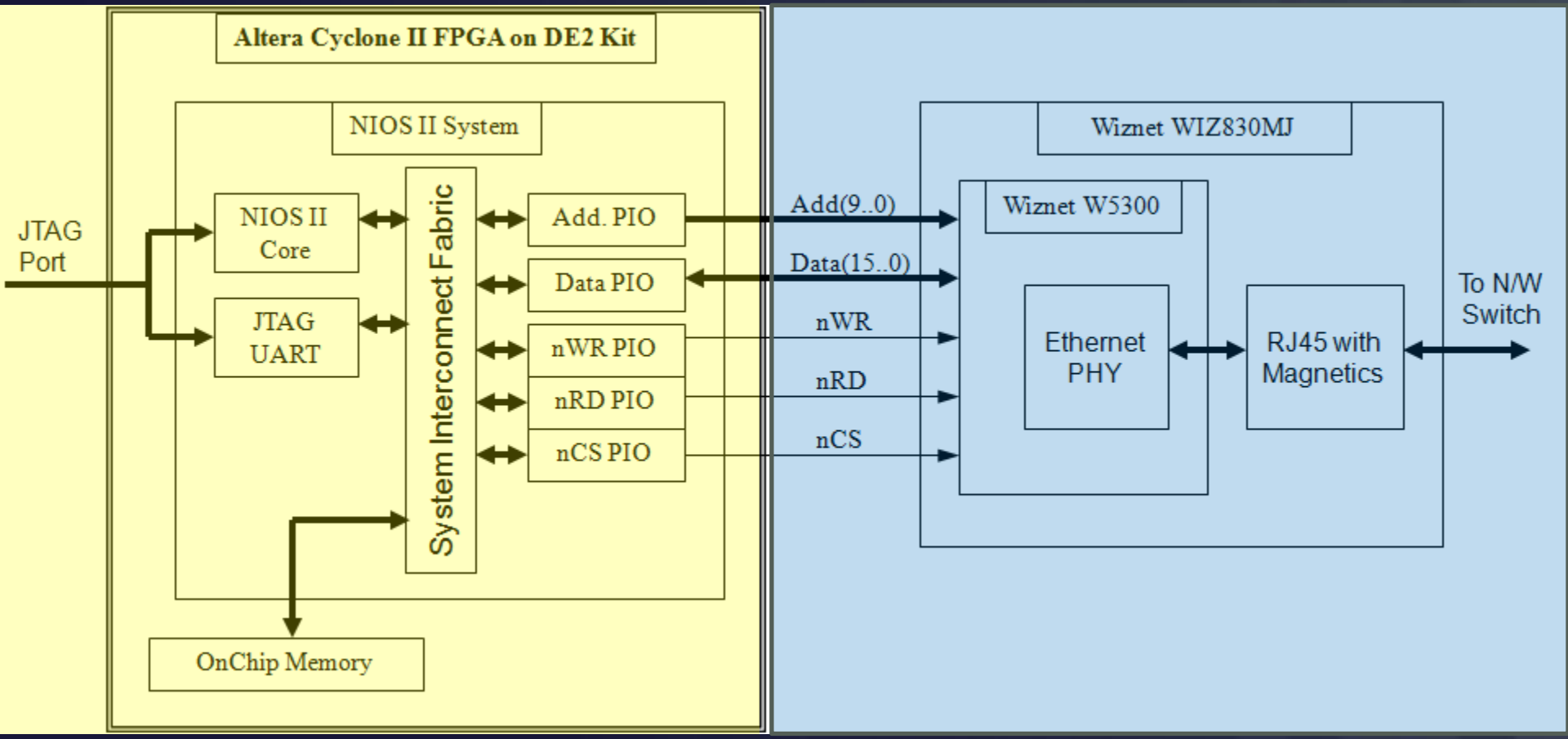
# Networked DAQ scheme

- Alternate approach for VME back-end
- Choose  appropriate controller
- Simplified system design, cabling
- Speed, switching, protocols

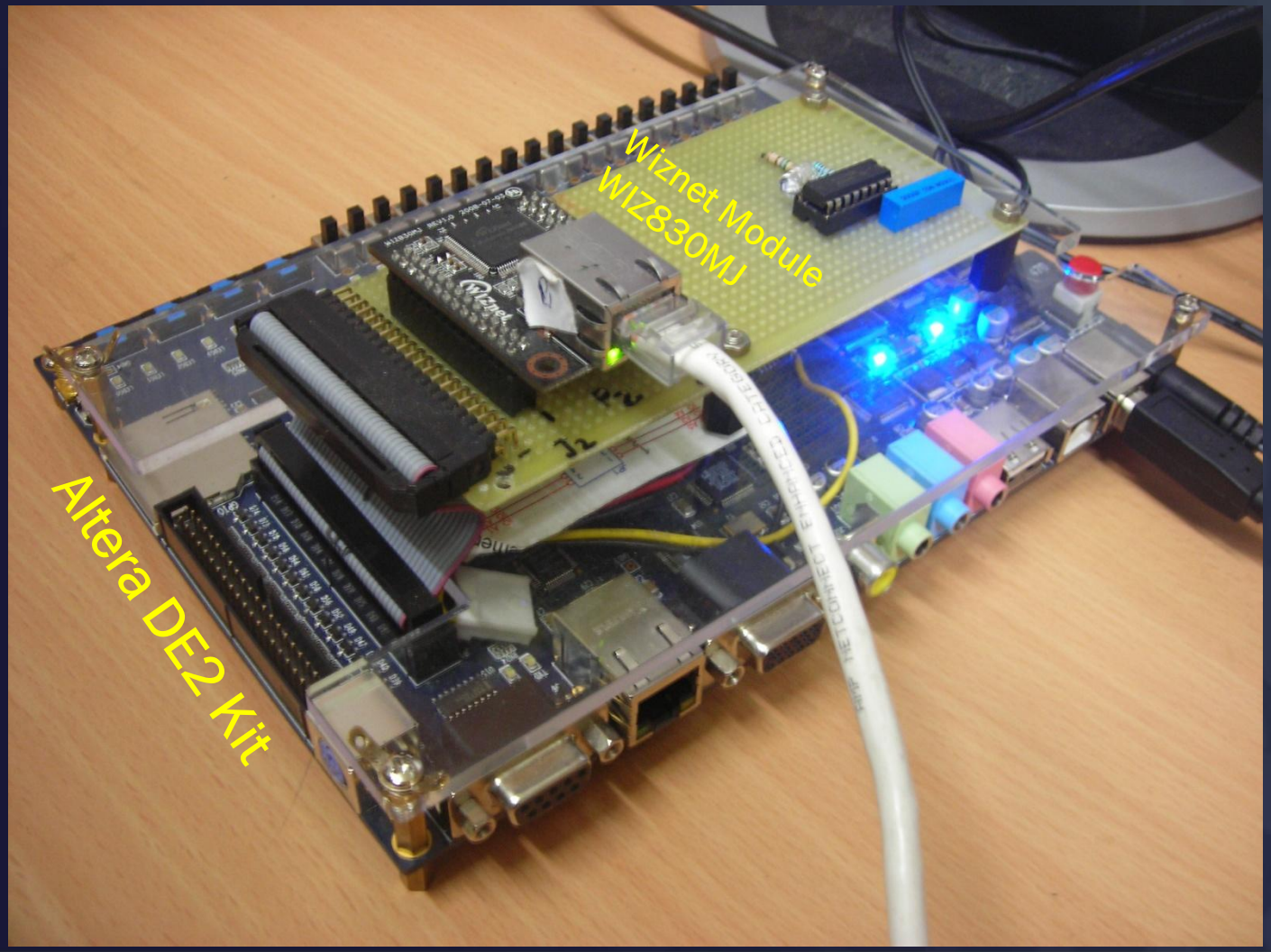
# Wiznet to FPGA Interface



# Current work on data interface

- Altera DE2 kit with Cyclone II EP2C35 FPGA
- FPGA configured with NIOS II system using SOPC Builder a part of Altera Quartus
- Wiznet W5300 interfaced to NIOS II in port mapped I/O mode
- Software developed in NIOS II EDS IDE in C
- Established two way communication between PC and Wiznet test setup.

# Wiznet to FPGA Interface



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# Event data rates

- Event Data per Trigger is as follows: (64 strips on each plane of RPC)
- TDC data = 1 channel for 8 strips and both the edges per hit, up to 4 hits per channel per event = 16 channels x 2 edges x 4 hits x 16 bits = 2048 bits
- Hit data per RPC = 128 bits
- RPC ID = 32 bits
- Event ID = 32 bits
- Time Stamp = 64 bits
- DRS data = 16 channels x 1000 samples x 16 bits = 256000 bits
- (DRS data comes in event data only if we get summed analog outputs from the preamplifier)
- Data size per event per RPC
- With DRS data, $D_R$ = 2048 + 128 + 32 + 32 + 64 + 256000 = 258,304 bits
- Without DRS data, $D_R$ = 2048 + 128 + 32 + 32 + 64 = 2,304 bits
- **Considering 1Hz trigger rate, Maximum Data Rate at each RPC = 252.25 kbps**

- Total data size per event across 3 modules
- With DRS data, $D_T$ = 258304 x 28800 = 7,439,155,200 bits i.e. 6.928 Gbits
- Without DRS data, $D_T$ = 2304 x 28800 = 66,355,200 bits i.e. 63.28125 Mbits
- Considering 1Hz trigger rate, Maximum Data Rate at backend = **6.928 Gbps**

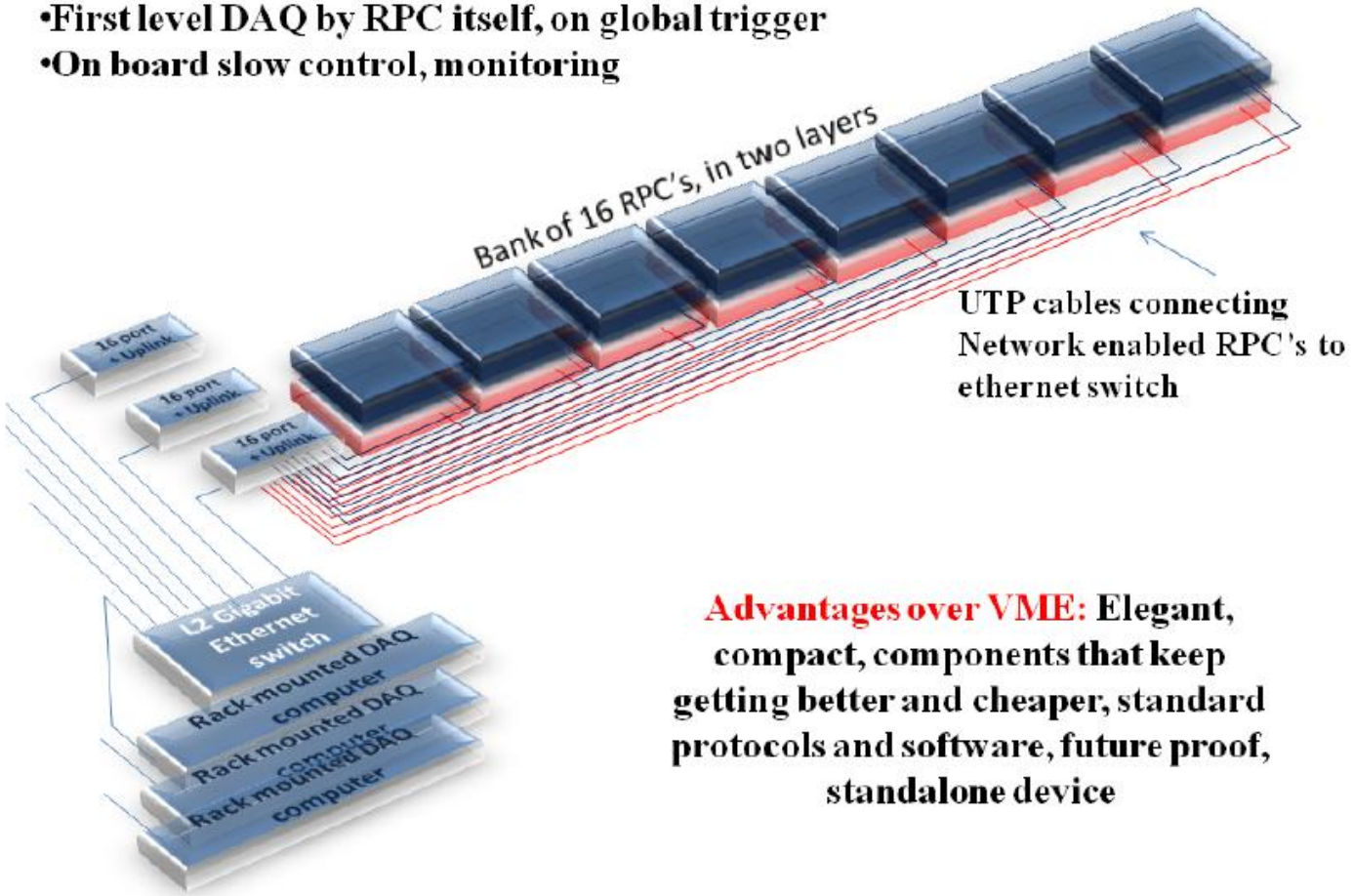
# Monitor data rates

- Monitor Data per 10 seconds
- We require to monitor 1 pick-up strip per plane per RPC.
- Monitor Data per strip = 24 bits
- Channel ID = 8 bits
- RPC ID = 32 bits
- Mon Event ID = 32 bits
- Ambient Sensors' data = 3 x 16 bits = 48 bits
- Time Stamp = 64 bits
- DRS data = 1000 pulses (if noise rate is 100Hz) x 16 bits x 100 samples = 1600000 bits
- (DRS data comes in monitoring data only if we get multiplexed analog outputs from the preamplifier)

- Data size per 10 seconds RPC
- With DRS data = 24 + 8 + 32 + 32 + 48 + 64 + 2048 + 1600000 = 1,602,256 bits
- Without DRS data = 24 + 8 + 32 + 32 + 48 + 64 + 2048 = 2,256 bits
- **Max Data Rate for 10 second monitoring period per RPC = 156.47 kbps**

# Networking issues, devices

- RPC's designed as network devices
- Each RPC will have Embedded μP + Linux + TCP/IP
- First level DAQ by RPC itself, on global trigger
- On board slow control, monitoring




**Advantages over VME:** Elegant, compact, components that keep getting better and cheaper, standard protocols and software, future proof, standalone device

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# Trigger scheme for ICAL

- Validation of the trigger schemes
- Ready to go for implementation
- Integration issues
  - Segment trigger module positions
  - Pre-trigger signal driving issues
- Specifications:
  - Coincidence window: 100ns
  - Maximum trigger latency: 1us
  - Singles rate for RPC detector pickup strips: 250 Hz
  - The skew and jitter in arrival instant of the global trigger at different RPCs should be as low possible
- News: BARC team (Anita Behere *et al*) joined the trigger team for implementation

# Trigger implementation

- Trigger scheme developed and validated
- Layout of trigger scheme implementation
- Study of LVDS transmission
- Conceptual design of the trigger modules
- FPGA logic development
- Validation of design concept in FTM

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# Role of waveform sampler for ICAL

- Walk correction of TDC data
- Leading edge discriminator
- Time over threshold information
- Pulse profile, height and width monitoring
- Remote display of RPC signals

# Consolidation of its function

- Better understood DRS4 – thanks to the *demo RPC* project!
- Not sure though, if we understood the exact role and hence its exact operation scheme ICAL electronics
- Do we use in both event and monitoring modes?
- The above required different front-ends for the analog front-ends
  - Multiplexed analog signal
    - Easier to implement?
    - Timing problem in event mode
  - Summed/ORed analog signal
    - Relatively difficult to implement?
    - No timing issue, hit channel id could be inferred
- Where is the chip?

# Power supply options

- High voltage (Central scheme)
  - Two options: a channel at 12kV or two channels at ±6kV
  - Consider powering 4 RPC with a single HV channel (10μA current)
  - Cable diameter an integration issues, connectors a cost issue
- High voltage (Distributed scheme)
  - DC-DCHV converters
  - Each RPC has to be identical to the others
  - Each RPC will have its own DC-HVDC converter for generating HV and LV
- Low voltage
  - Power budget 25W per RPC
  - How many low voltages?
- Space for DC-DC converters inside the RPC unit an integration issue
- Magnetic field
  - Fringe field mostly is below 100 Gauss
  - But some places between 100 and 1000 Gauss
  - Difference between 100 and 1000 Gauss is relevant for the design of the DC-HVDC

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# Software components

- RPC-DAQ controller firmware
- Backend online DAQ system
- Local and remote shift consoles
- Data packing and archival
- Event and monitor display panels
- Event data quality monitors
- Slow control and monitor consoles
- Database standards
- Plotting and analysis software standards
- OS and development platforms

# Software

- News: BARC team (Diwakar, Padmini *et al*) joined the software team
- Back-end Data Acquisition and Monitoring System
  - Event Data Acquisition
  - Periodic Online Monitoring of RPC Parameters
  - Event Data Quality Monitoring
  - Control and Monitoring Console
  - Local and Remote Consoles
- Front-end firmware/software will be responsibility of the TIFR group
- Scope for more players (especially physicists)

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| CMEMS group | BARC | Status of TDC design |
| Nagendra Krishnapura | IITM | Integrated Circuits for the INO |
| Mandar Saraf+Piyush Verma | TIFR | Integration issues |
| S.S.Upadhya+B.K.Nagesh | TIFR | Data interface schemes |
| P.Nagaraj | TIFR | Networking scheme |
| Sudeshna Dasgupta | TIFR | Trigger scheme implementation studies |
| B.Satyanarayana+Satyajit Saha | TIFR+ SINP | Power supplies |
| Deepak Samuel+BARC S/W group | TIFR+BARC | Software issues |
| ECIL group | ECIL | Status report |

# Industrial interfaces, services

# Presentations to follow

| B.Satyanarayana | TIFR | Overview and status |
|---|---|---|
| Sonal Dhuldhaj | TIFR | FE chip tests with RPC |
| CMEMS group | BARC | FE chip upgrade work |
| Mandar Saraf | TIFR | RPC-DAQ module |
| CMEMS group | BARC | Status of TDC design |
| Nagendra Krishnapura | IITM | Integrated Circuits for the INO |
| Mandar Saraf+Piyush Verma | TIFR | Integration issues |
| S.S.Upadhya+B.K.Nagesh | TIFR | Data interface schemes |
| P.Nagaraj | TIFR | Networking scheme |
| Sudeshna Dasgupta | TIFR | Trigger scheme implementation studies |
| B.Satyanarayana+Satyajit Saha | TIFR+ SINP | Power supplies |
| Deepak Samuel+BARC S/W group | TIFR+BARC | Software issues |
| ECIL group | ECIL | Status report |

# Priorities and promises

- ICAL Electronics documentation
- Delays and Synchronisation scheme
- Timeline for the 8m×8m engineering model
- Location of components and their integration issues