The India-based Neutrino Observatory (INO) is currently engaged in designing a massive neutrino detector, called Iron Calorimeter (ICAL) to be located in a cavern in South India. The detector uses 56mm iron slabs arranged as about 150 layers and weighing about 50Ktons as the interacting medium for the neutrinos. Resistive Plate Chambers (RPCs) of 1.84m X 1.84m in area, inserted between the iron layers will be used active detector medium. ICAL will use about 29,000 RPCs. The total number of electronic readout channels will be about 3.6 million. The detector will be built as three equal modules, of which the first module is expected to be completed in about 5 years.

The RPCs will be operated in the (low gas gain) avalanche mode. The detector pulses are about 0.5 to 2mV in amplitude (across a 50Ω load) and therefore require external voltage amplification of 100-200. While the rise time of these pulses is typically under a nano second, the opening width (after amplification) is about 20-30 nSec. This along with the following discriminator and pulse shaping stages are being planned to be designed into ASICs and mounted on the detector body itself.

The main information to record as far as the physics events are concerned is the chamber strip hit (Boolean) and its timing with reference to that of the detector trigger signal - the resolution specification for the latter being bout 200pS. Apart from this, we will also record a lot of monitoring data in the background - in channel multiplexed manner, which is useful to keep track of health of the chambers. One such data is on the noise/background rate of individual channels, which remains fairly constant if integrated for long enough period.

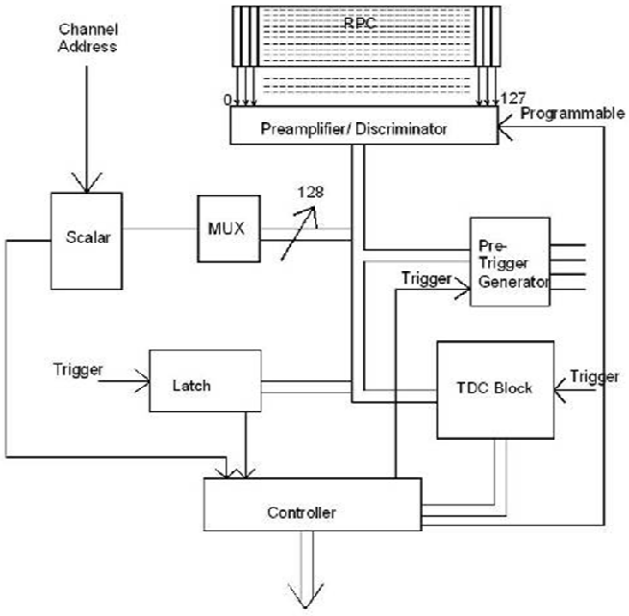

Figure 1: Proposed scheme of the ICAL electronics

Main architecture of the data acquisition system (DAQ) depends whether we plan to build a triggered or trigger-less system. The triggered system, using the Boolean information of all the readout channels, produces an on-line trigger using typically distributed (at least two-tiered)

combinatorial logic. This hardware trigger signal is used by the readout sub-system to record the data. On the other hand, in a trigger-less scheme, all the data is time-stamped and sent to the back-end processors to reconstruct the events and record if found interesting. The main issues in the trigger-less system are time-stamping resolution and noise/background rates of the readout channels.

We have decided to start our preliminary design using the more conventional triggered scheme (Figure 1). We may look at the alternate design using trigger-less scheme later, if needed. Design of a sophisticated and flexible trigger system is an important task in itself.

Another idea that we are zeroing on, is to use the RPC detector (with about 128-electronic channels) as the basic and stand-alone unit for the purpose of designing electronics and other services. All the front-end processing of this unit will be done on the detector itself and the data is sent to the back-end on high-speed serial optical links. We plan to have a embedded processor on each RPC unit, which will take care of all the tasks mentioned above.

Another important role of the DAQ is the slow control and monitoring of various ambient as well as operating parameters. This includes gas systems, magnet, power supplies, temperature, RH, barometric pressure and so on.

We will discuss the technical aspects of the current overall scheme of the electronics, trigger, data acquisition, control and monitoring systems suitable for the ICAL detector. We would like to get comments and suggestions from Dr Yasuo Arai san on our general scheme as well specific inputs on the design of timing elements and his expertise on the novel VSLI design techniques. We also would like to discuss with Dr Arai san on the front-end design issues as well as data-transfer techniques and hardware from the front-end to back-end. We have seen this hardware and discussed with his colleagues in the labs when we visited KEK last year. We also would like Dr Arai san sharing his experiences on the industries' role in design and fabrication, quality control standards, identification of chip fabrication facilities etc.