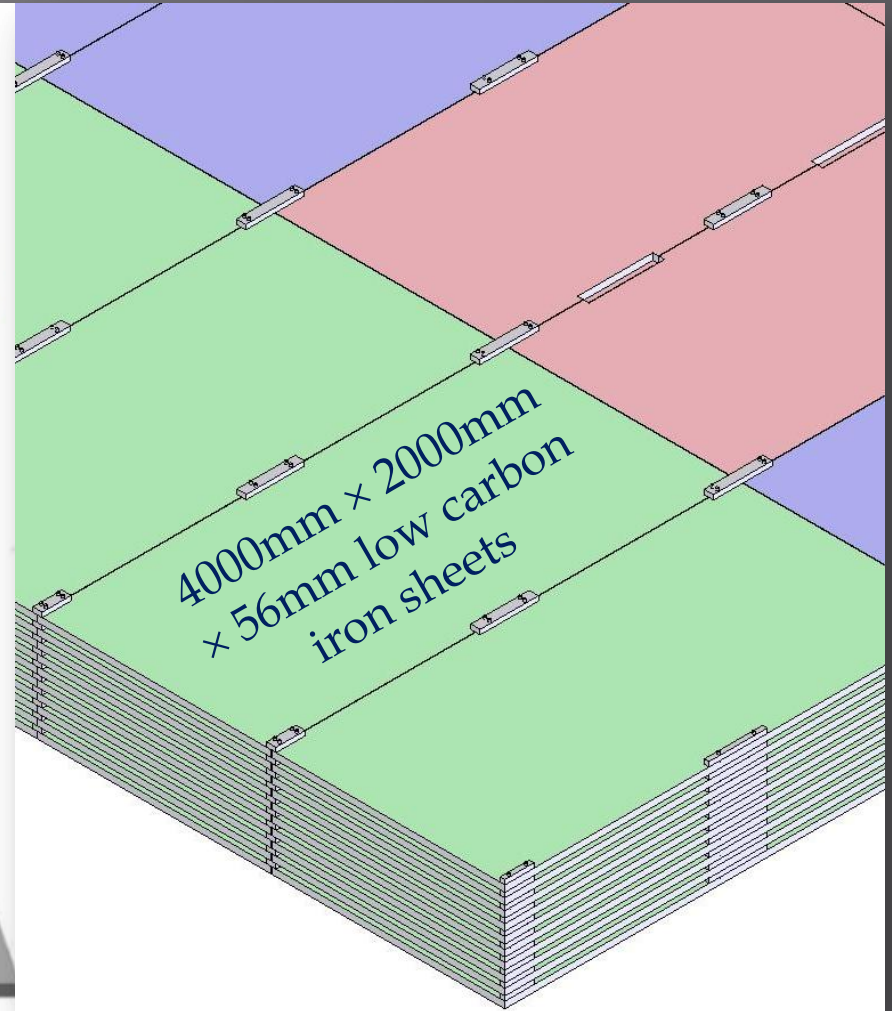
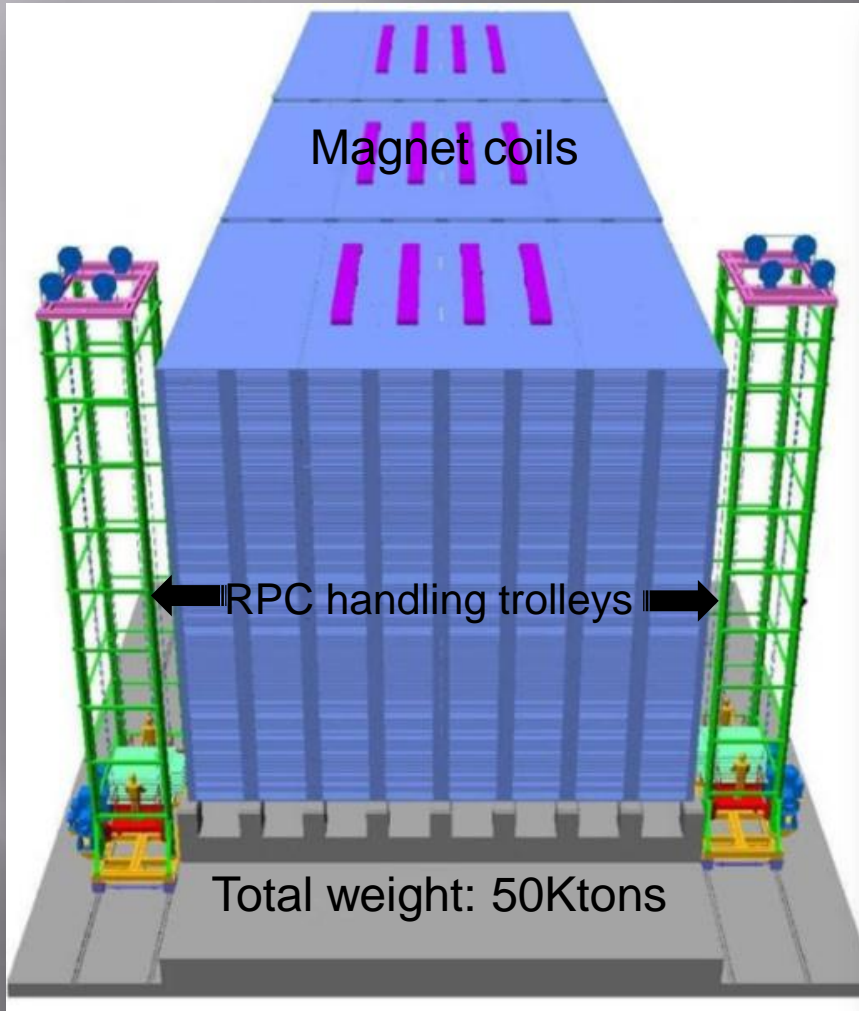


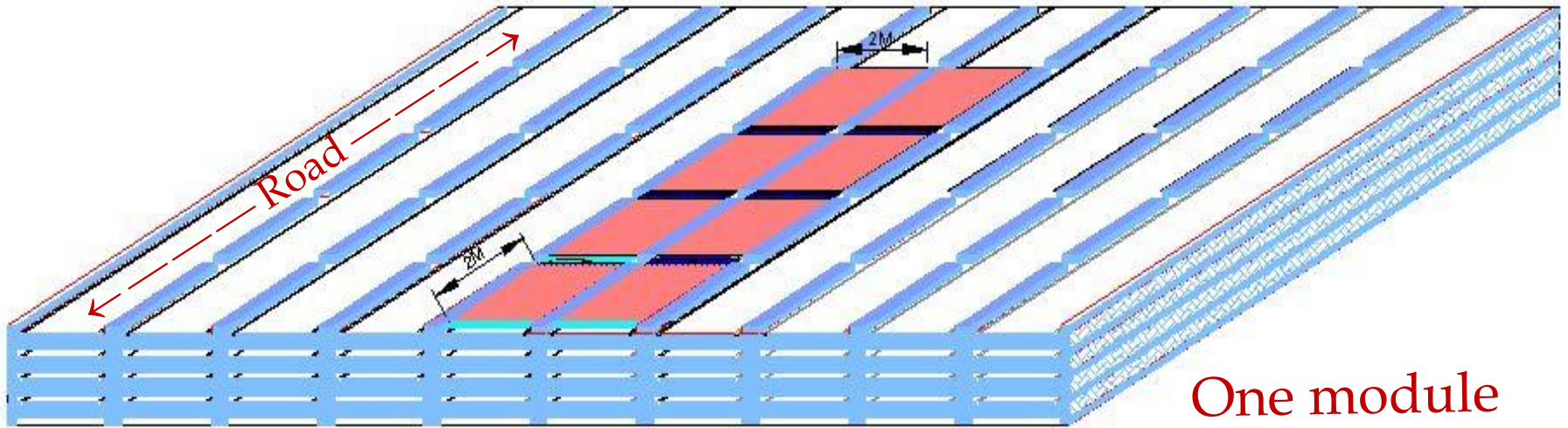
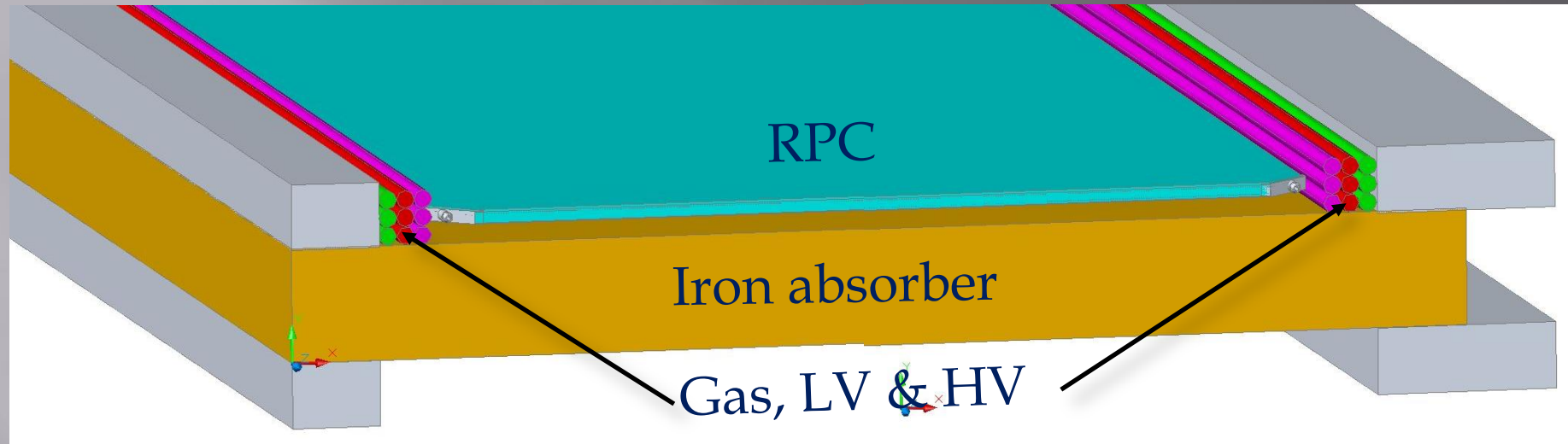
DISCUSSION MEETING ON ICAL ELECTRONICS

SINP, Kolkata April 29-30, 2011

ICAL detector and construction



RPC in the ICAL detector

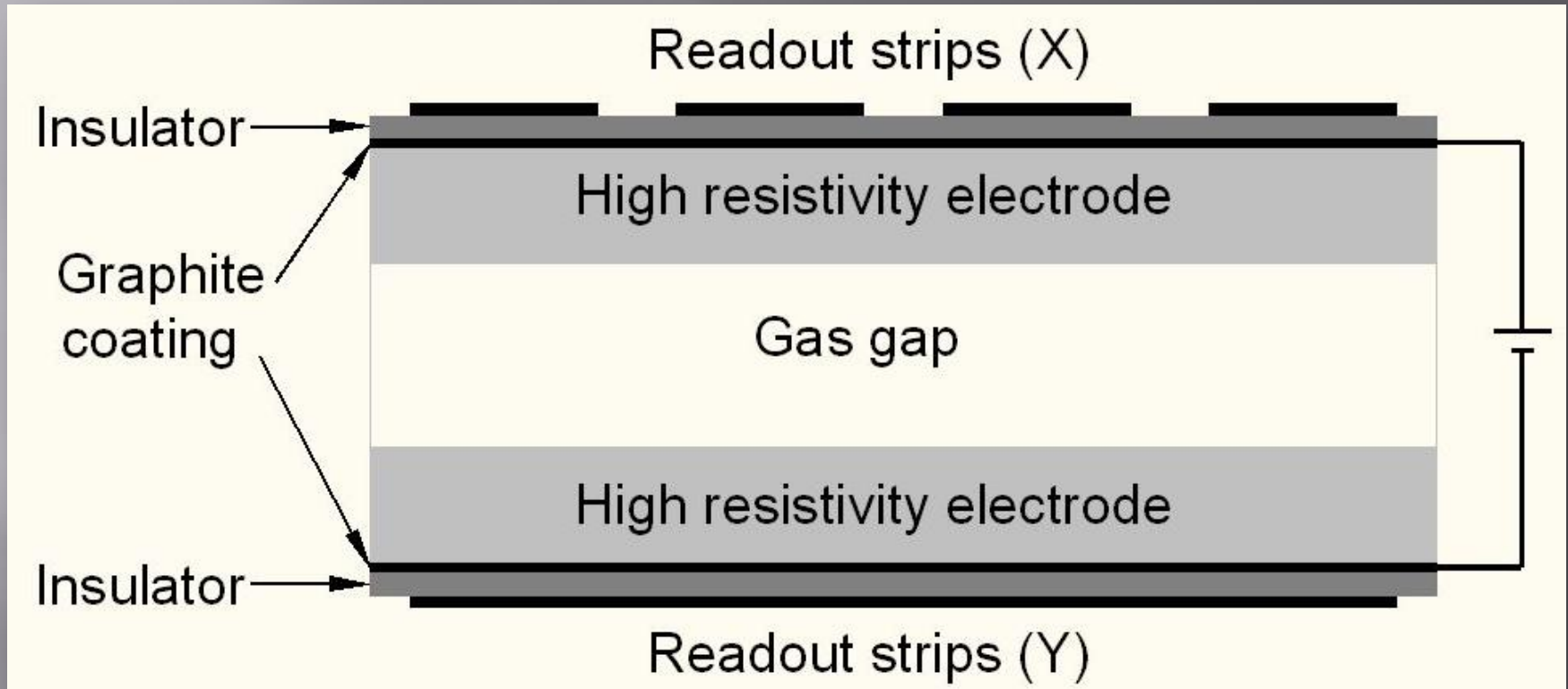


One module

Factsheet of ICAL detector

No. of modules	3
Module dimensions	16m × 16m × 14.5m
Detector dimensions	48.4m × 16m × 14.5m
No. of layers	150
Iron plate thickness	56mm
Gap for RPC trays	40mm
Magnetic field	1.3Tesla
RPC dimensions	1,950mm × 1,840mm × 26mm
Readout strip pitch	30mm
No. of RPCs/Road/Layer	8
No. of Roads/Layer/Module	8
No. of RPC units/Layer	192
No. of RPC units	28,800 (97,505m ²)
No. of readout strips	3,686,400

Schematic of a basic RPC



- ❖ Glass (bakelite) for electrodes
- ❖ Special paint mixture for semi-resistive coating
- ❖ Plastic honeycomb laminations as pick-up panel
- ❖ Special plastic films for insulation
- ❖ Avalanche (streamer) mode of operation
- ❖ Gas: $\text{R134a} + \text{Iso-butane} + \text{SF}_6 = 95.5 + 4.2 + 0.3$ ($\text{R134a} + \text{Iso-butane} + \text{Argon} = 56 + 7 + 37$)

Honeycomb pickup panel



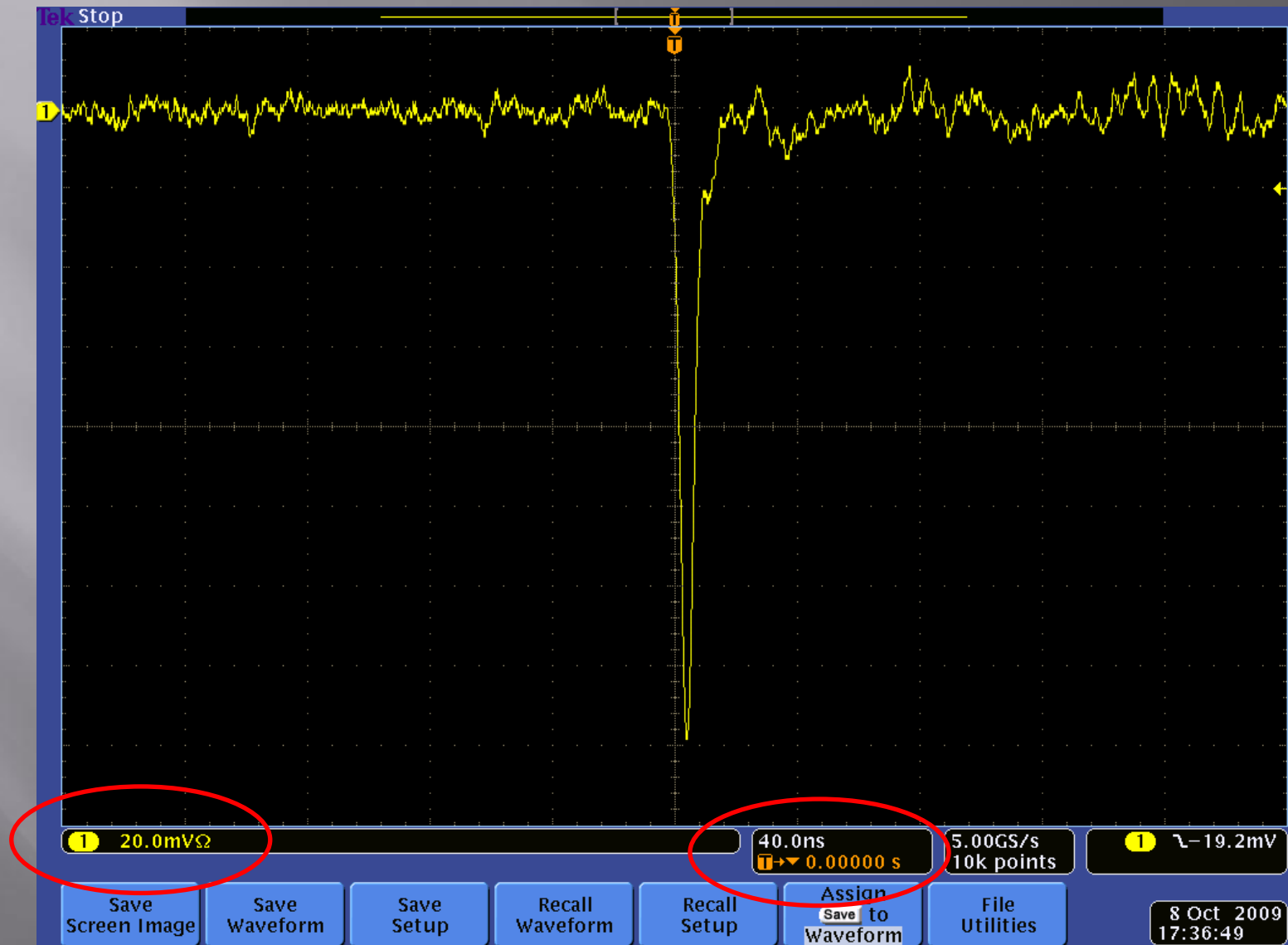
Terminations on the non-readout end



Machined pickup strips on honeycomb panel

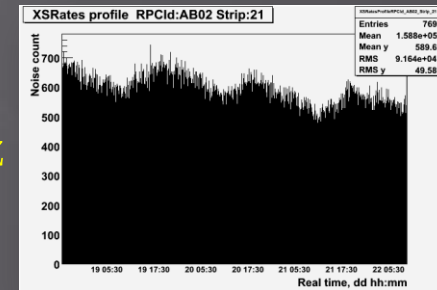
Preamp connections on the readout end

Post amplifier RPC pulse profile



DAQ system requirements

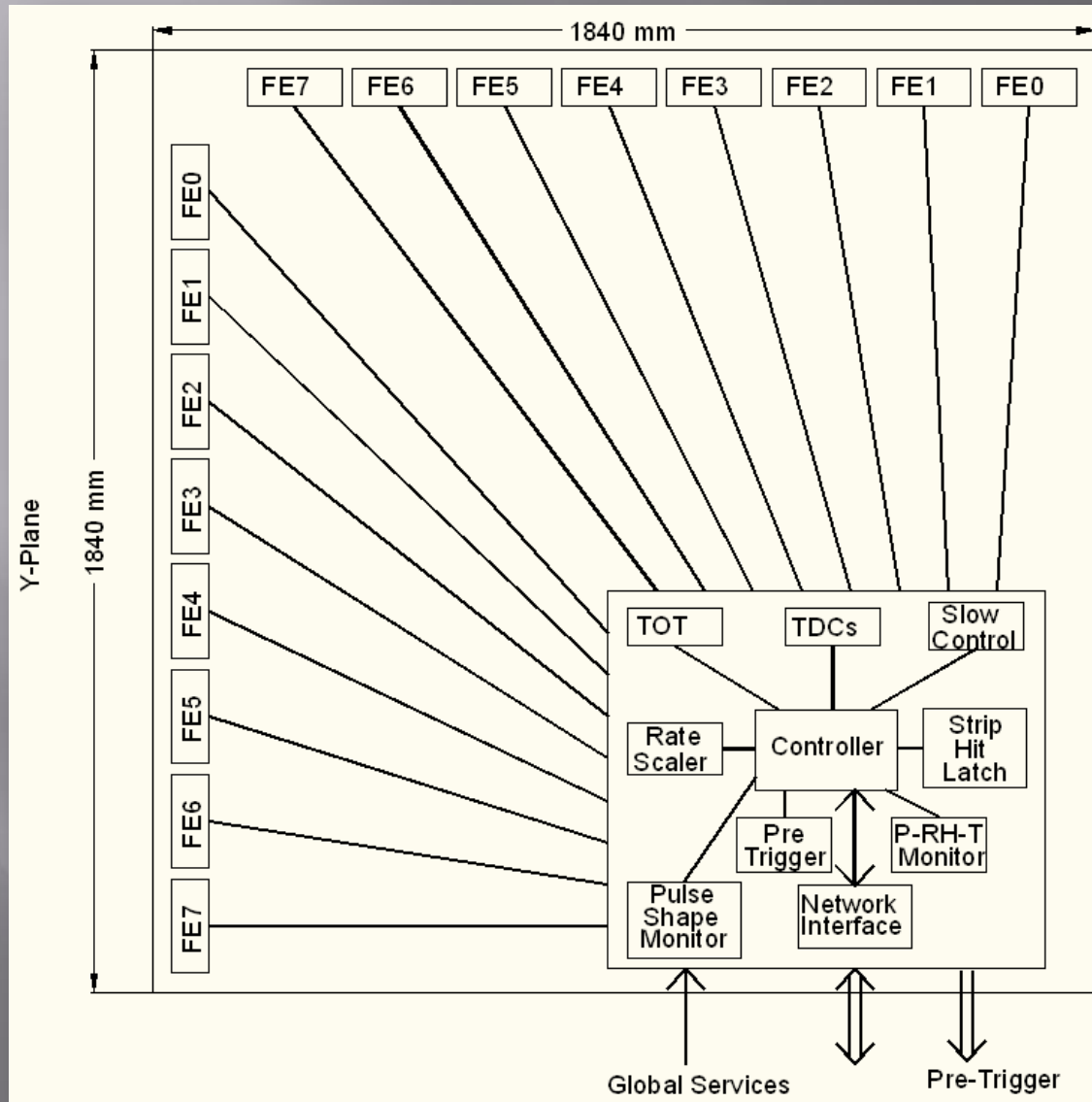
- ▣ Information to record on trigger
 - Strip hit (1-bit resolution)
 - Timing (200ps LC)
 - Time Over Threshold (used for time-walk correction)
 - ▣ TDC can measure TOT as well.
 - Pulse profile (using waveform sampler, 200ps LC)
- ▣ Rates
 - Individual strip background rates on surface $\sim 300\text{Hz}$
 - ▣ Underground rates differ: depth, rock radiation etc.
 - Muon event rate $\sim 10\text{Hz}$ (The 'blue' book says $\sim 2\text{Hz}$)
- ▣ On-line monitor
 - RPC parameters (High voltage, current)
 - Ambient parameters (T, P, RH)
 - D.C. power supplies, thresholds
 - Gas systems and magnet control and monitoring



Expected data sizes and rates

- ▣ Strip hit - 128bits
- ▣ TDC: 16 channels (8 strips ORed), dual edges, 16 hits /ch, 16-bits - $16 \times 2 \times 8 \times 16 = 4096\text{bits}$
- ▣ Pulse profile: 16 channels, 50ns, 200ps LC, 8bits - $16 \times 50 \times 5 \times 8 = 32\text{kbits!}$
- ▣ RPC id - 16bits
- ▣ Event id - 32bits
- ▣ Time stamp - 100bits!
- ▣ Event size - 4272bits (excl. pulse profile + time stamp)
- ▣ Assuming trigger rate to be 10Hz, event data rate = 42720bits/s
- ▣ Ambient sensors (TPH) - $3 \times 16 = 48\text{bits/s}$
- ▣ Noise rate data (1 second, 16 channels, 32bits) - 512bits/s
- ▣ Estimated data rate/RPC - $42720\text{bits/s} + 48\text{bits/s} + 512\text{bits/s} = 43280\text{bits/s}$
- ▣ Add formatters, headers etc. - 50kbits/s/RPC
- ▣ Add data from at least 8 RPCs = $8 \times 50\text{kbits/s} = 400\text{kbits/s}$
- ▣ No data compression or zero suppression considered.
- ▣ Channel occupancy a few%
- ▣ Pulse height analyser - do we need it? Difficult to implement as online monitor routine

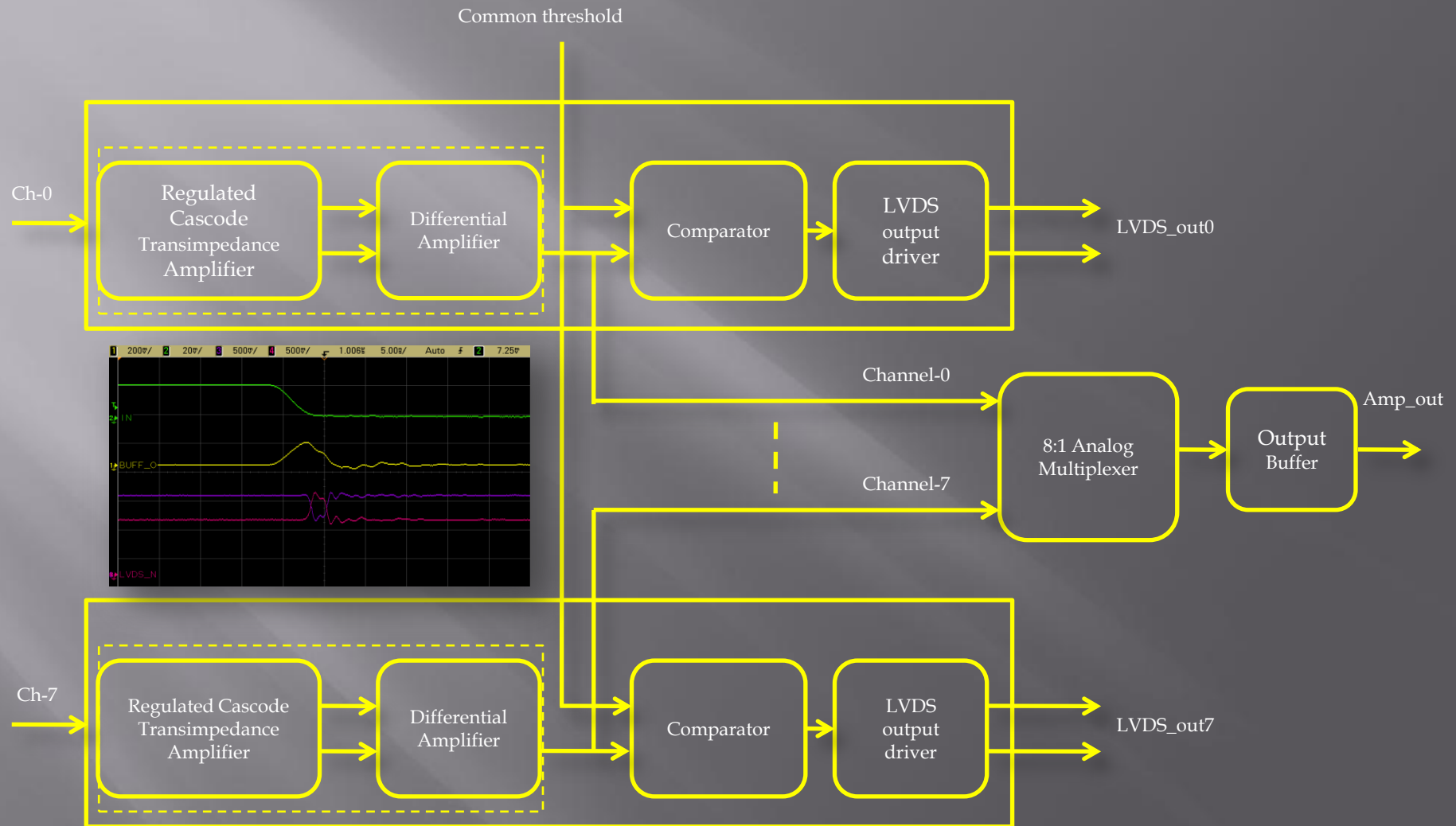
Functional diagram of RPC-DAQ



Front-end to RPC-DAQ bus

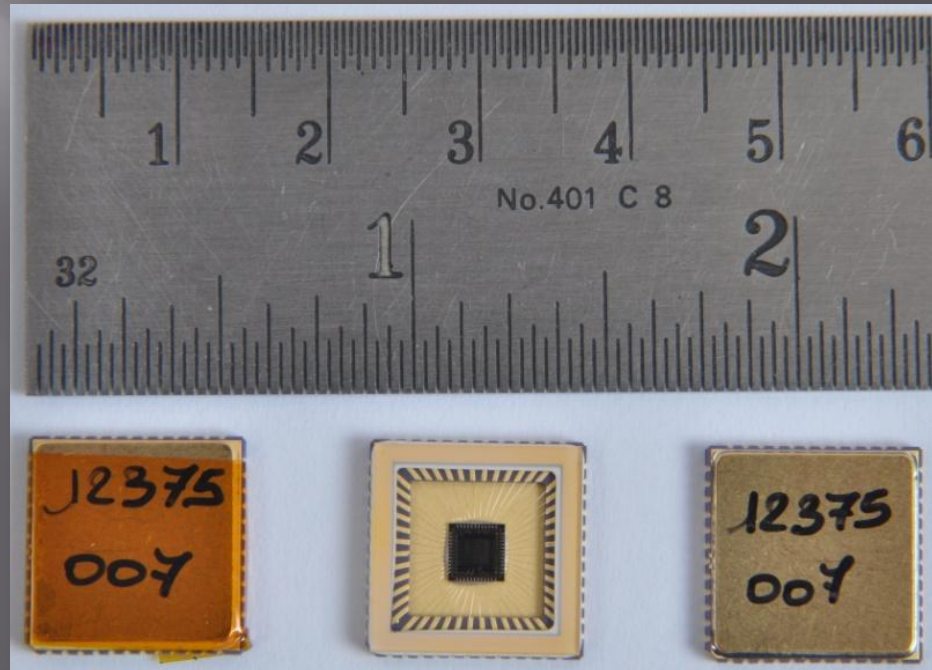
- ❖ 8, LVDS pairs of unshaped comparator signals (I)
- ❖ 1, amplified & multiplexed RPC pulse on 50Ω (I)
- ❖ 3-bit channel address bus for multiplexer (O)
- ❖ Power supplies (O)
- ❖ Threshold control (d.c. or DAC bus) (O)

Functional diagram of FE ASIC

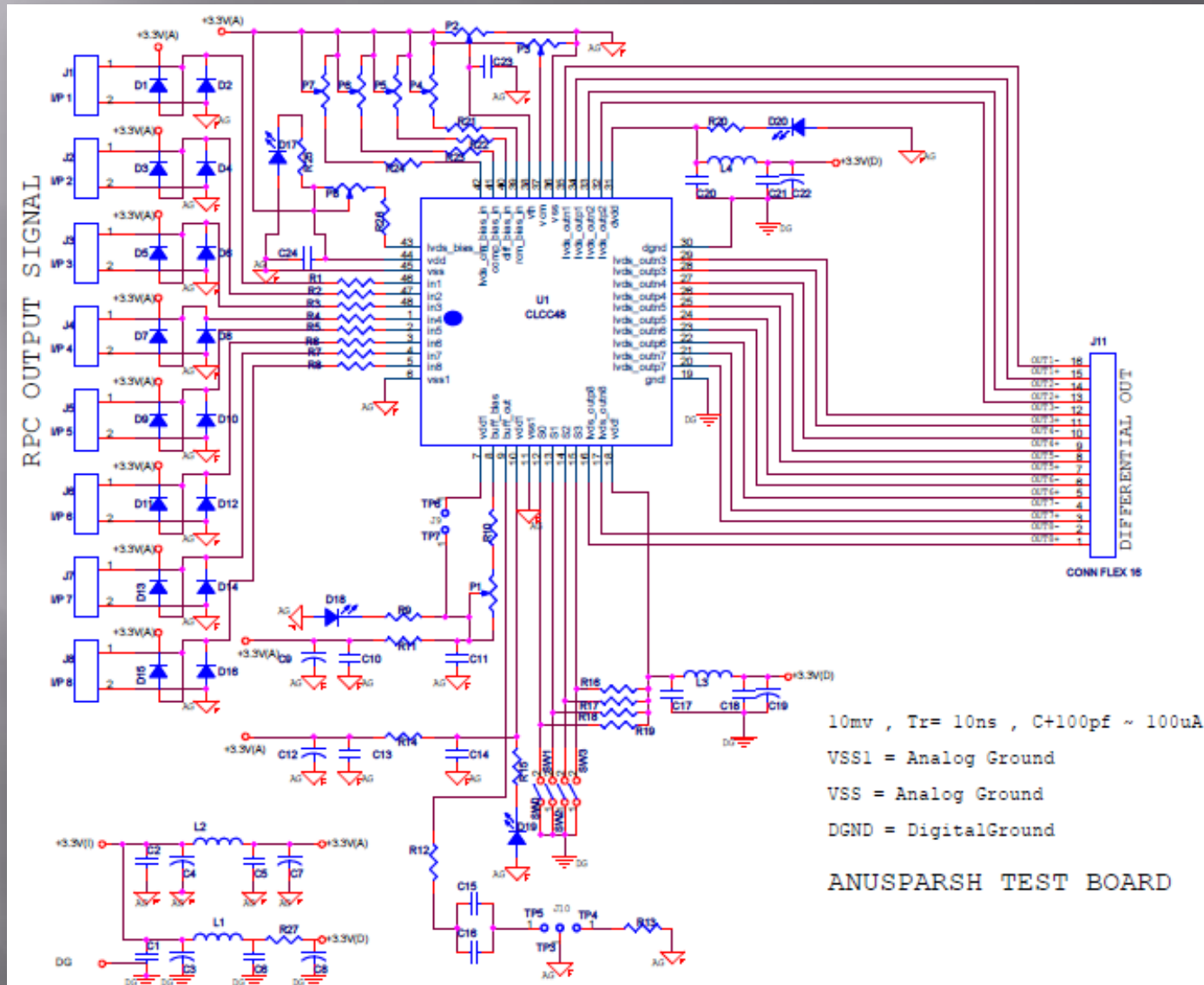


Features of ICAL FE ASIC

- ❖ IC Service: Europractice (MPW), Belgium
- ❖ Service agent: IMEC, Belgium
- ❖ Foundry: austriamicrosystems
- ❖ Process: AMSc35b4c3 (0.35 μ m CMOS)
- ❖ Input dynamic range: 18fC – 1.36pC
- ❖ Input impedance: 45 Ω @350MHz
- ❖ Amplifier gain: 8mV/ μ A
- ❖ 3-dB Bandwidth: 274MHz
- ❖ Rise time: 1.2ns
- ❖ Comparator's sensitivity: 2mV
- ❖ LVDS drive: 4mA
- ❖ Power per channel: < 20mW
- ❖ Package: CLCC48(48-pin)
- ❖ Chip area: 13mm²



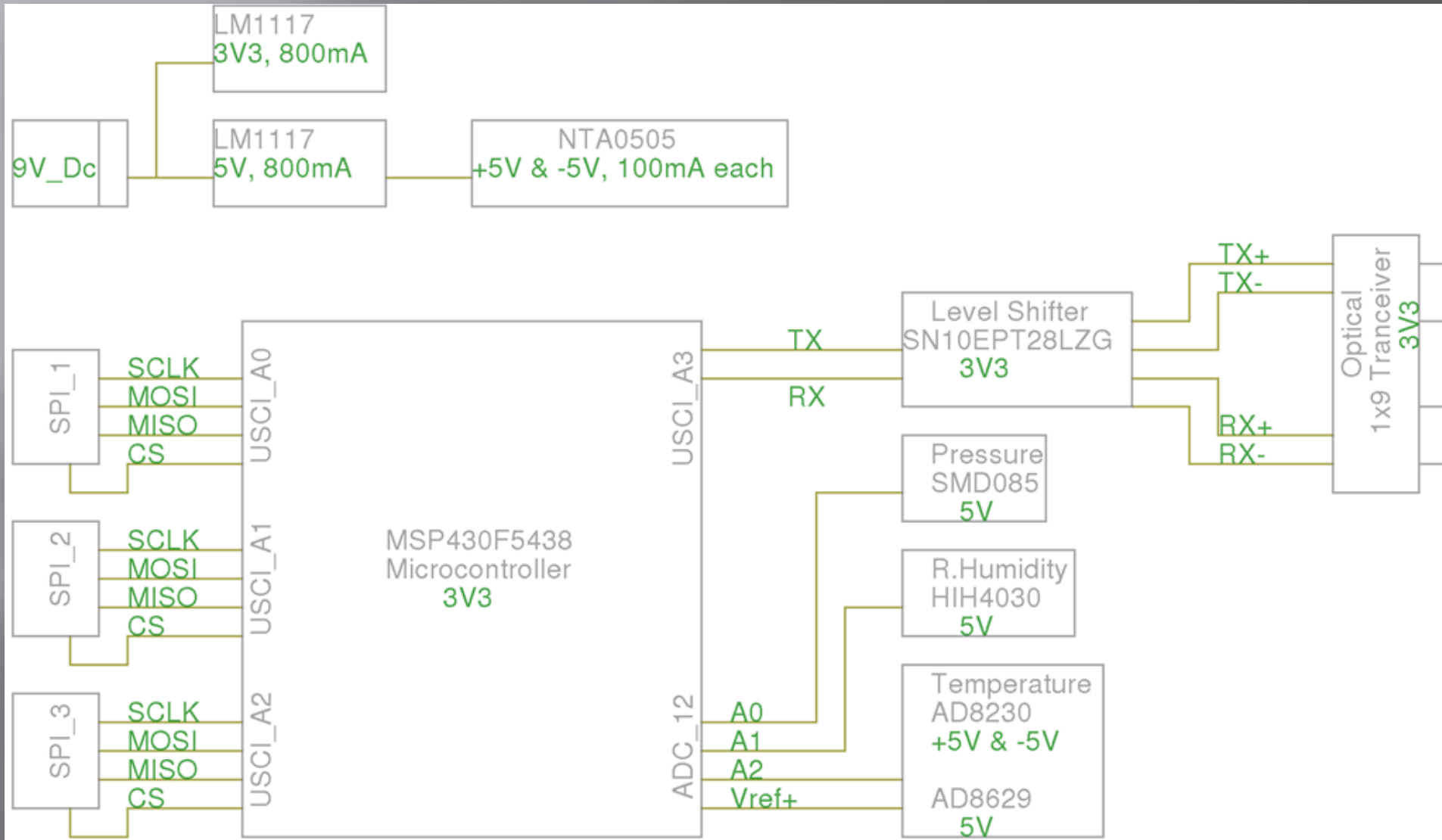
FE ASIC evaluation board



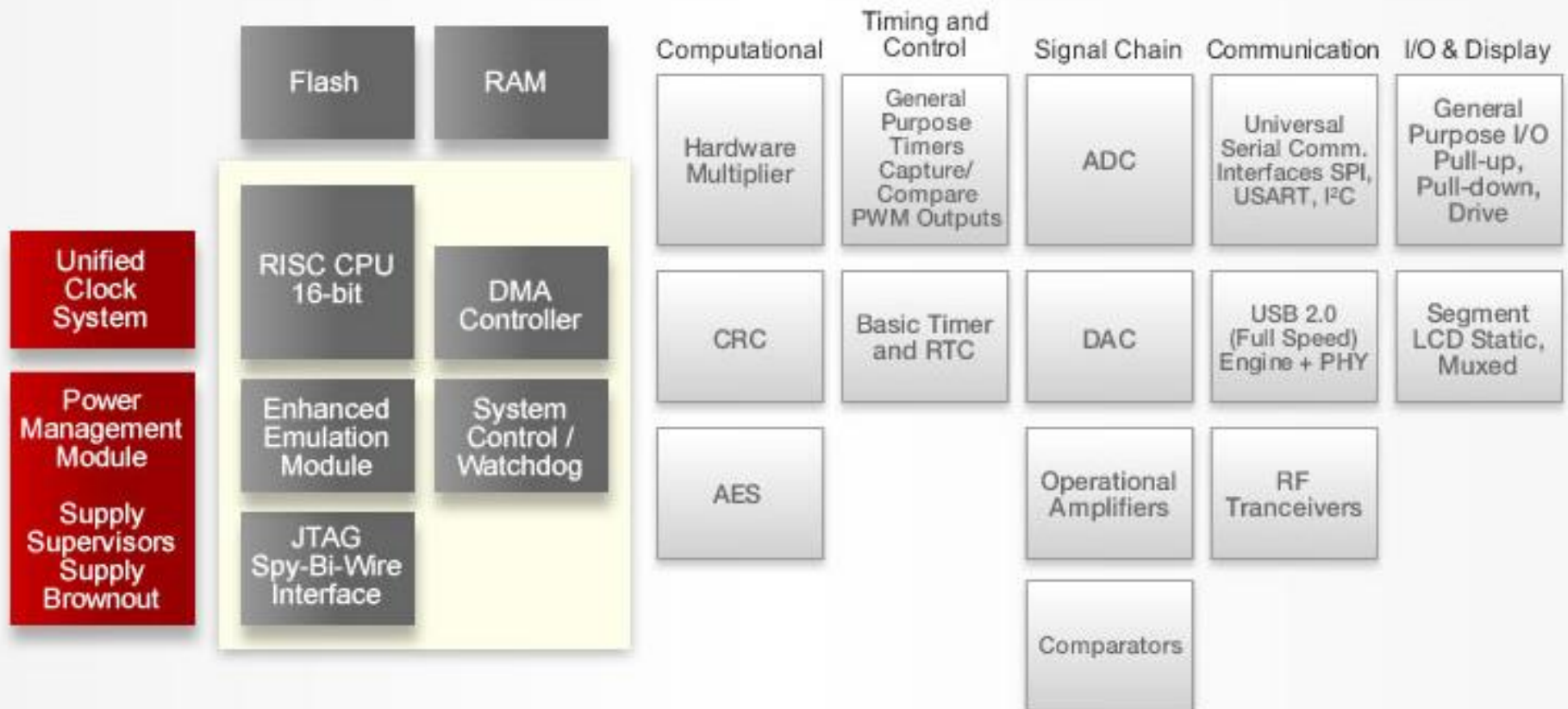
An important issue on FE ASIC

- ▣ Separate chips for amplifier and discriminator?
- ▣ Helps better to support FE for glass and bakelite versions of RPC
- ▣ Also helps trying out for example, different designs for comparator. For example: CFD
- ▣ Does not matter much for the FE board – it is matter of one versus two ASIC chips onboard.
- ▣ Alternative: Amplifier bypass option in the current ASIC (amp+comp) chip.
- ▣ Can we have analog sum of eight channels, in addition to multiplexing?

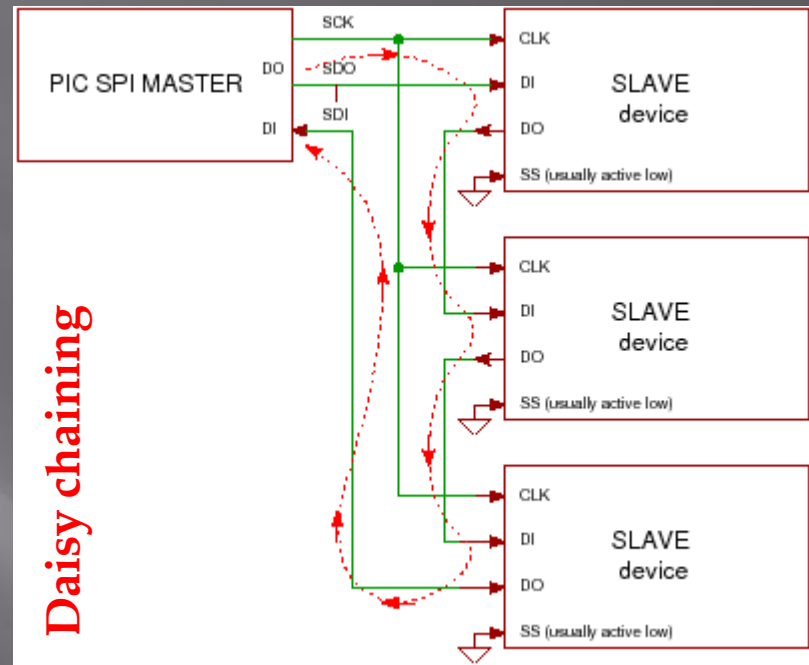
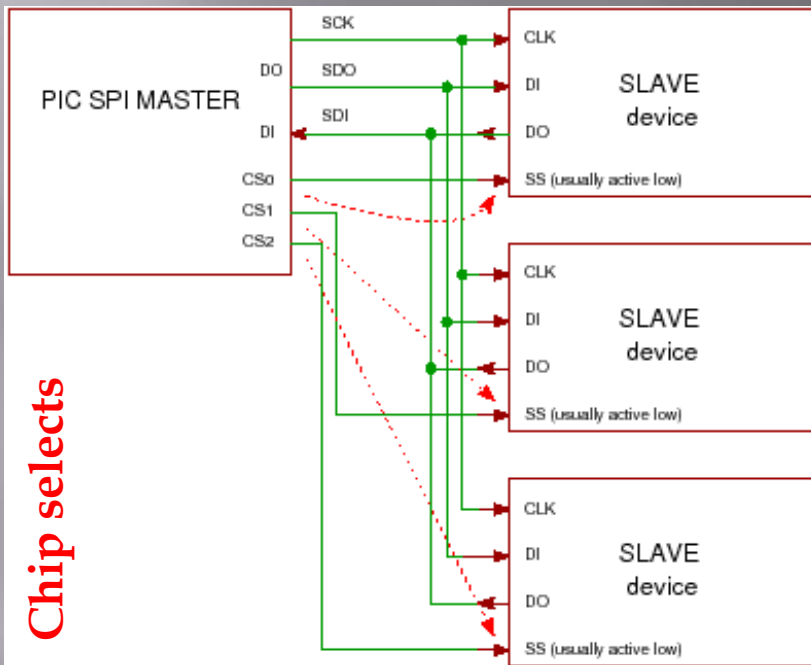
Scheme of RPC-DAQ controller



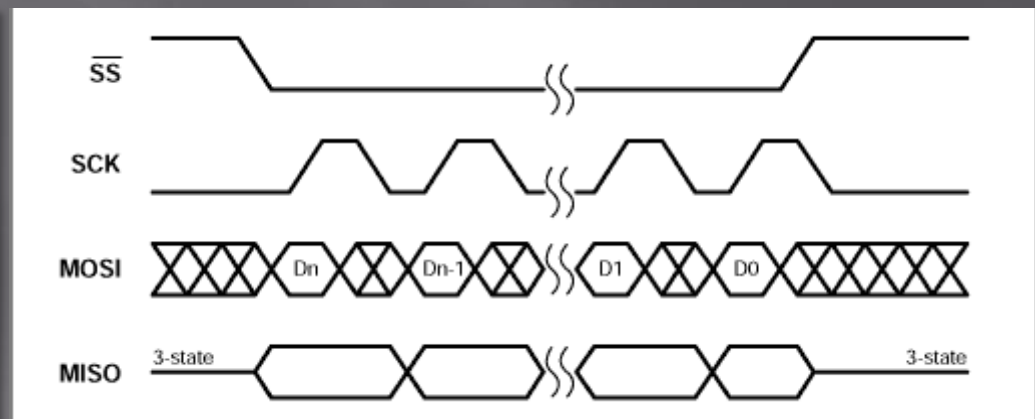
Block diagram of MSP430F5xx



Serial Peripheral Interface (SPI)

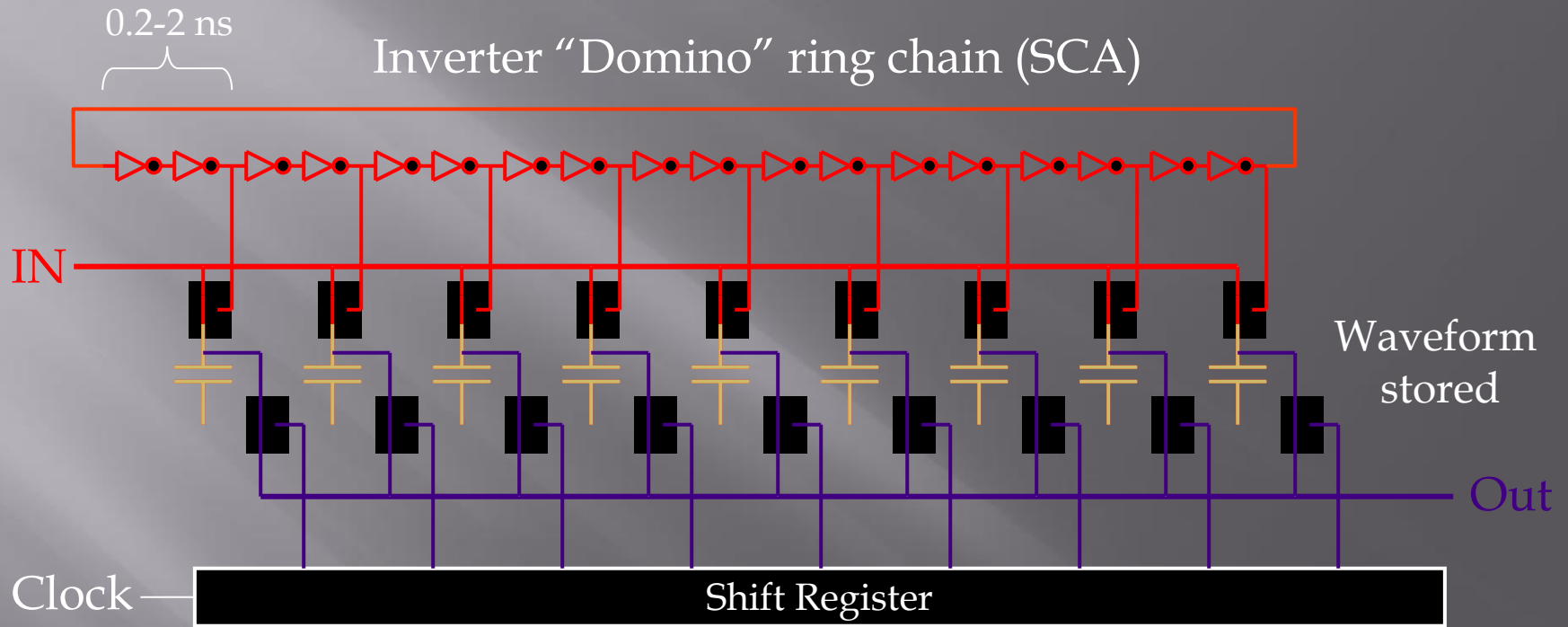


SPI Signals	Slave Data Input	MOSI
	Slave Data Output	MISO
	Chip Select Input	SS
	Master Clock Input	SCK



Pulse shape monitor

Stefan Ritt, Paul Scherrer Institute



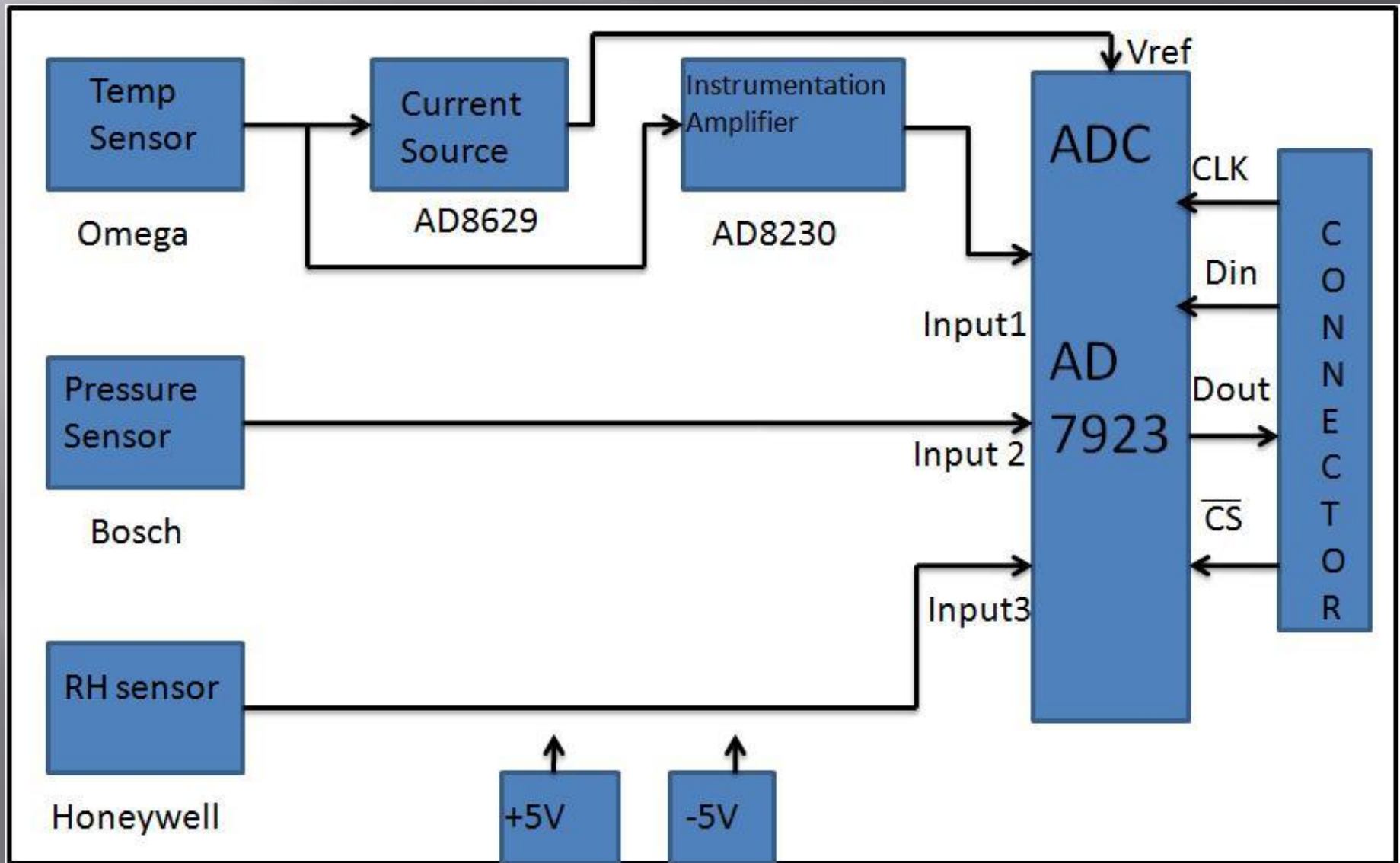
"Time stretcher" GHz \rightarrow MHz

Also *ANUSMRITI* ASIC: 500MHz Transient Waveform Sampler
V.B.Chandratre *et al* (BARC)

ICAL timing device

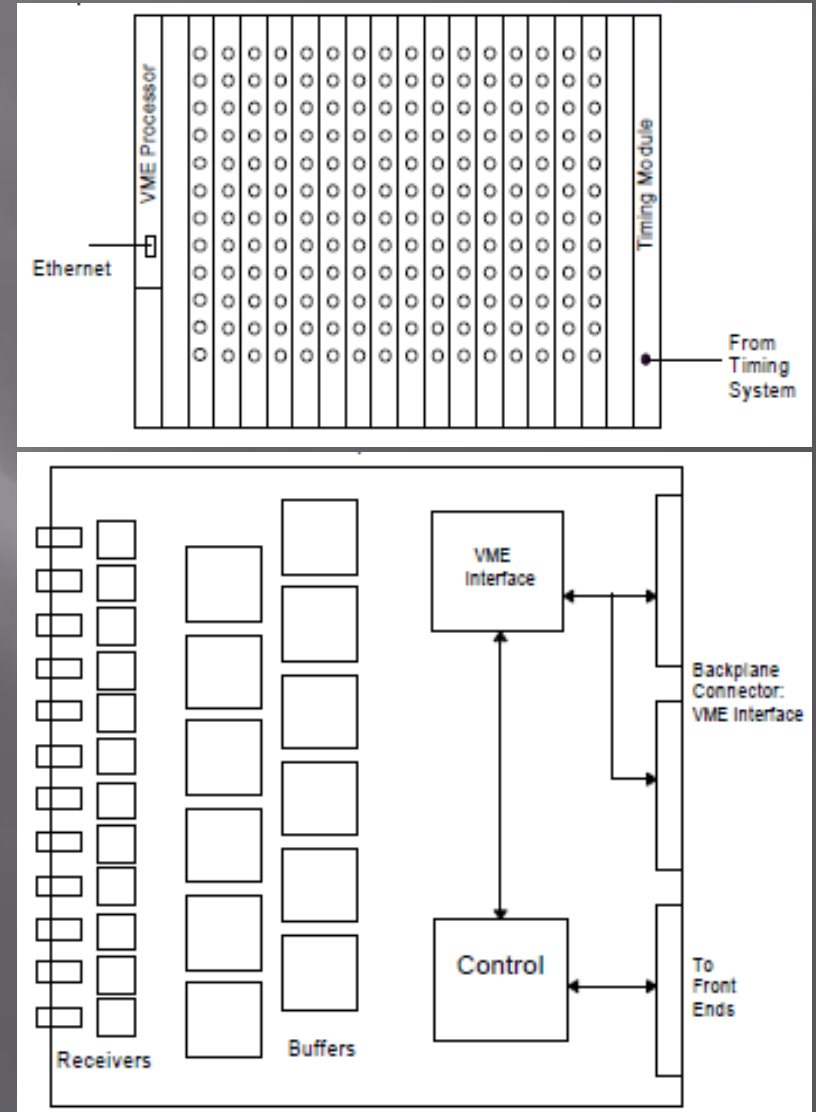
- ▣ ASIC (3-stage interpolation technique)
 - The new approach is to mix and match ASIC+FPGA techniques/architectures
- ▣ FPGA (Vernier technique)
- ▣ FPGA (Differential delay line technique)
 - The FPGA efforts will continue
 - Some issues (delay matching, routing etc.) to be solved
- ▣ Good and bad of an FPGA solution
- ▣ FPGA is a lesser travelled path (only used in CKM experiment, Fermilab)

TPH monitor module



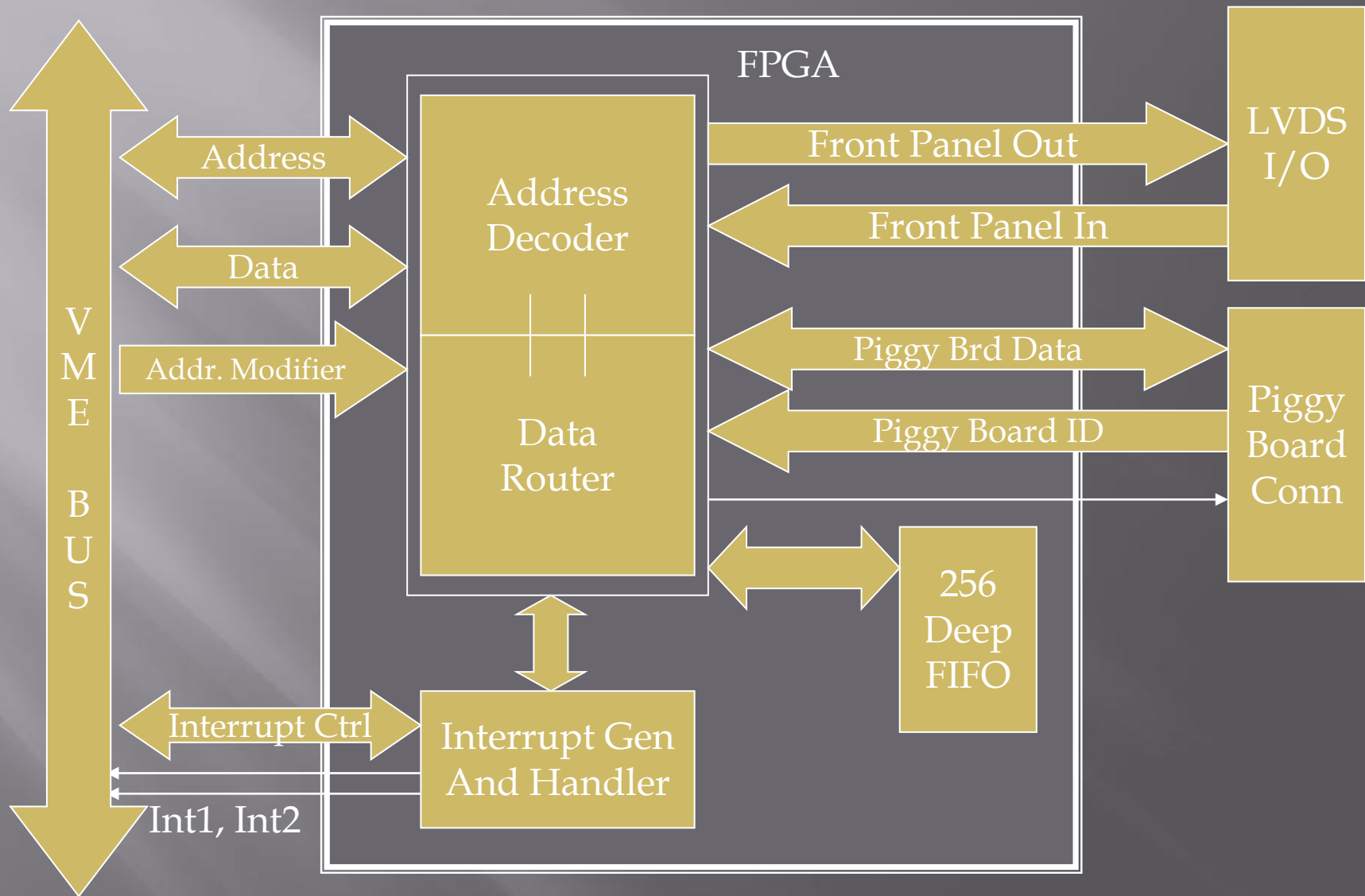
Back-end issues

- ▣ VME is the ICAL's backend standard
- ▣ Global services (trigger, clock etc.), calibration
- ▣ Data collector modules
- ▣ Computer and data archival
- ▣ On-line DAQ software
- ▣ On-line data quality monitors
- ▣ Networking and security issues
- ▣ Remote access protocols to detector sub-systems and data
- ▣ Voice and video communications

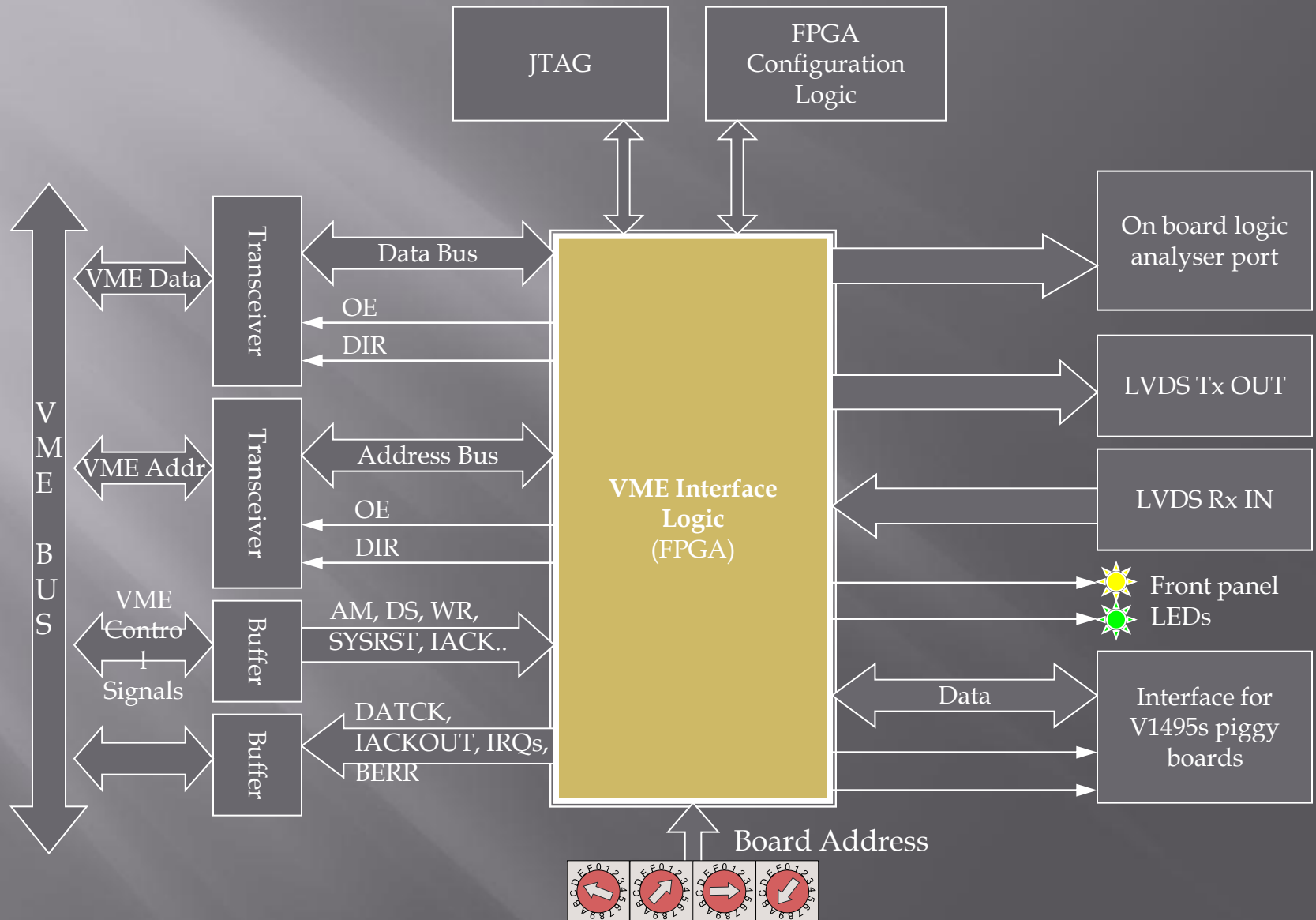


Drawings courtesy: Gary Drake

VME Interface Logic



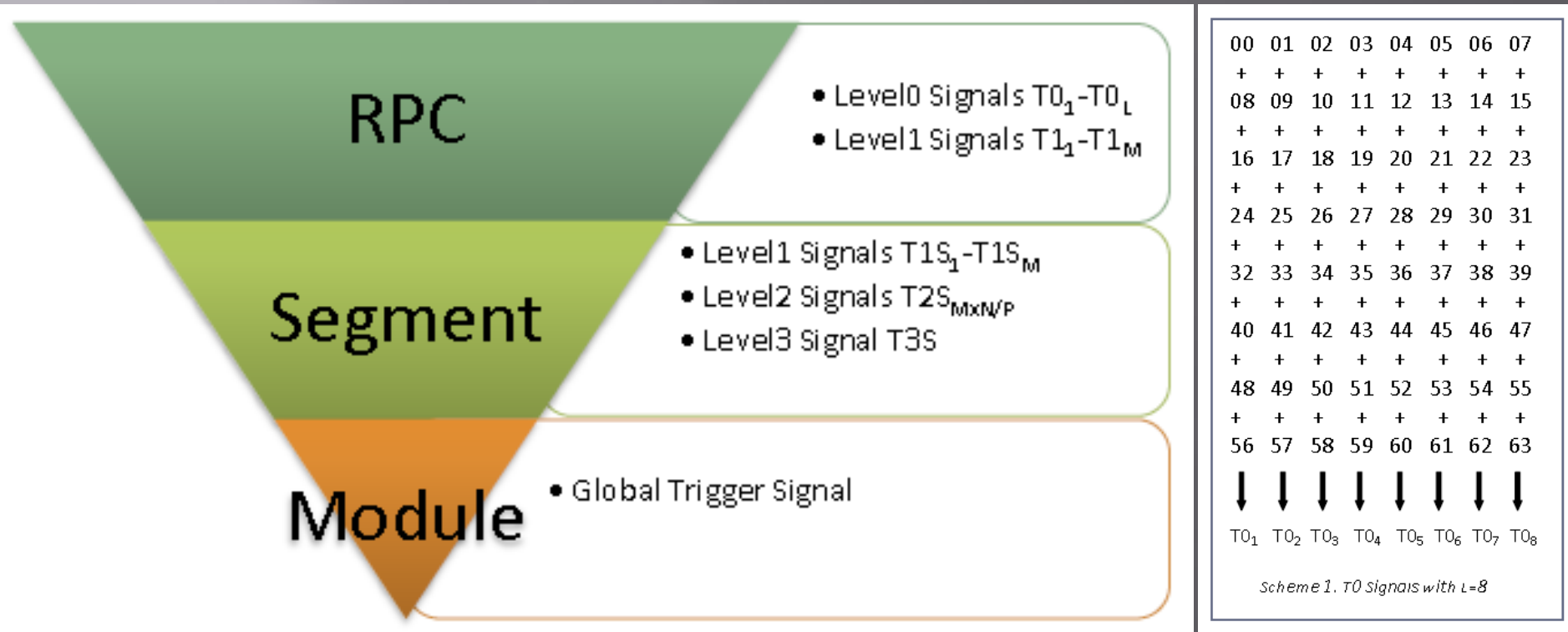
Custom VME Module



Features of ICAL trigger system

- ▣ *In situ* trigger generation
- ▣ Autonomous; shares data bus with readout system
- ▣ Distributed architecture
- ▣ For ICAL, trigger system is based only on topology of the event; no other measurement data is used
- ▣ Huge bank of combinatorial circuits
- ▣ Programmability is the game, FPGAs, ASICs are the players

Proposed trigger scheme - 1



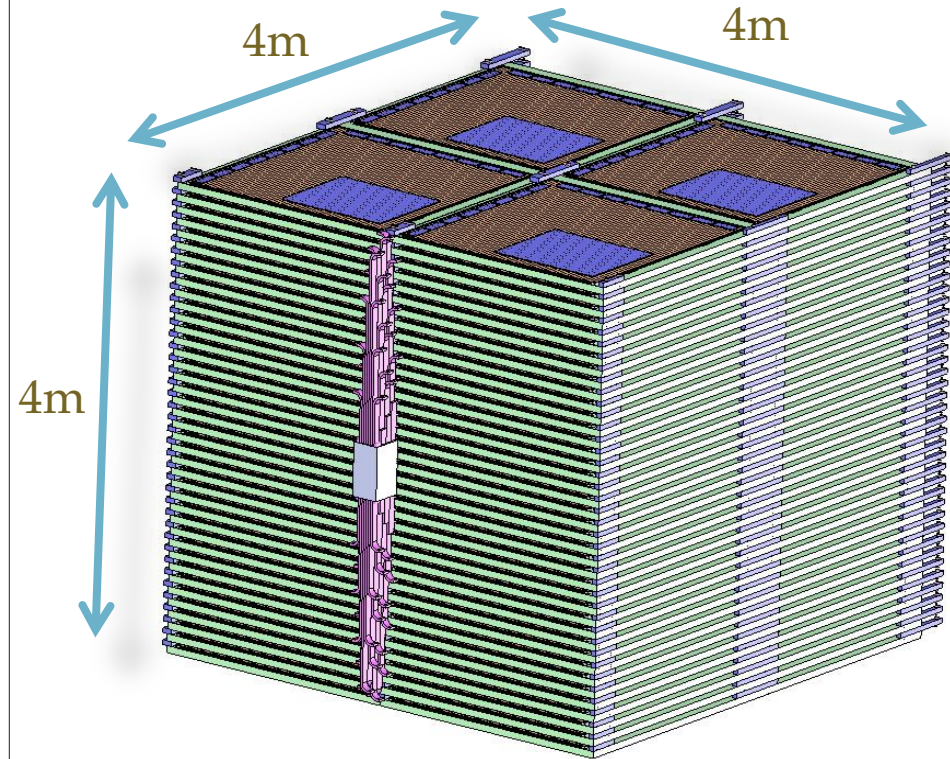
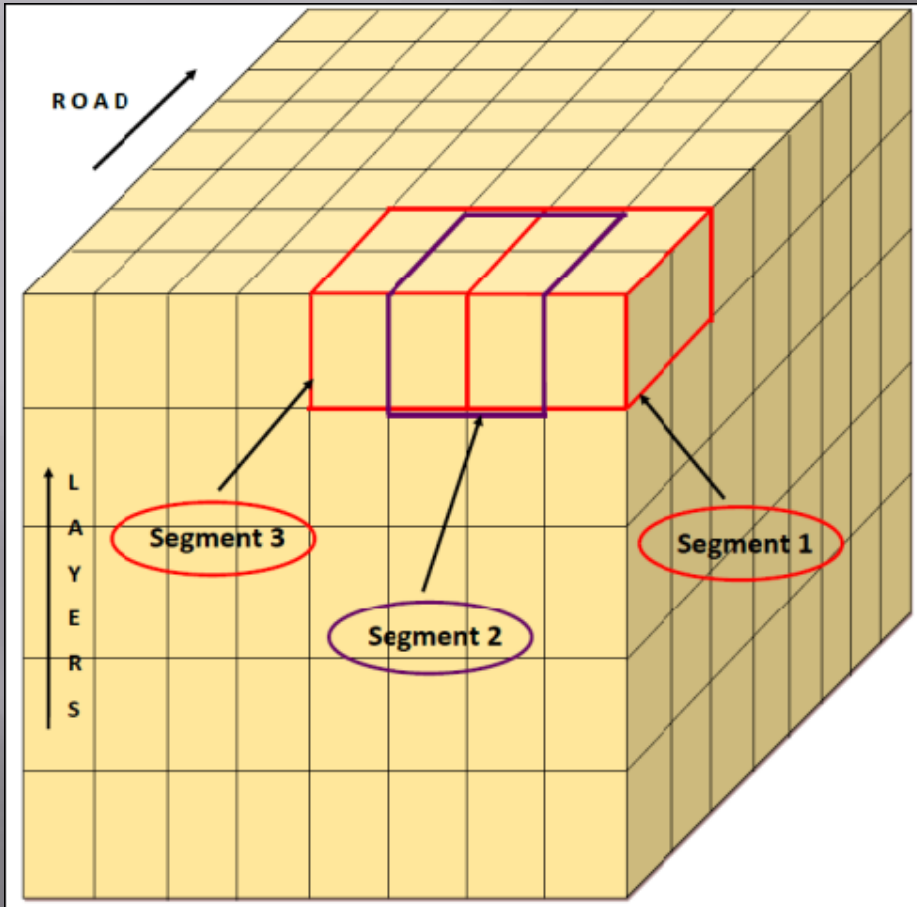
1-Fold : $T11 = T01 + T02 + \dots + T0L-1 + T0L$

2-Fold : $T12 = T01.T02 + T02.T03 + \dots + T0L-1.T0L + T0L.T01$

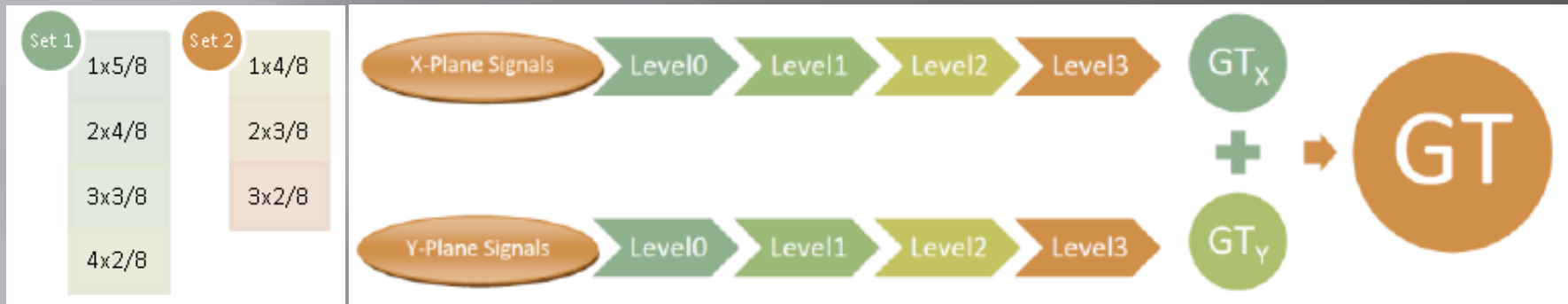
3-Fold : $T13 = T01.T02.T03 + T02.T03.T04 + \dots + T0L-1.T0L.T01 + T0L.T01.T02$

4-Fold : $T14 = T01.T02.T03.T04 + T02.T03.T04.T05 + \dots + T0L-1.T0L.T01.T02 + T0L.T01.T02.T03$

Segmentation of ICAL



Proposed trigger scheme - 2



Hspread	Vspread	Segment Size	Segment Type	T2S _{1,4/8} Rate (Hz)	T2S _{2,4/8} Rate (Hz)	T2S _{3,4/8} Rate (Hz)	T2S _{4,8} Rate (Hz)	T3S Rate (Hz)
4 (2x2)	10	4mx4mx1m	A	0.30	1.20×10^{-12}	7.61×10^{-13}	2.35×10^{-16}	0.30
			B	0.09	3.61×10^{-15}	2.28×10^{-13}	7.05×10^{-17}	0.09
	20	4mx4mx2m	A	0.60	2.41×10^{-12}	1.52×10^{-17}	4.70×10^{-16}	0.60
			B	0.09	3.61×10^{-15}	2.28×10^{-13}	7.05×10^{-17}	0.09
9 (3x3)	40	4mx4mx4m	A	1.20	4.81×10^{-12}	3.04×10^{-17}	9.40×10^{-16}	1.20
			B	0.69	2.77×10^{-12}	1.75×10^{-17}	5.40×10^{-16}	0.69
	30	6mx6mx3m	A	52.01	9.25×10^{-11}	2.60×10^{-16}	3.57×10^{-15}	52.01
			B	39.88	7.09×10^{-11}	1.99×10^{-16}	2.73×10^{-15}	39.88
16 (4x4)	40	6mx6mx4m	A	69.35	1.23×10^{-10}	3.47×10^{-16}	4.76×10^{-15}	69.35
			B	39.88	7.09×10^{-11}	1.99×10^{-16}	2.73×10^{-15}	39.88
	60	6mx6mx6m	A	104.02	1.85×10^{-10}	5.20×10^{-16}	7.13×10^{-15}	104.02
			B	39.88	7.09×10^{-11}	1.99×10^{-16}	2.73×10^{-15}	39.88
	40	8mx8mx4m	A	1.23×10^5	1.23×10^{-9}	1.95×10^{-13}	1.50×10^{-14}	1.23×10^5
			B	708.09	7.08×10^{-10}	1.12×10^{-13}	8.64×10^{-15}	708.09
	60	8mx8mx6m	A	1.85×10^5	1.85×10^{-9}	2.92×10^{-13}	2.25×10^{-14}	1.85×10^5
			B	708.09	7.08×10^{-10}	1.12×10^{-13}	8.64×10^{-15}	708.09
	80	8mx8mx8m	A	2.46×10^5	2.46×10^{-9}	3.90×10^{-13}	3.01×10^{-14}	2.46×10^5
			B	1.94×10^5	1.94×10^{-9}	3.07×10^{-13}	2.37×10^{-14}	1.94×10^5

Power supplies

- ▣ High voltage for RPCs
 - Voltage: 10kV (nominal for Glass, less for Bakelite)
 - Current: 15mA (approx., 500nA per chamber)
 - Ramp up/down, on/off, monitoring
- ▣ Low voltage for electronics
 - Voltages and current budgets still not available
- ▣ Commercial and/or semi-commercial solutions
 - Buy supplies, design distribution(and control)?
- ▣ DC-DC and DC-HVDC converters; cost considerations

DC-HVDC converters

1. E101CT, lowest cost

- Input = +15VDC
- Dual output is +5KV / -5KV (with a full load)
- Output current = 0.2mA
- Outputs are not separately controlled, but will track each other.
- E-Series Data Sheet - <http://www.emcohighvoltage.com/pdfs/eseries.pdf>

2. G50 [x 2units], low cost, separate control

- Input = +12VDC
- Output is 5KV, positive or negative (with a full load)
- Output current is 0.3mA
- Two units would be configured for a positive and negative output pair.
- Units can be controlled separately.
- G-Series Data Sheet - <http://www.emcohighvoltage.com/pdfs/gseries.pdf>

3. Custom solution, Q101 with a centre tap, miniature package

- Input = +5VDC (can be 12VDC)
- Dual output is +5KV / -5KV (with a full load)
- Output current = 50uA
- Outputs are not separately controlled, but will track each other.
- Note: This is a custom solution

4. Q60-5, Q60N-5, 2 units together, miniature package, separate control

- Input = +5VDC
- Output is +6KV / -6KV (with a full load)
- Output current is 0.1mA
- Two units would be configured for a positive and negative output pair.
- Units can be controlled separately.
- Q-Series Data Sheet - <http://www.emcohighvoltage.com/pdfs/qseries.pdf>

Cables and interconnects

- ▣ RPC to front-end boards – *the toughest!*
 - Integration with pickup panel fabrication
- ▣ Front-end boards to RPC-DAQ board
 - LVDS signals (any alternatives?, prefer differential)
 - Channel address
 - Multiplexed analog pulse
 - Power supplies
- ▣ RPC-DAQ boards to trigger segment stations
 - Four pairs, Copper, multi-line, flat cable?
- ▣ RPC-DAQ boards to back-end
 - Master trigger
 - Central clock
 - Data cable (Ethernet: copper/fibre, ...)

Other critical issues

- ▣ Power requirement and thermal management
 - If 50mW/channel → 200KW/detector
 - Front-end positioning; use absorber to good use!
 - Do we need forced, water cooled ventilation?
 - UPS, generator power requirements
 - ▣ High voltage supplies, critical controls, computers on UPS
- ▣ Suggested cavern conditions
 - Temperature: $20 \pm 2^\circ\text{C}$
 - Relative humidity: $50 \pm 5\%$

Roll of electronics industries

- ▣ Chip fabrication
- ▣ Board design, fabrication, assembly and testing
- ▣ Cabling and interconnects
- ▣ Crates and mechanics
- ▣ Slow control and monitoring
 - Control and monitoring systems for gas systems and magnet
- ▣ Industries (both public and private) are looking forward to work with INO

Software components

- ▣ RPC-DAQ controller firmware
- ▣ Backend online DAQ system
- ▣ Local and remote shift consoles
- ▣ Data packing and archival
- ▣ Event and monitor display panels
- ▣ Event data quality monitors
- ▣ Slow control and monitor consoles
- ▣ Database standards
- ▣ Plotting and analysis software standards
- ▣ OS and development platforms

Proof of principle effort

- ▣ Can be tested today on the RPC stacks
- ▣ Front-end board with the current board's form-factor, but using ASICs
- ▣ RPC-DAQ board with:
 - TDC
 - Waveform sampler
 - Strip-hit latch and rate monitor
 - Controller + data transceiver
 - Firmware for the above
 - Pre-trigger front-end
 - TPH monitoring
 - Pulse width monitoring
 - Front-end control
 - Signal buffering scheme
 - and GP area or ports for accommodating new blocks
- ▣ VME data concentrator module
- ▣ Result: Complete readout chain is tested
- ▣ Can we use this for RPC QC test stands or what?

Work packages – Part 1

- ▣ Developing thin signal pickup panels
- ▣ RPC to front-end interconnect scheme
- ▣ Front-end
 - ASIC (including two separate ASICs' option), *freeze design*
 - Board design
- ▣ RPC-DAQ module design (+ signal routing/buffering)
 - TDC chip, *freeze design*
 - Waveform sampler chip, *freeze design*
 - Strip-hit latch and rate monitor (similar to prototype's design)
 - Pre-trigger front-end (similar to prototype's design)
 - Controller + data transreceiver (including firmware development)
 - TPH monitoring section (done?)
 - Front-end control scheme (threshold, test inputs)

Work packages – Part 2

- ▣ Trigger system
 - Validation of the scheme
 - Segment trigger station design (do we need a crate?)
 - Locating segment trigger stations and routing of pre-trigger lines
 - Locating backend trigger station, trigger fan-out and routing
 - Global clock? Depends on TDC scheme
- ▣ DAQ backend
 - VME data concentrator module (Readout for 64 RPCs?)
 - VME crate controller
 - Location of backend VME crates, crates production
 - On R&D track: Alternate backend standard PCI/PCIe etc?
- ▣ Proof of principle effort

Work packages – Part 3

- ▣ DAQ software
 - Databases
 - Standardising OS, development tools, graphical tools
 - Data acquisition, packaging, archival, event display, DQMs, monitor controls, user interfaces etc.
- ▣ Power supplies
 - Low Voltage
 - High Voltage (commercial, DC-HVDC, semi-commercial)
 - Power supplies' mains and distribution
 - Routing of LV, HV lines to the RPC
 - Routing of LV, HV on the magnet
- ▣ Power requirement and thermal management
 - Simulations of heat dissipation
 - Ventilation methods

Work packages – Part 4

- ▣ Integration issues
 - Mounting of front-ends and RPC-DAQ module on the RPC unit
 - Alternate schemes
- ▣ Production jobs
 - Boards and modules design
 - Production, programming and calibration
 - Cabling and connectorisation etc. (specifications decided by the collaboration)
 - Crates, racks and other mechanics
- ▣ Installation and commissioning
- ▣ Operation and long-term continuity considerations

Thanks

- ▣ Prof. Satyajit Saha & Dr. Subhasis Chattopadhyay for all the local arrangements despite prevailing election season
- ▣ Dr. Deepak Samuel for designing the meeting's web page
- ▣ Prof. N.K.Mondal for approving all the expenses
- ▣ MOM writers, Deepak and Mandar Saraf
- ▣ All of you who could make it despite disruption of AI services