Data Acquisition Systems

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Outline

- Introduction
- Basics of RPC signal formation
- Recordable parameters
- Front-end circuit design issues
- DAQ system for ICAL prototype
- DAQ schemes for INO detector
- Course module summary
- Acknowledgements & References

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General requirements of DAQ system

- Preserve detector signal characteristics
- Improve signal-to-noise
- Pulse shaping
- Flag interesting events (Trigger)
- Trigger threshold level considerations
- Physicist driven configurations
- Record all observables
- Play back on-line a sample of events
- Automatic (or manual) monitor and control of crucial experimental parameters

General characteristics of DAQ system

- Modular
- Segmented; divide-and-conquer
- Scalable and upgradable
- On-site and/or on-line configurable
- Reliable (Ambient parameters, RF etc)
- Deployment of state-of-the-art technologies
- Long gestation periods of current experiments
- Simple operational procedures
- Fault tolerant; redundant paths
- Low power requirement

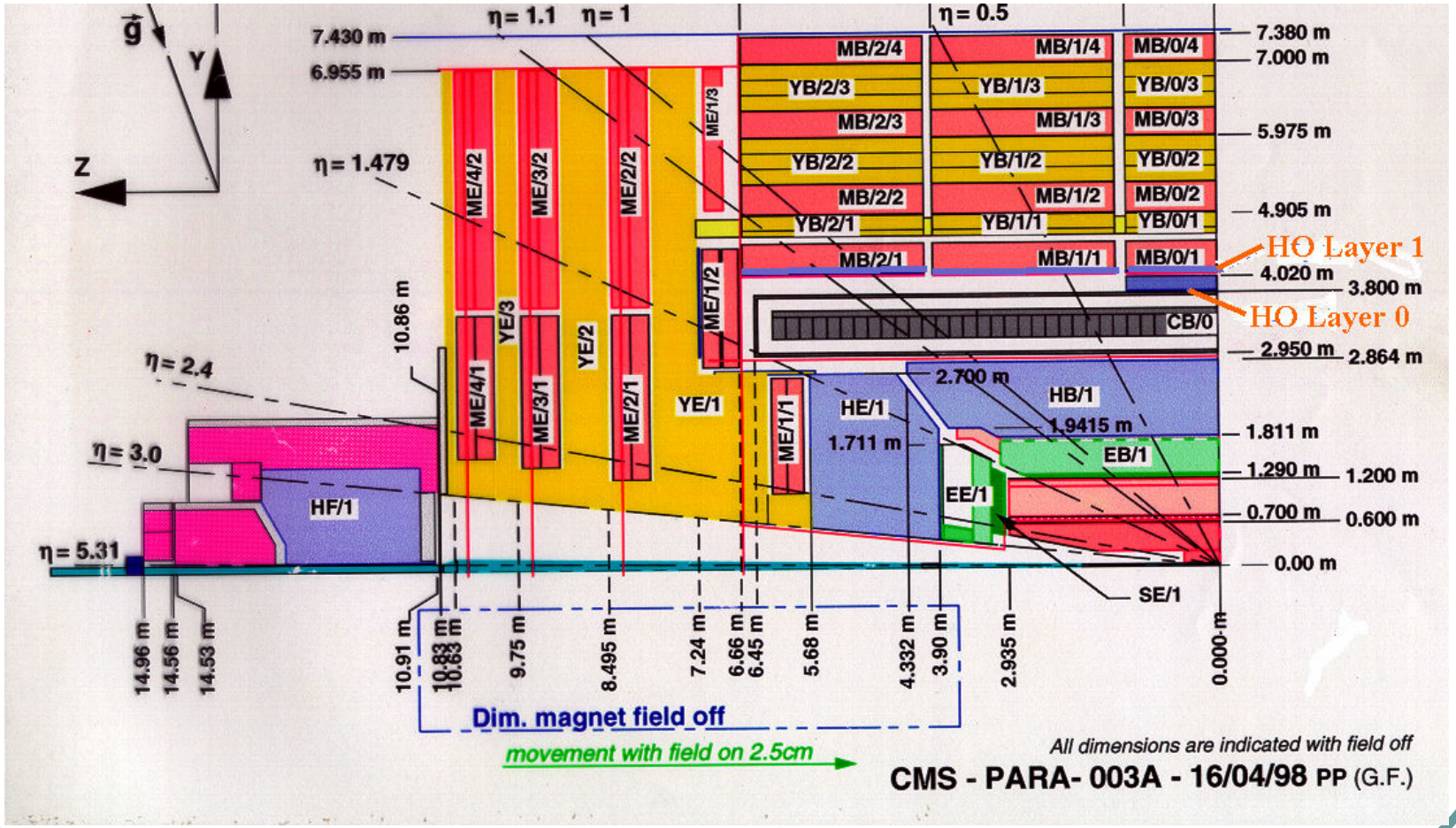
Example of a vintage DAQ system!

DAQ system for KGF underground Proton decay experiments

What is specific for ICAL DAQ

- Large number of data channels to handle; large scale integration
- But, fewer and simpler parameters to record
- Monolithic detector; compare with accelerator based experiments

CMS detector



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RPC signal generation

- A passing ionising particle will liberate N_0 electrons, creating an initial current, $i_0=eN_0v/g$, that depends on the electron's drift velocity v and on the width g of the gas gap.
- The gas avalanche process will immediately amplify the initial current in time as $i=i_0e^{st}h(t)$, where s is a real positive parameter and $h(t)$ the unit step function.
- The exponential multiplication factor may reach very large value, up to 10^8. The output voltage signal is given by $v(t)=i_0Z(s)e^{st}$

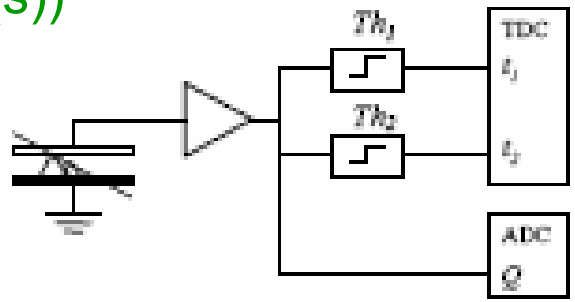
RPC signal characteristics

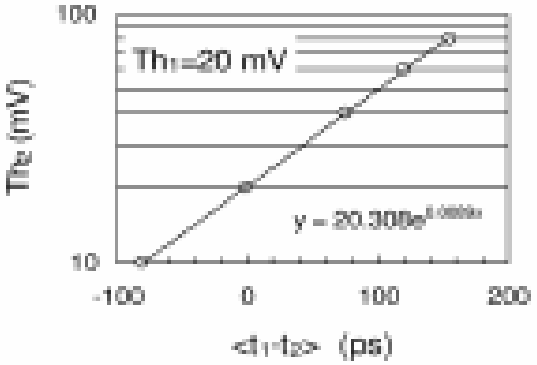
$$Th_1 \equiv v_0(s)\exp(st_1)$$

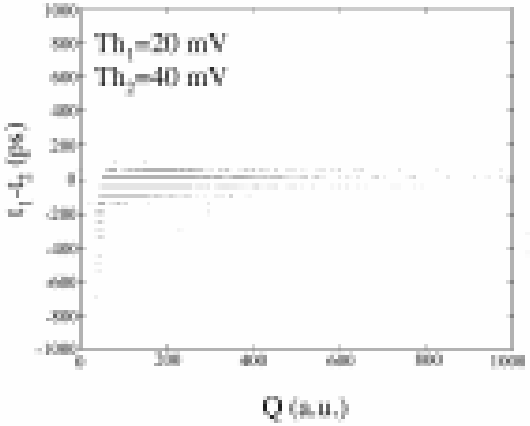
$$Th_2 \equiv v_0(s)\exp(st_2)$$

$$\ln(Th_1 / Th_2) \equiv s(t_1 - t_2)$$

For a given threshold setting, time deference should be independent of i_0 (which fluctuates event by event) and independent of the circuit properties (represented by Z(s))







Important conclusions

- The nature of the detector electrodes, coupling lines, amplifiers, etc, will affect only the magnitude of the output signal through the combined transimpedance *Z(s)*, while leaving unaffected the time development of the signal.

- The signal shape (exponential) will be influenced only by the value of *s*, determined by the gas avalanche process in the detector.

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Recordable parameters (Detectors)

- Event data
  - Strip hit information (1 bit per strip)
  - Strip/RPC signal timing with reference to event trigger
- Monitor data
  - Strip single counting rate
  - Chamber voltage and current

Recordable parameters (DAQ)

- Preamplifier gain and input offset
- Discriminator threshold and pulse width
- Trigger logic parameters and tables
- DAQ system parameters
- Controllers and computers' status

Recordable parameters (Gas system)

- Open loop versus closed loop systems
- Gas flow via Mass Flow Controllers
- Exhaust gas flow monitor
- Residual gas analyser data
- Gas contaminants' monitor data
- Gas leak detectors
- Safety bubblers' status

Recordable parameters (Ambient)

- Temperature
  - Gas
  - Front-end electronics
- Barometric pressure
  - Gas
- Relative humidity
  - Dark currents of the bias supplies
  - Electronics

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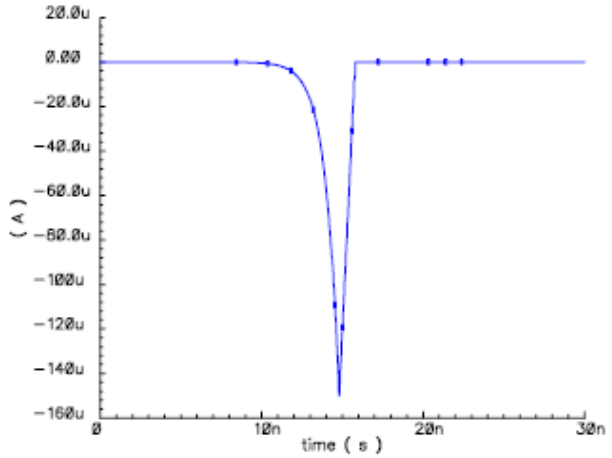
RPC signal characteristics

Shape of the signal: $I(t) = I_0 \exp(t/\tau)$ $(0 \le t \le 15\ ns)$

$\tau = 1/\eta v$ (~ 0.8 ns, at detector working point)



Strip line 1.3 m long and 2 - 4 cm wide:

$15\ \Omega \le R_0 \le 40\ \Omega$

$160\ pF \le C_{strip} \le 350\ pF$

Propagation delay ~ 5.5 ns/m

- **Input dynamic range:** $20\ fC \le Q_{in} \le 20\ pC$

Typical front-end circuit

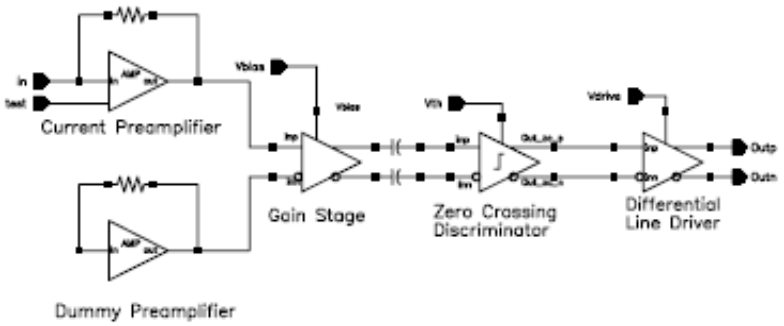
Technology: **0.8 μm BiCMOS of AMS (supported by multiprojects)**

8 channels, **each one made of:**

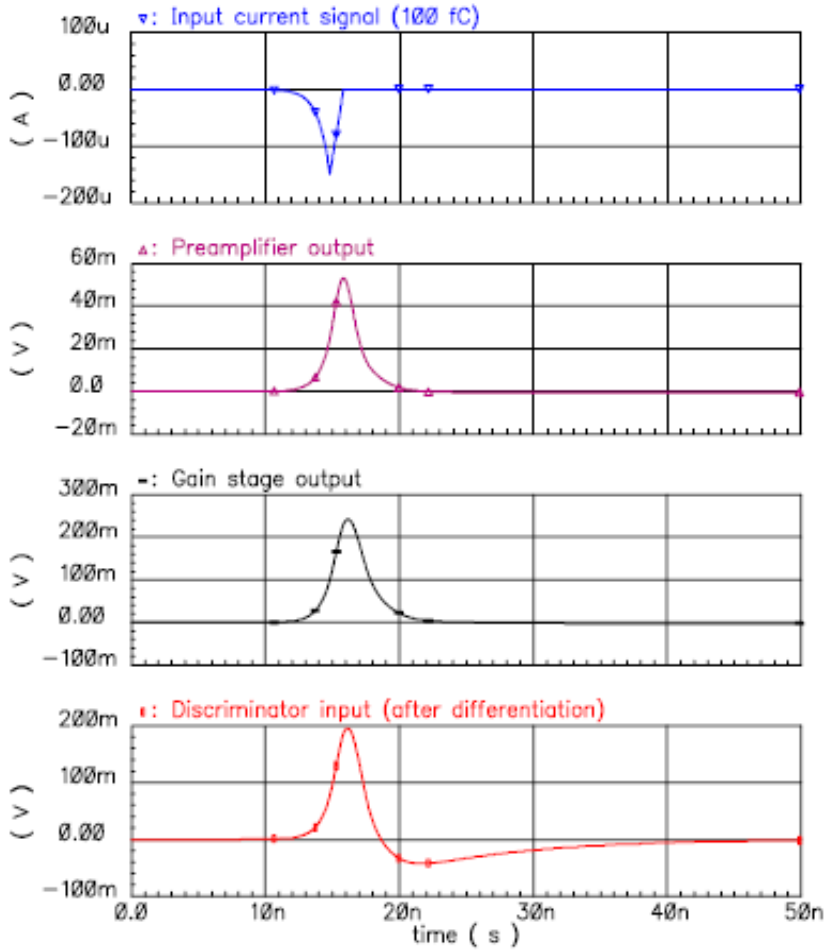
- **amplifier**
- **zero-crossing discriminator**
- **one-shot**
- **differential line driver.**

Power supplies: +5 V; GND

Power consumption: ~ 40 mW/channel



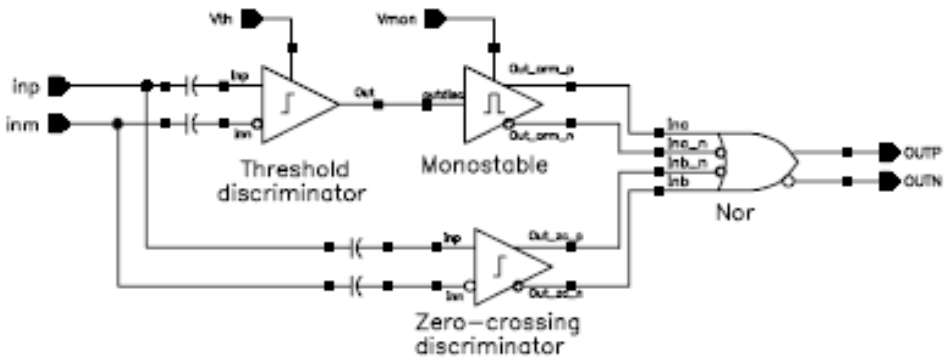
Various signal profiles



Zero-crossing discriminator

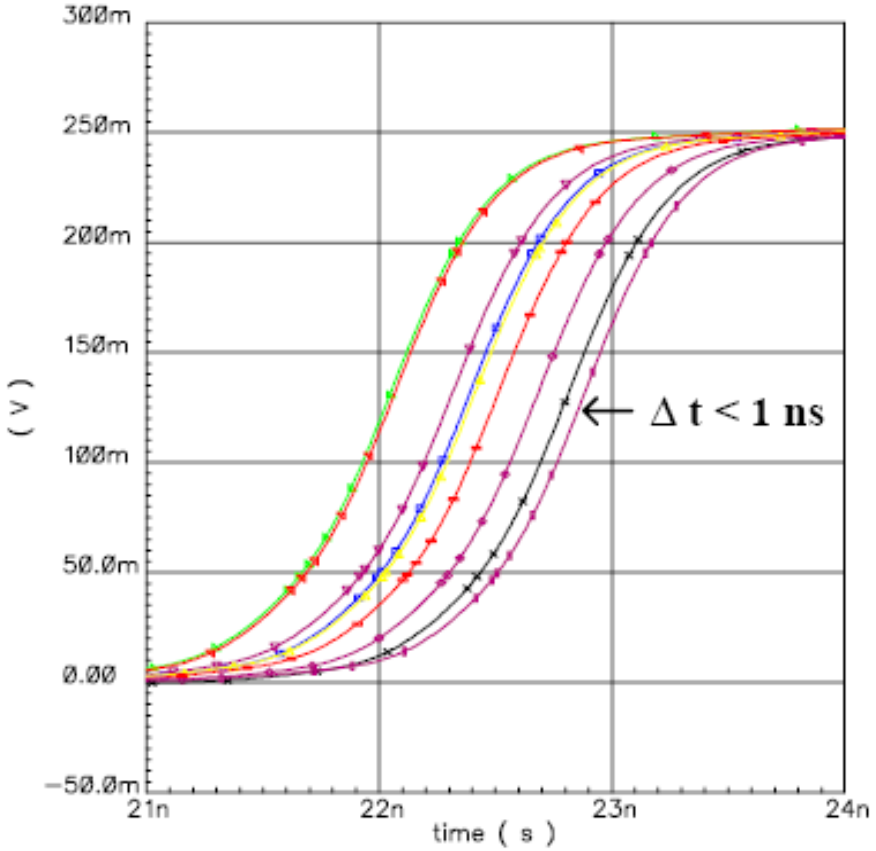
- **Threshold discriminator**
- **Monostable (One-shot)**
- **Zero-crossing discriminator**
- **NOR**

- **AC-coupling with amplifier (RC ~ 3 ns)**
- **50 ns ≤ T_{width} ≤ 400 ns**
- **Dead time ~ T_{width} + 10 ns**
- **f_{max} = 13 MHz (Qin = 2 pC)**
- **Power consumption: ~ 8 mW**

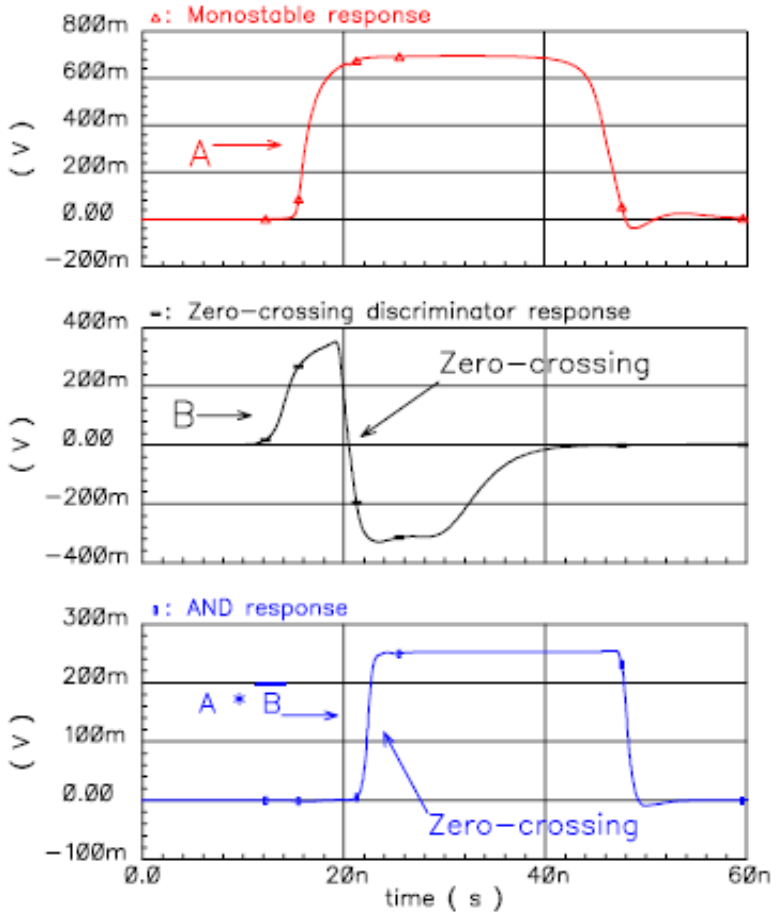


Discriminator response (Overdrive)

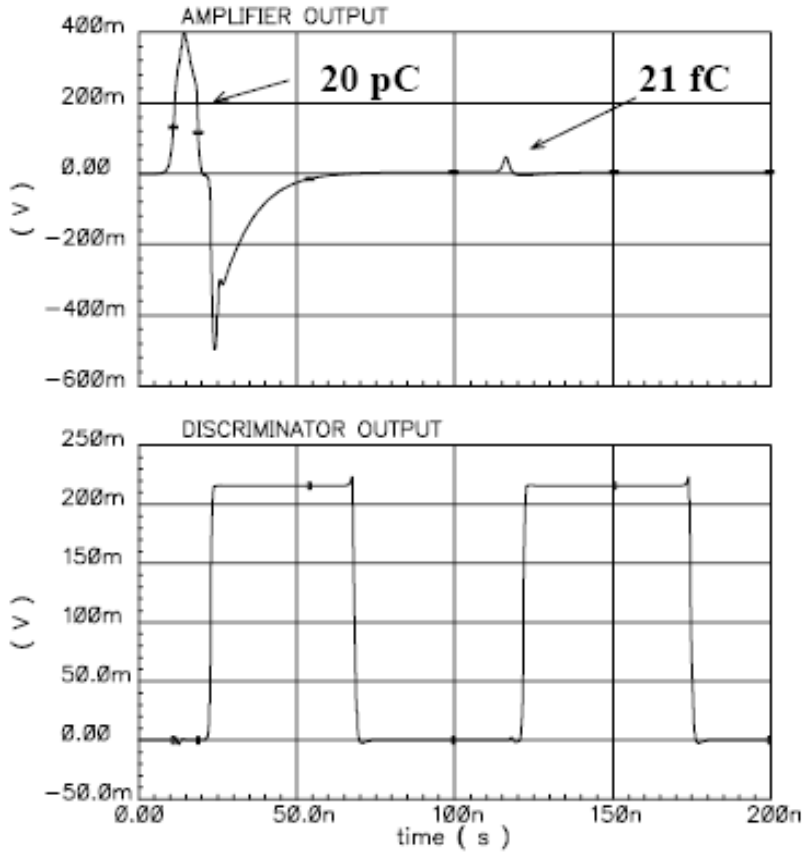
$1\ fC < Q_{ov} < 20\ pC$



Discriminator response



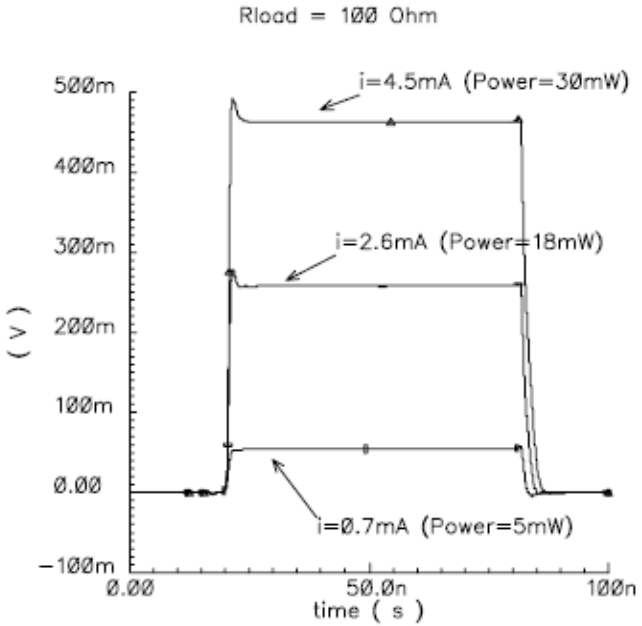
Double pulse resolution



Dead time (worst case) ~ 100 ns

Output driver

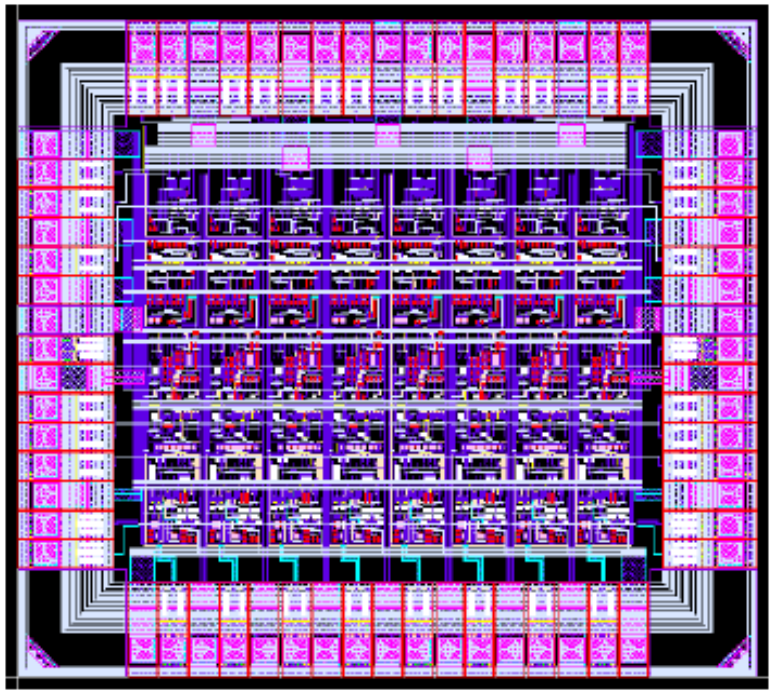
- 110 Ω twisted pair cable
- LVDS receiver, 250 mV minimum signal
- Power consumption (typical): ~ 16 mW.



Output driver response

The output current is externally tunable and the power could be reduced down to 5 mW

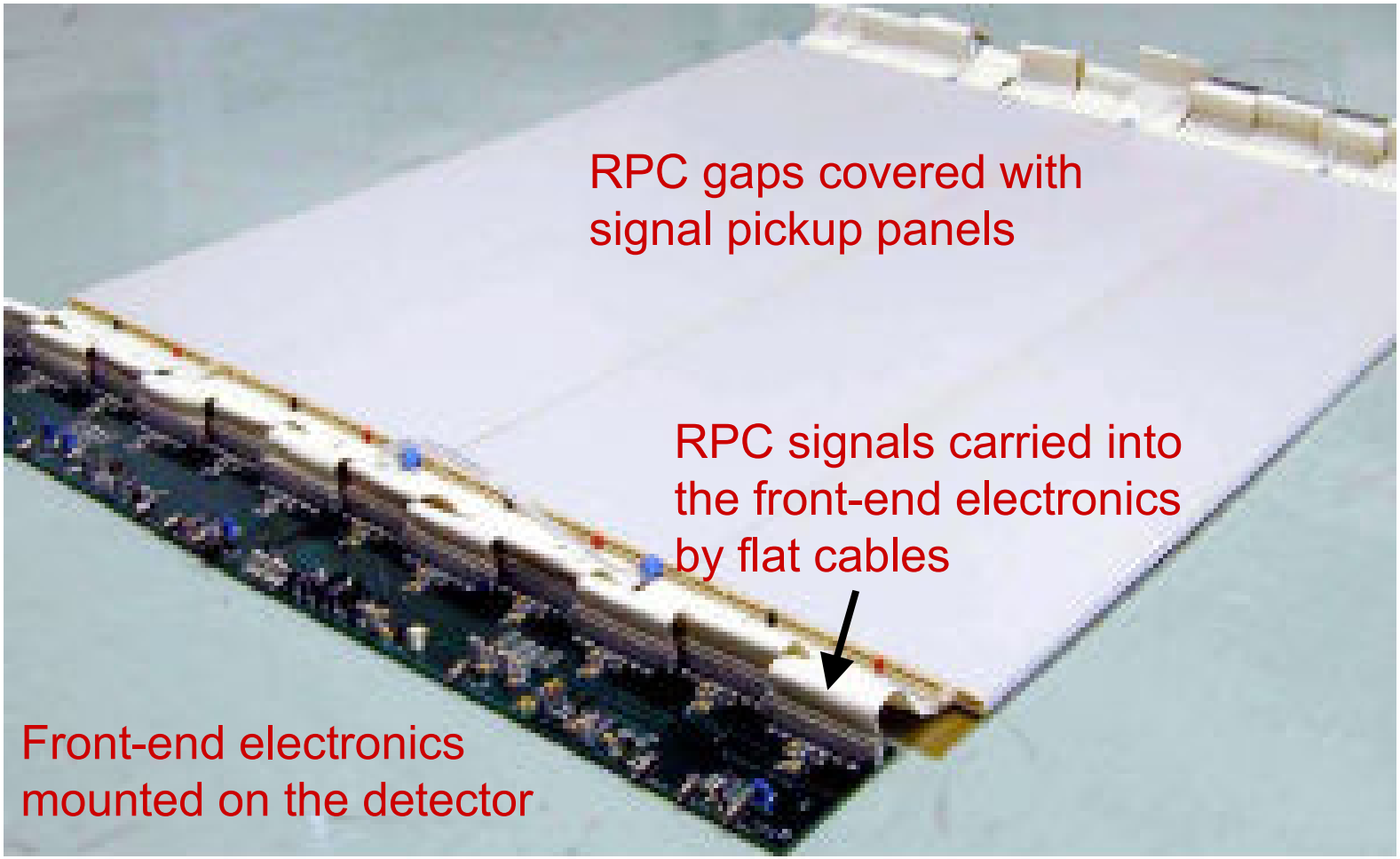
Layout of front-end chip



Layout of the chip

- Dimensions: 2.9 mm X 2.6 mm
- 64 I/O pads
- Package: QFP 68

Arrangement of front-end system



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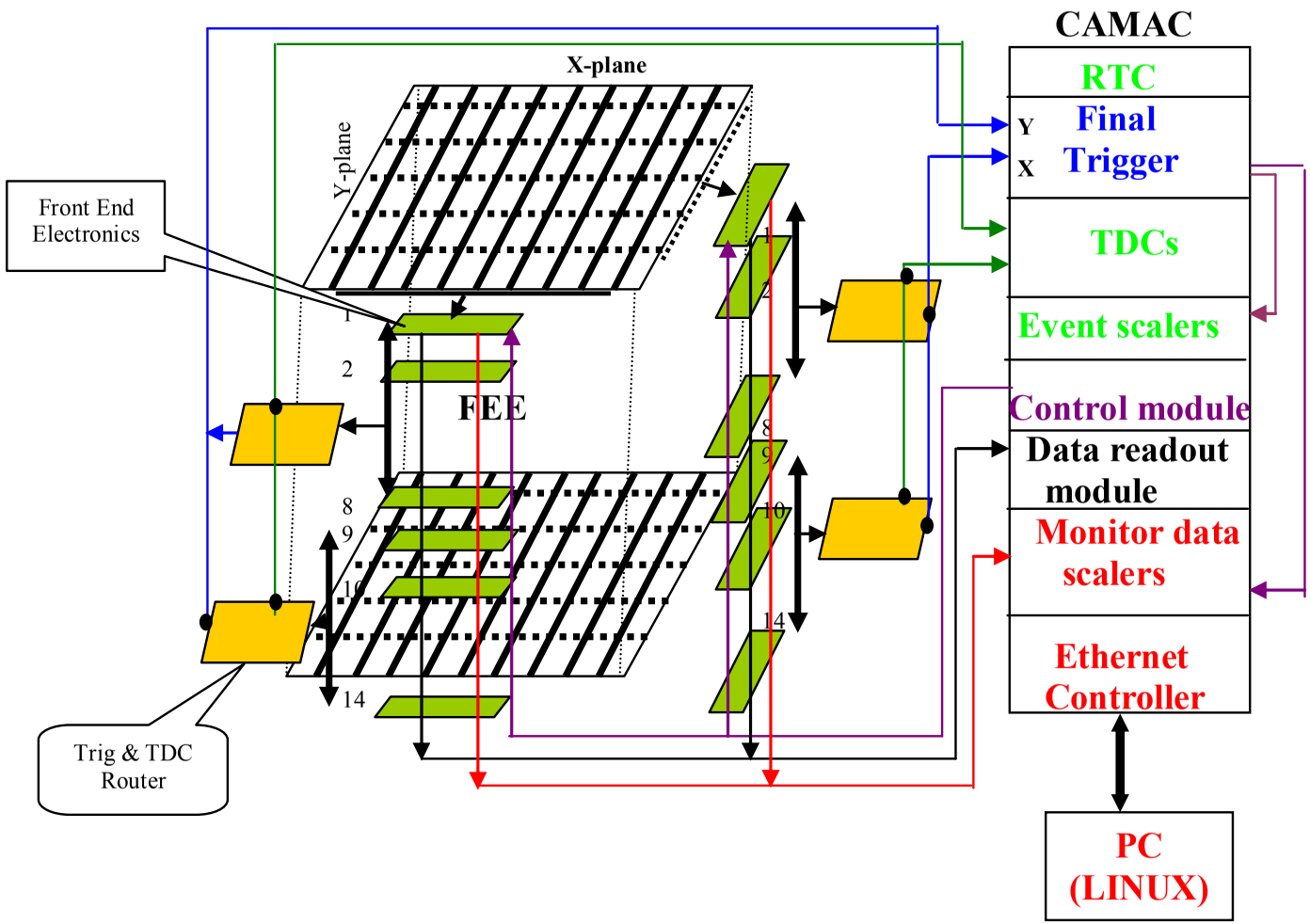
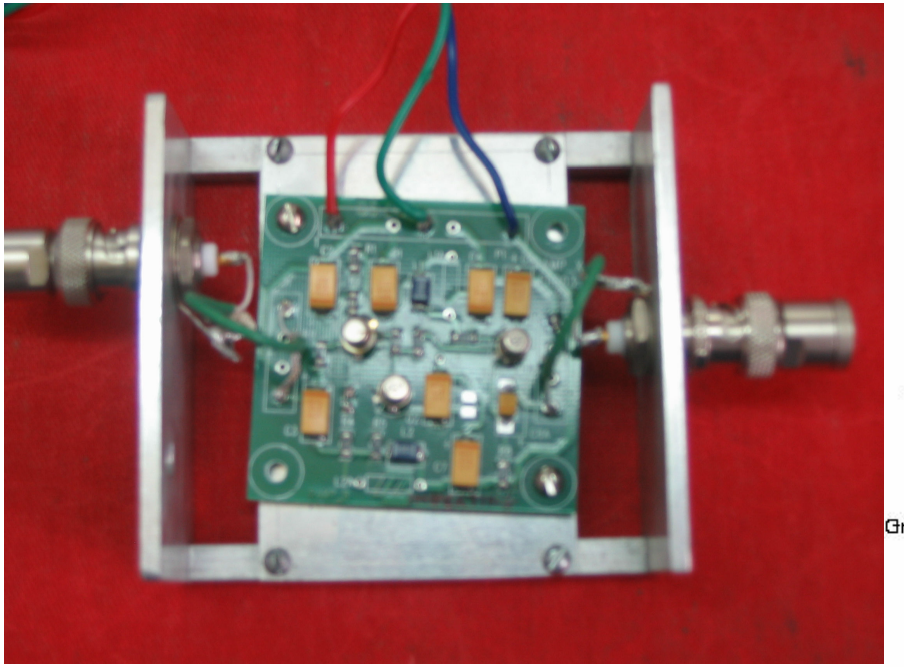
INO prototype detector

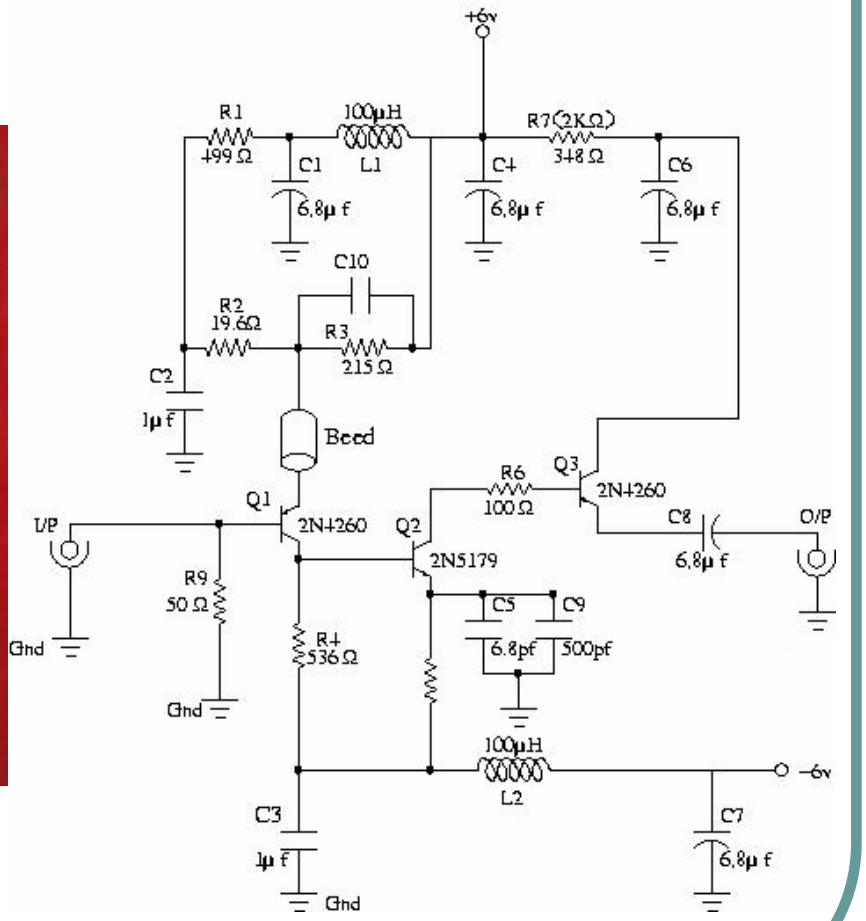
- **Detector and signal specifications**
  - Detector dimensions: 1m X 1m X 1m (approx.)
  - 14 layers (max) of RPCs with 6cm iron plates interleaved.
  - Two signal planes orthogonal to each other and each having 32 pick-up strips
  - Total channels = 32 X 14 X 2 = 896
  - Pulse height = 100 to 300mV; Rise time = < 1 ns
  - Pulse width = ~50ns; Rate ~ 1KHz
- **Trigger information**
  - Expected trigger rate is few Hz
  - Required (in situ) trigger logic is **m X n** fold, where
  - m = 1 to 4; no. of consecutive channels in a layer
  - n = 5 to 1; no. of consecutive layers with **m** fold in each layer
  - i.e. m x n = (1 x 5) OR (2 x 4) OR (3 x 3) OR (4 x 2)
  - External scintillate paddle based trigger
- **Information to be recorded on a trigger**
  - Absolute arrival time of the trigger
  - Track identification (XYZ points in RPC layers)
  - Direction of track (TDC information)
  - Miscellaneous information and calibration data
- **Monitoring health of the detector**

Readout scheme for prototype



Fast preamplifier

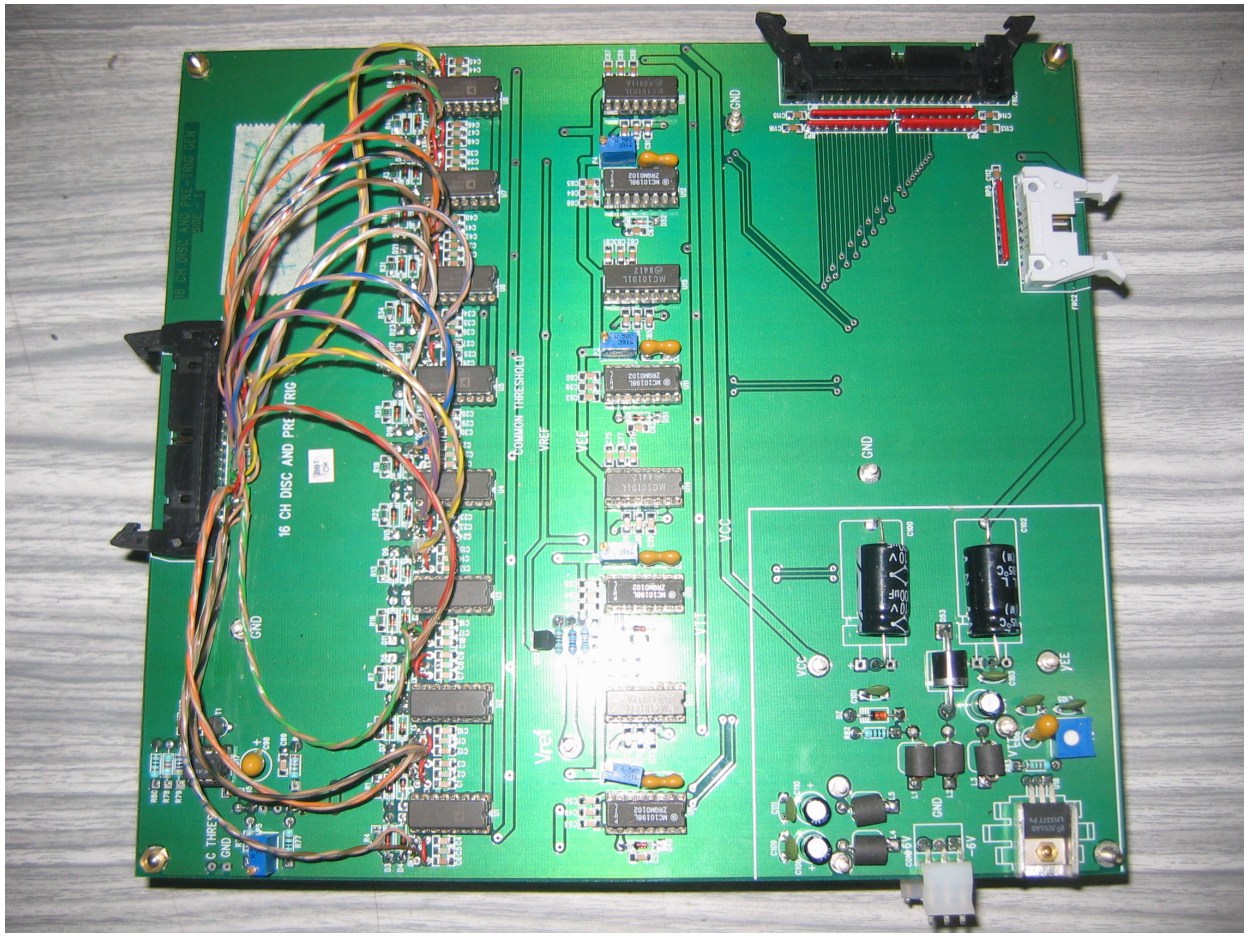




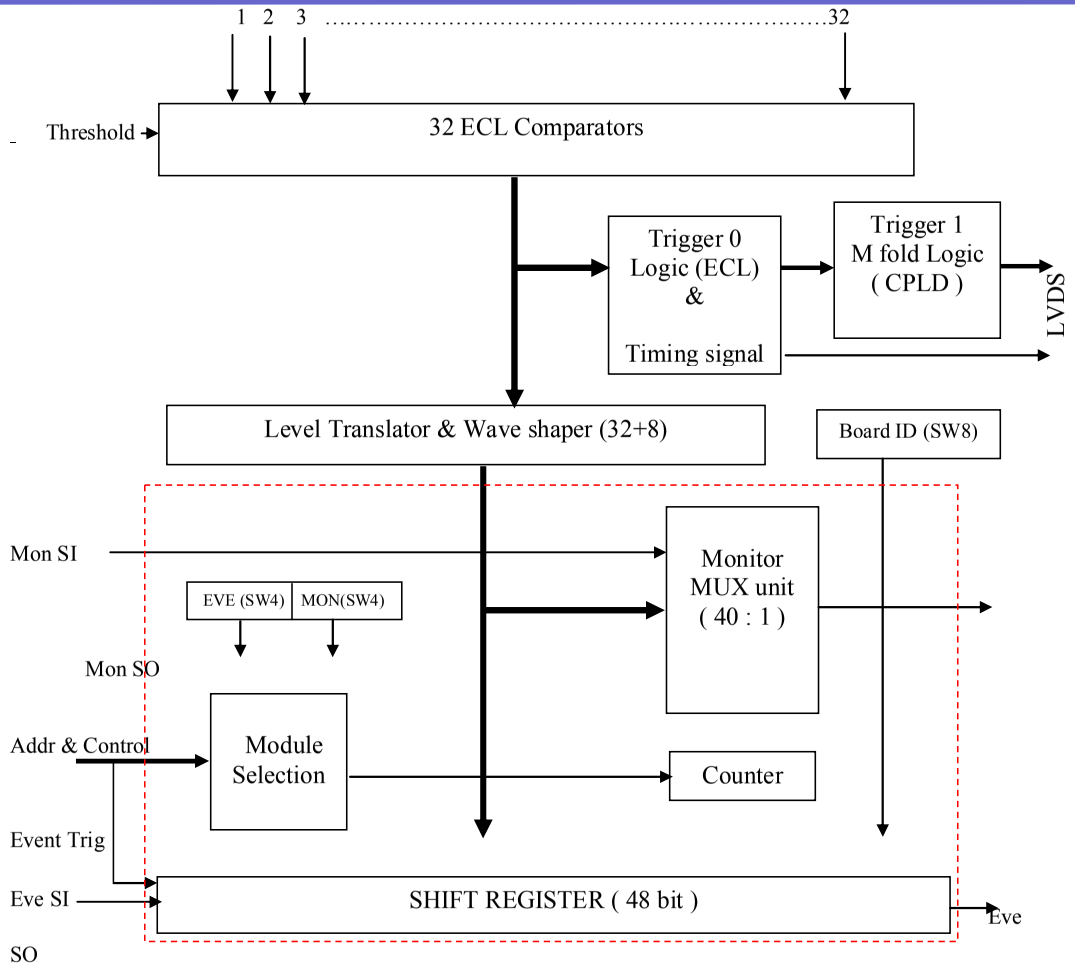
16-channel analog front-end

- Based on Analog Devices' Quad-device
- Fast comparator with ECL outputs
- Wire ORed pre-trigger outputs

16-channel analog front-end

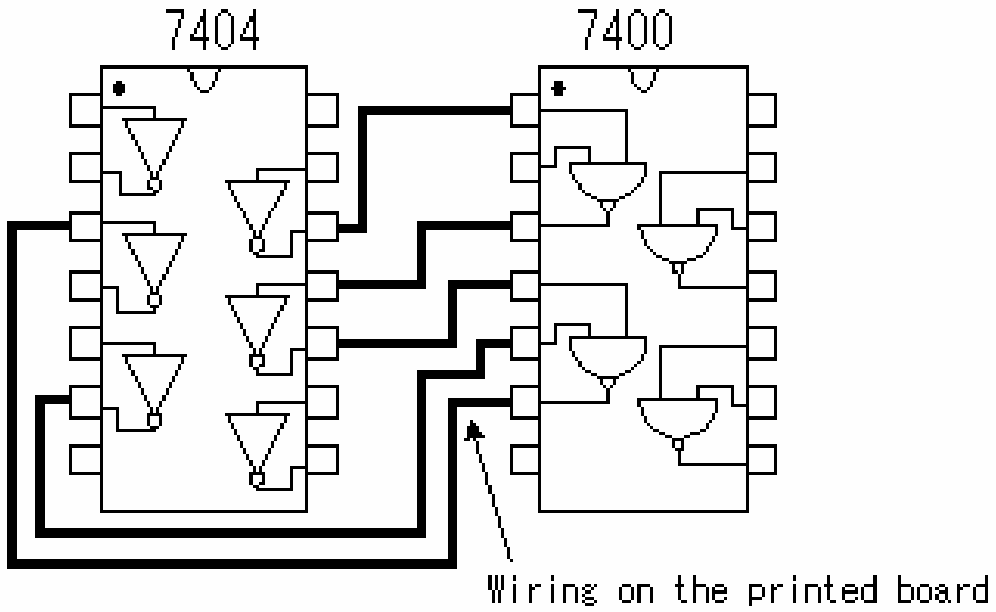


32-channel digital front-end



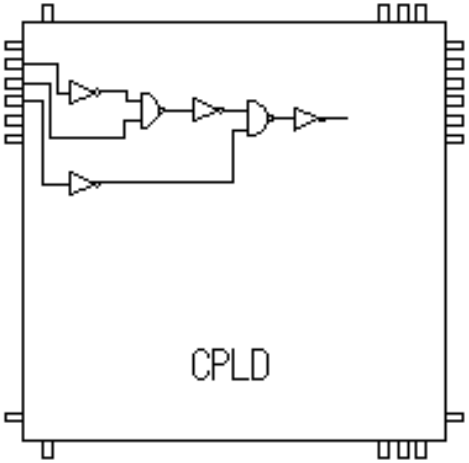
CPLD XC 95288 -HQ708

Discrete digital circuits

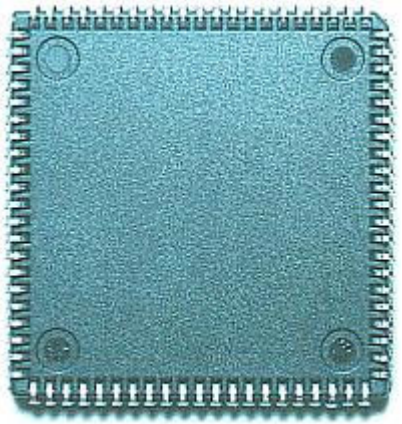


For example, in case of the 7400 IC, 4 circuits of 2 input NAND gate are housed. In case of 7404, 6 circuits of inverter are housed. These are separate ICs. Therefore, to compose a circuit, it is necessary to do each wiring among the pins using the printed board.

What is a CPLD?



Top side



Bottom side

- In case of CPLD, it has wiring among the logic in the IC. So, the wiring on the printed board can be made little.
- A lot of logic devices are housed in CPLD and those connections can be specified by the program.
- The capacity of CPLD is limited. There is limitation on the number of the pins, too.

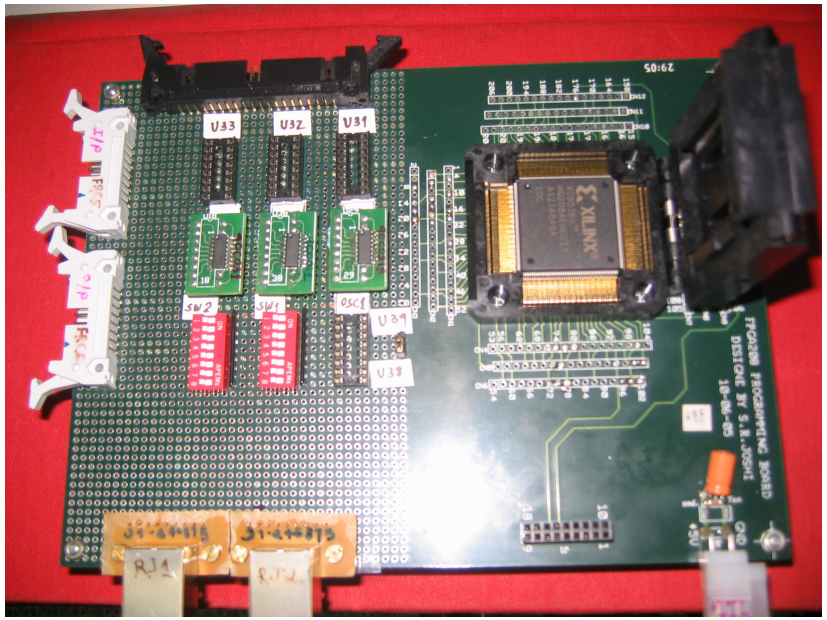
Features of CPLD

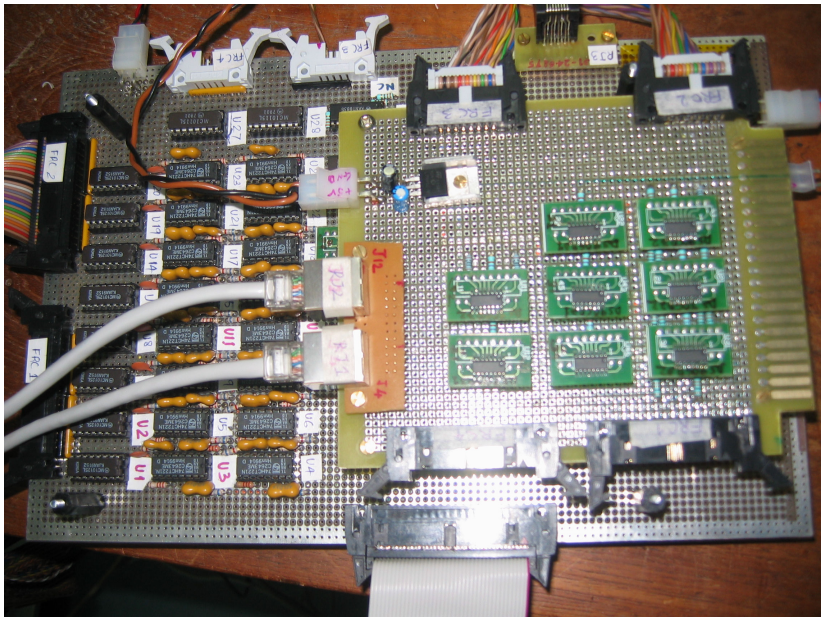
Parts name	Number of pins	Specification
XC9536-15PC44C	44pin PLCC	2FB/36macrocells/800gate
XC9572-15PC44C	44pin PLCC	4FB/72macrocells/1600gates
XC9572-15PC84C	84pin PLCC	4FB/72macrocells/1600gates
XC95108-5PC84C	84pin PLCC	6FB/108macrocells/2400gates

PLCC: Plastic Leaded Chip carrier, FB: Function Block

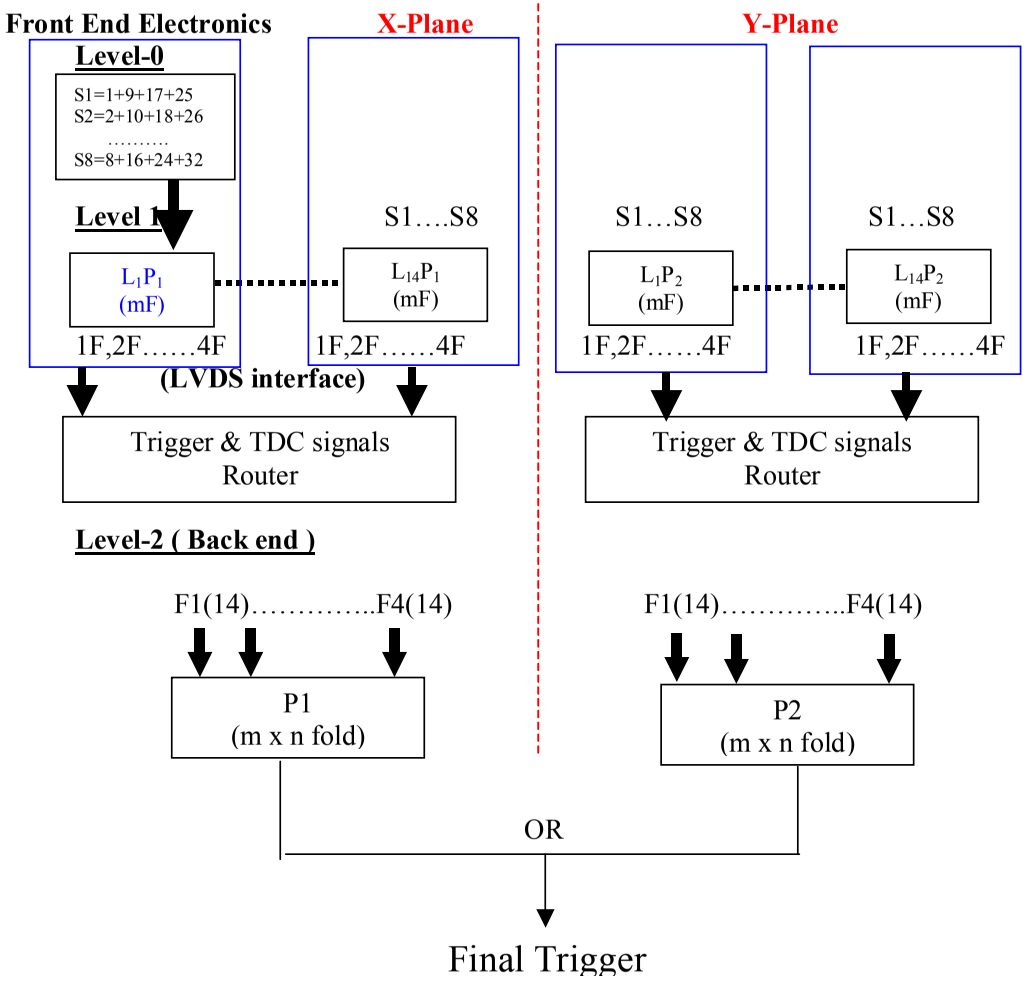
- It is possible to rewrite CPLD many times because it is recording the contents of the circuit to the flash memory.
- For example, in the case of XC9500 series, rewriting in about 10,000 is possible.
- In-situ programming of the chip possible.

32-channel digital front-end

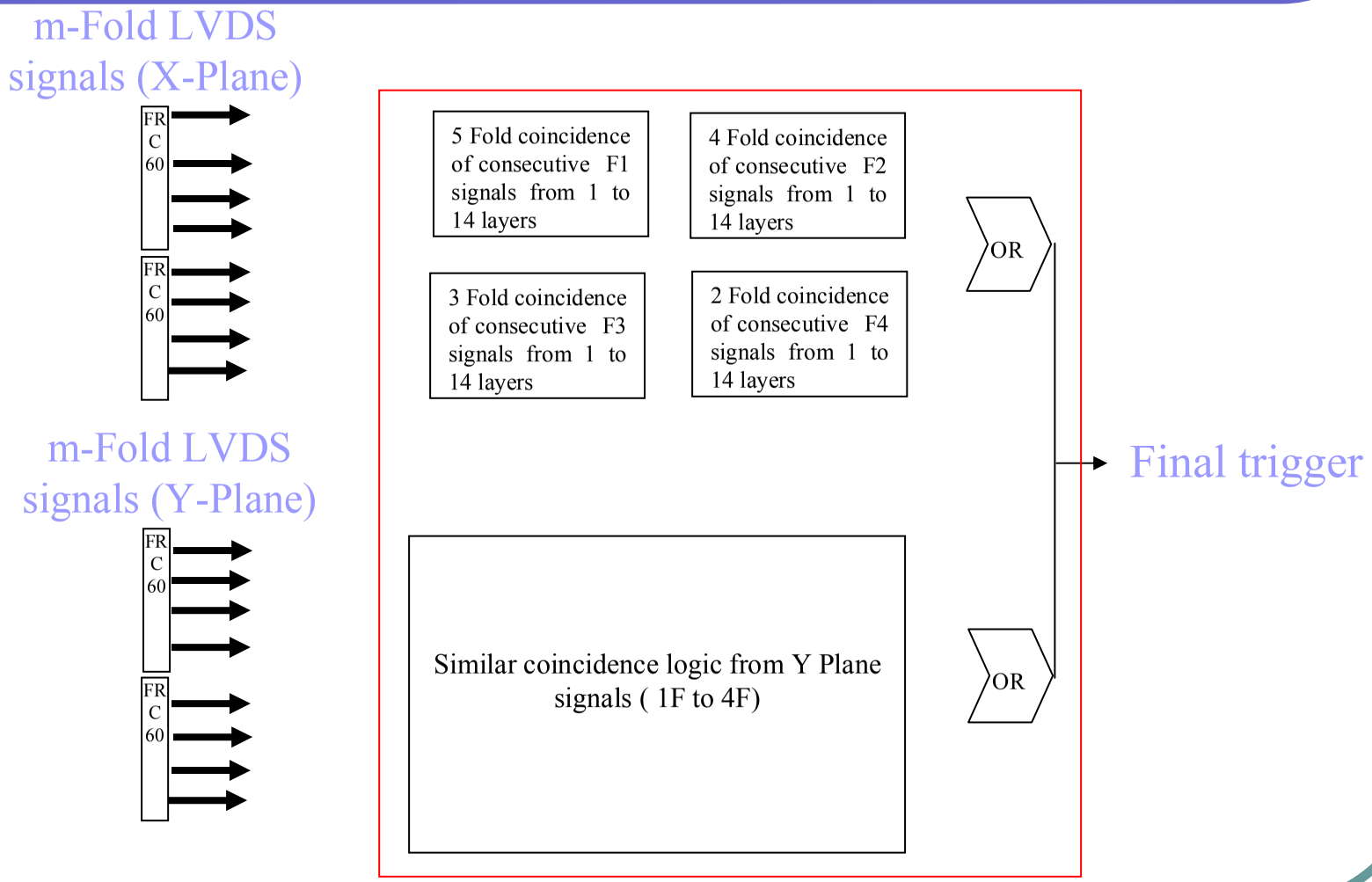




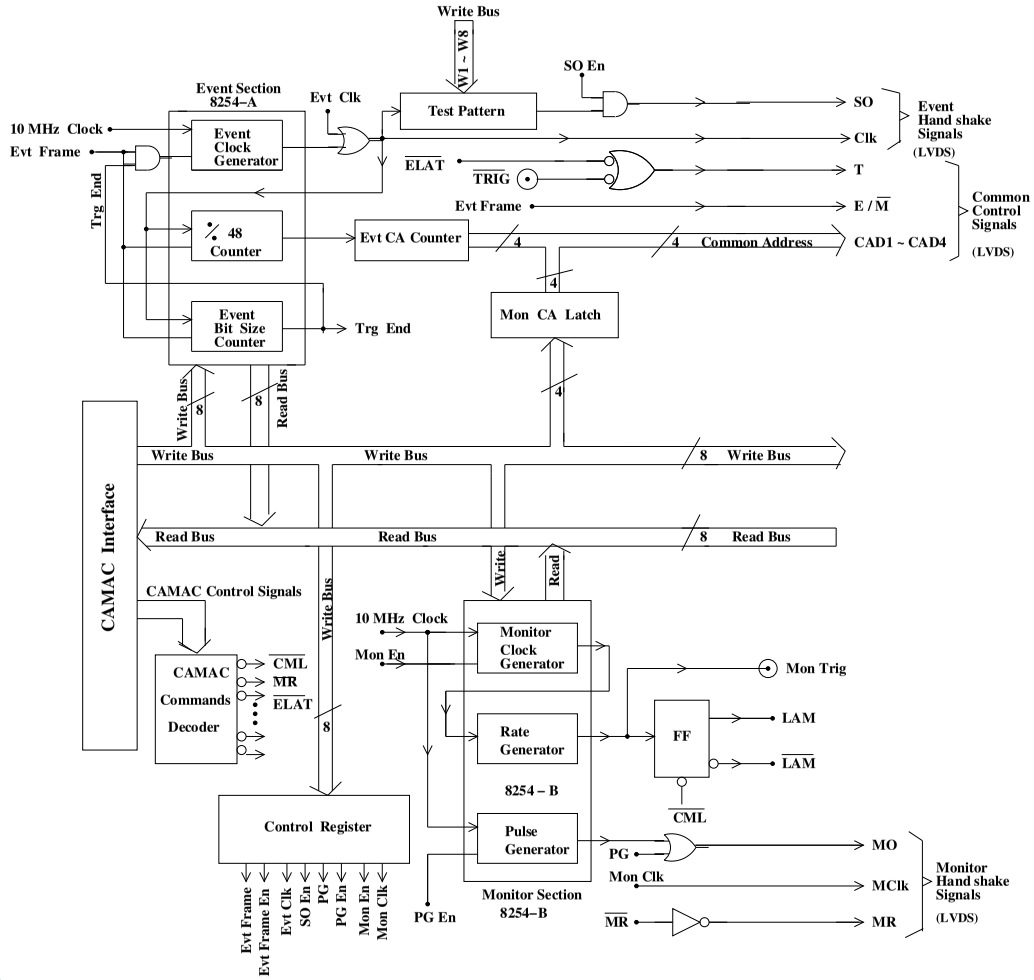
Prototype detector trigger logic



CAMAC based trigger module

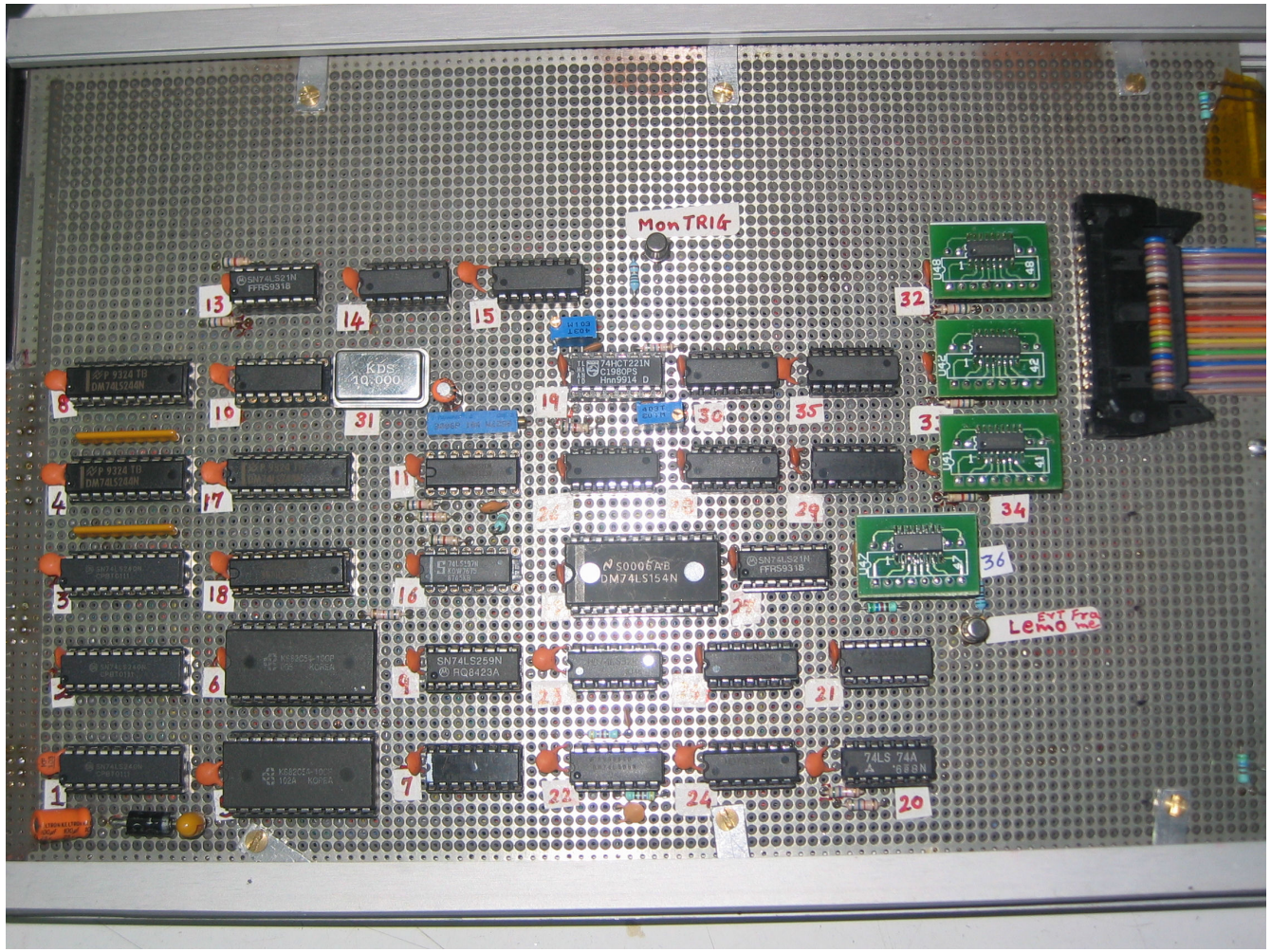


CAMAC based control module



Generates three sets of control and hand shake signals for selection of DFE board, readout of event data and monitoring of pickup signals in the selected board

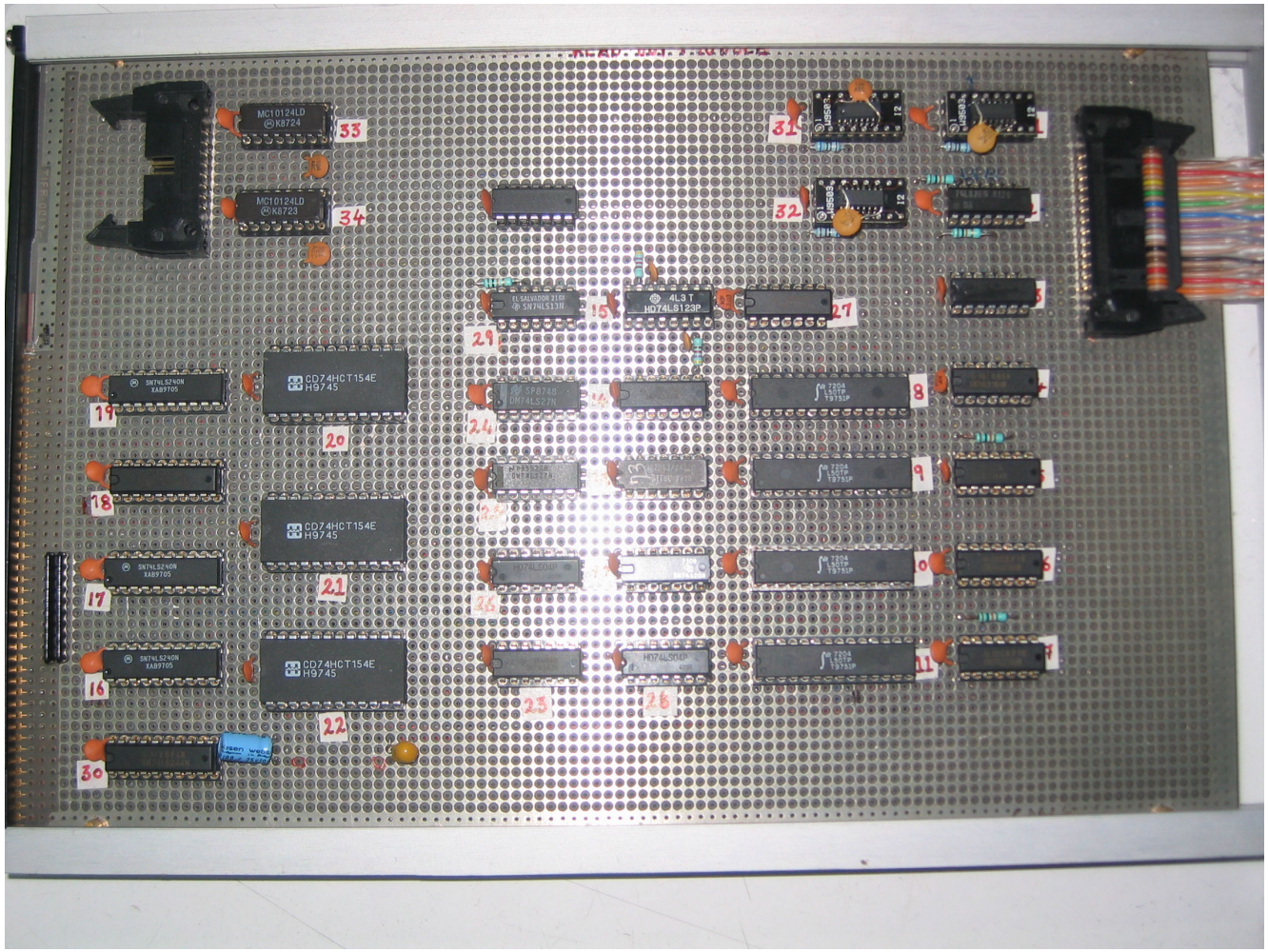
DAQ control module



CAMAC based readout module

- Four serial event data read out channels
- Eight monitor data inputs
- Serial to parallel conversion of event data
- Data written into FIFO buffer
- FIFO buffers readout through CAMAC backplane in the event routine
- Eight selected monitor channels translated into ECL logic signals
- Rates monitored through ECL input CAMAC scalar modules

Data readout module



Other items

- High voltage supplies
- Low voltage supplies
- Components, cables etc
- Commercial/available modules
  - TDCs
  - Scalers
  - CAMAC crates and controllers
- DAQ software on Linux platform

Backend DAQ system

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INO detector specifications

Number of modules	3
Module dimensions	16 m X 16 m X 12 m
Detector dimensions	48 m X 16 m X 12 m
Number of layers	140
Iron plate thickness	~6 cm
Gap for RPC trays	2.5 cm
Magnetic field	1.3 Tesla
RPC unit dimensions	2 m X 2 m
Readout strip width	3 cm
Number of RPCs/Road/Layer	8
Number of Roads/Layer/Module	8
Number of RPC units/Layer	192
Total number of RPC units	27000
Number of electronic channels	3.6×10^6

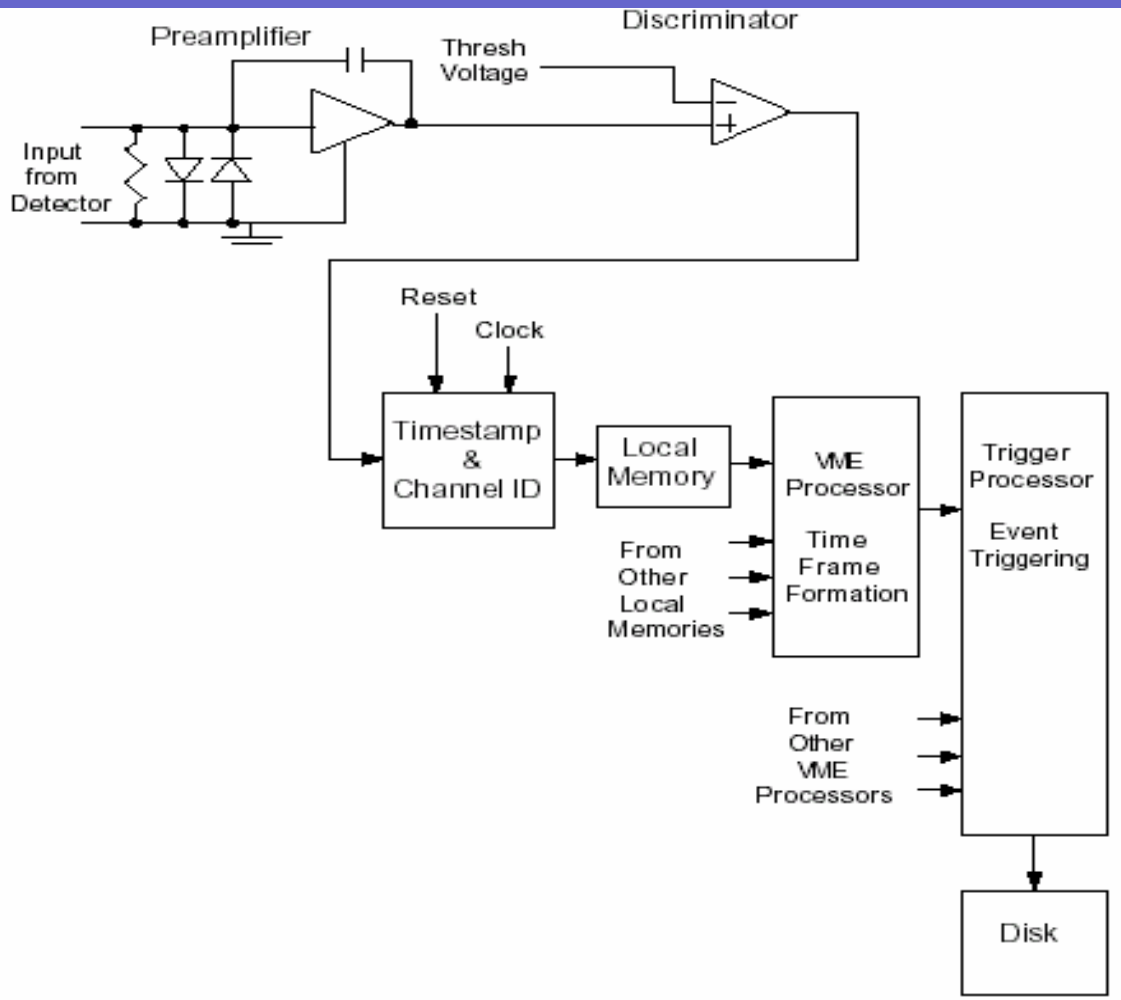
Thoughts on eTRIDAS for ICAL

- KGF still inspires!
- Channel count a factor of 1000 for ICAL
- Time tested ideas; blended with VLSI technology
- *Reasonably* simple scheme; the need is density
- Low rates; high degree of multiplexing possible
- ASICs, pipelining, trigger farm,VME are the keys
- ASICs for front-end, timing, even for trigger!

Major sub-systems

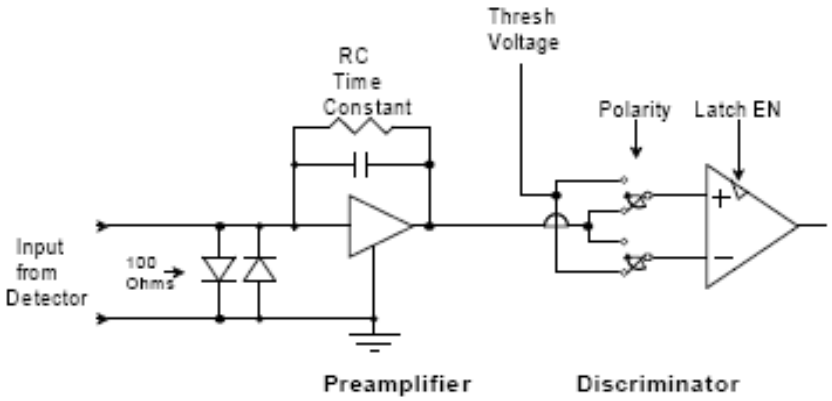
- Analog and digital front-ends
  - Mounted on or very close to detectors
  - Programmable preamps and comparators
  - Latches, pre-trigger generators, pipelines and buffers
  - Data concentrators and high speed serial transmitters
- VME back-ends
  - Data collectors and frame transmitters
  - Time to digital converters (TDCs)
- Trigger system
  - Works on inputs from front-ends, back-ends or external
  - Place for high density FPGA devices

Overall schematic of a DAQ system



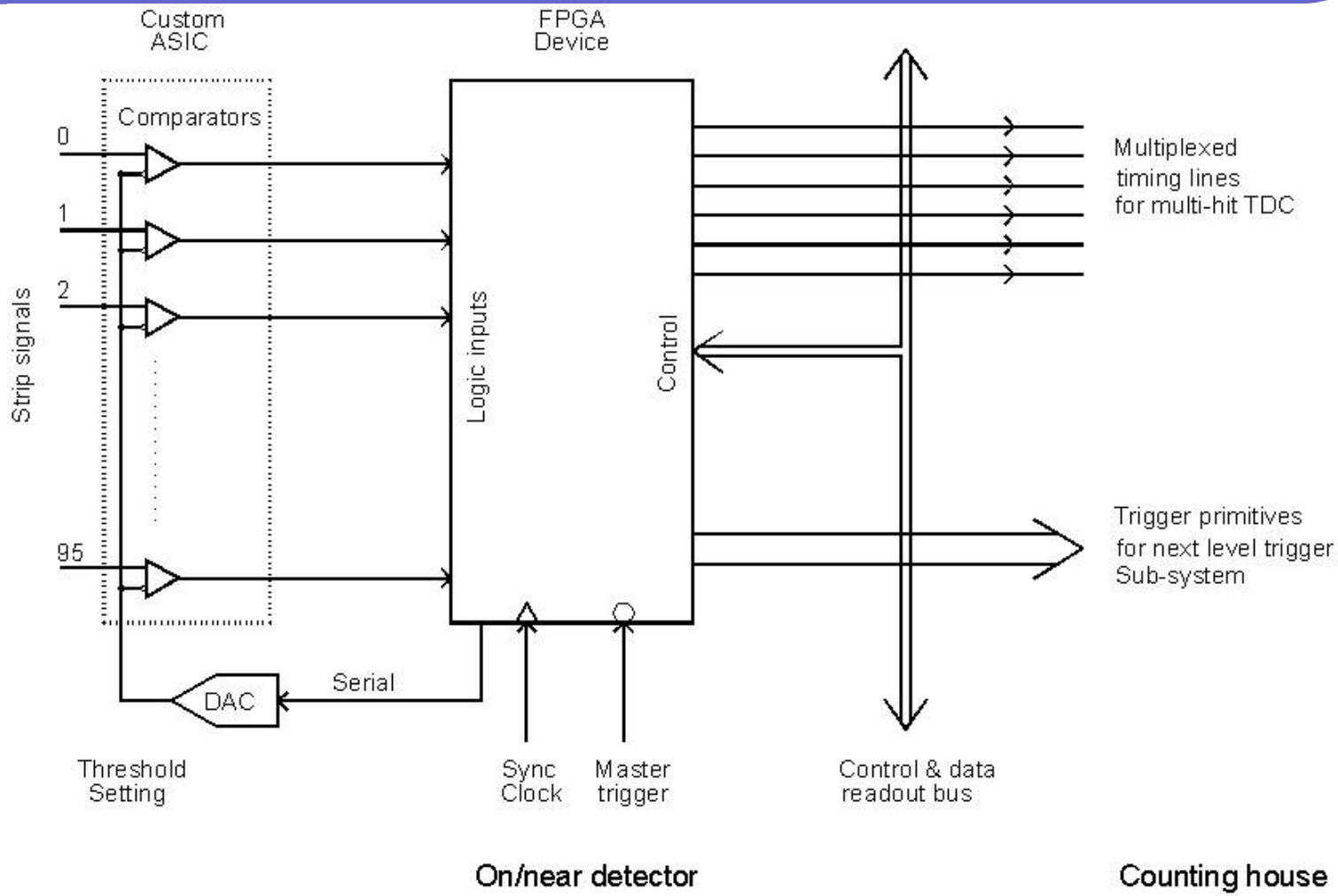
General concepts

- **Develop a Custom Front-End ASIC, Which Services Many Detector Channels (64 → 128)**
- **Each Channel has a Discriminator**
  - **A 1-Bit ADC!**
- **Each Channel has a Preamplifier**
  - **Needed for Avalanche Mode**
  - **Can Bypass if Desired (→ Streamer Mode)**
  - **Provides Pulse Shaping**

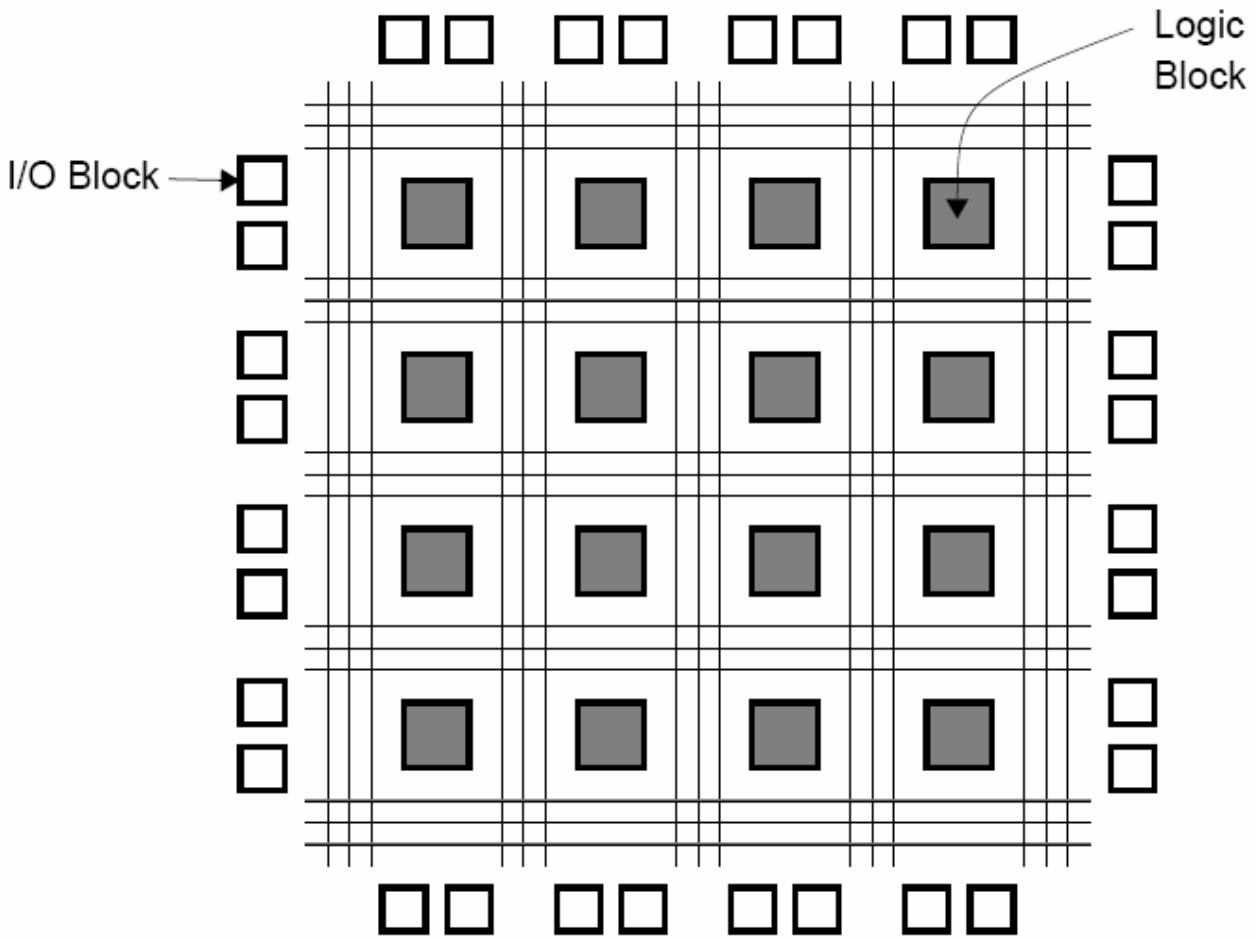


Block Diagram of Front End Amplifier (FEA)

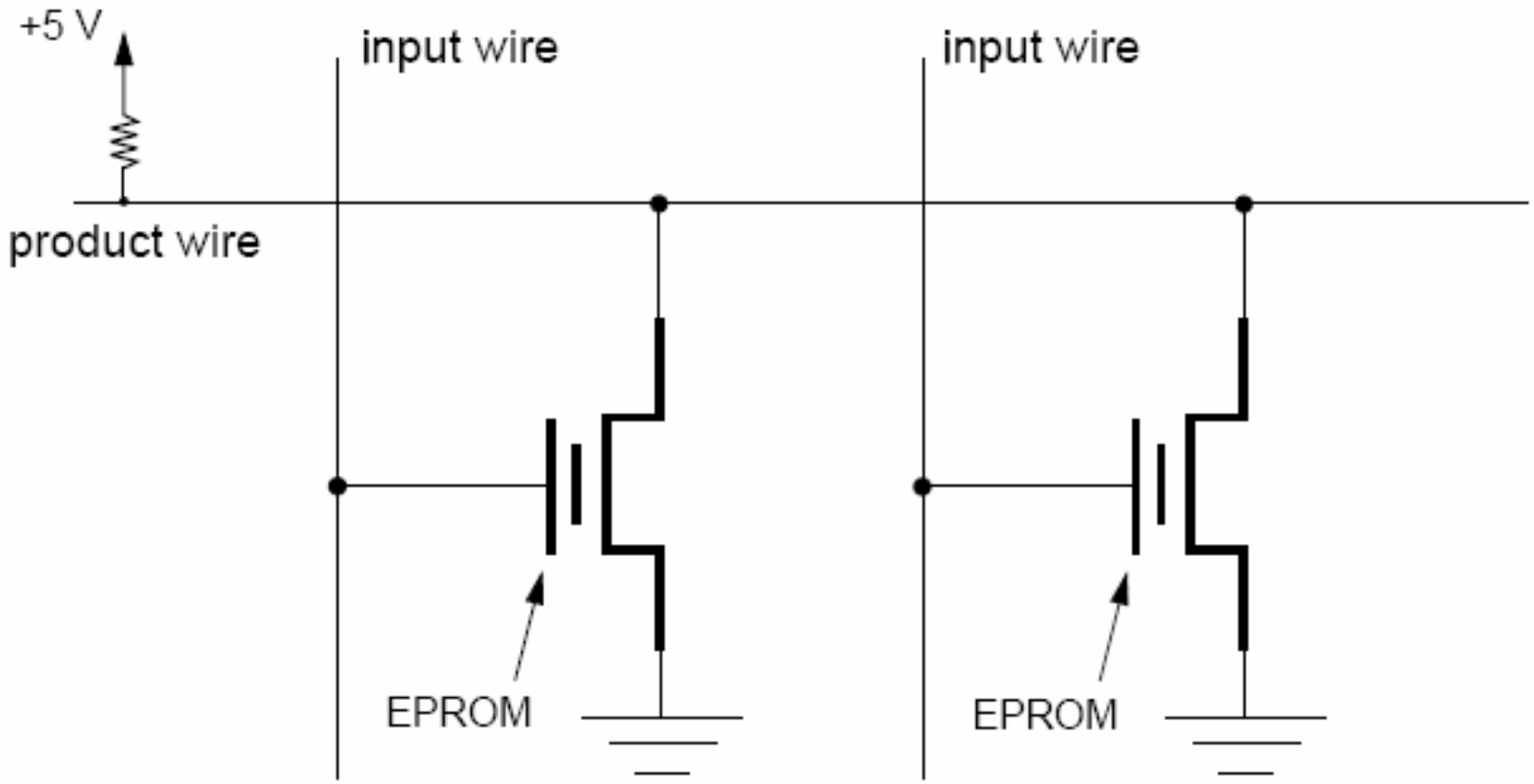
DAQ scheme for ICAL detector



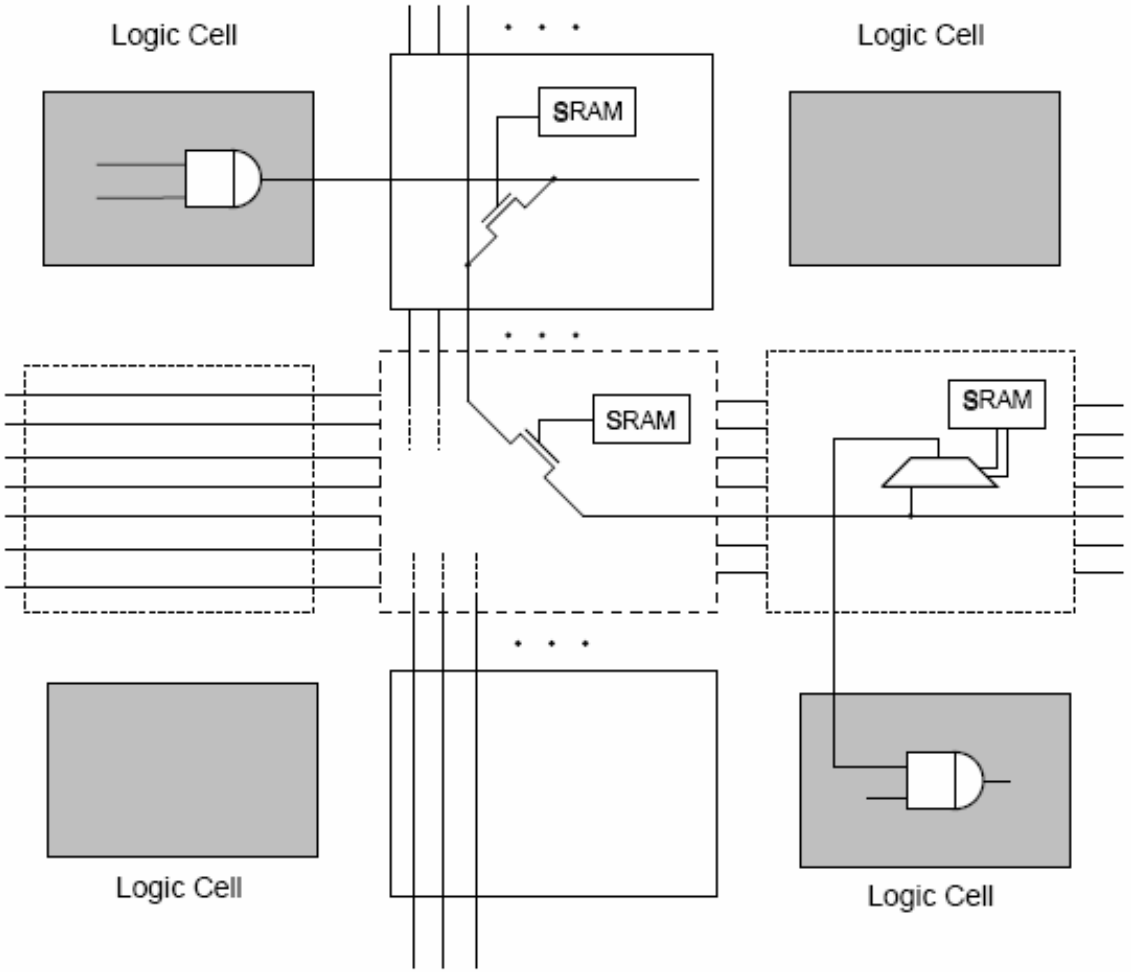
Structure of an FPGA



EPROM programmable switches



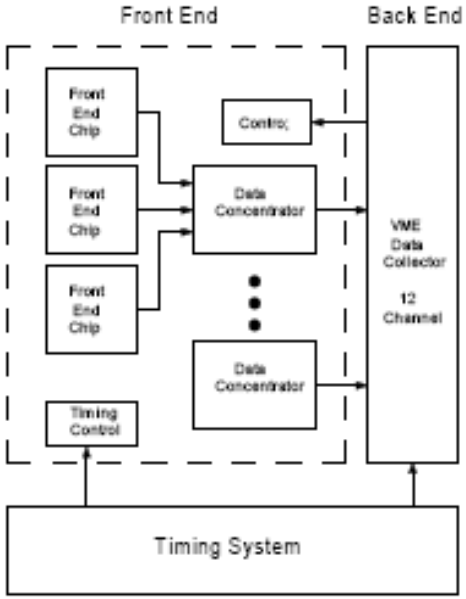
SRAM controlled programmable switches



Basic system architecture

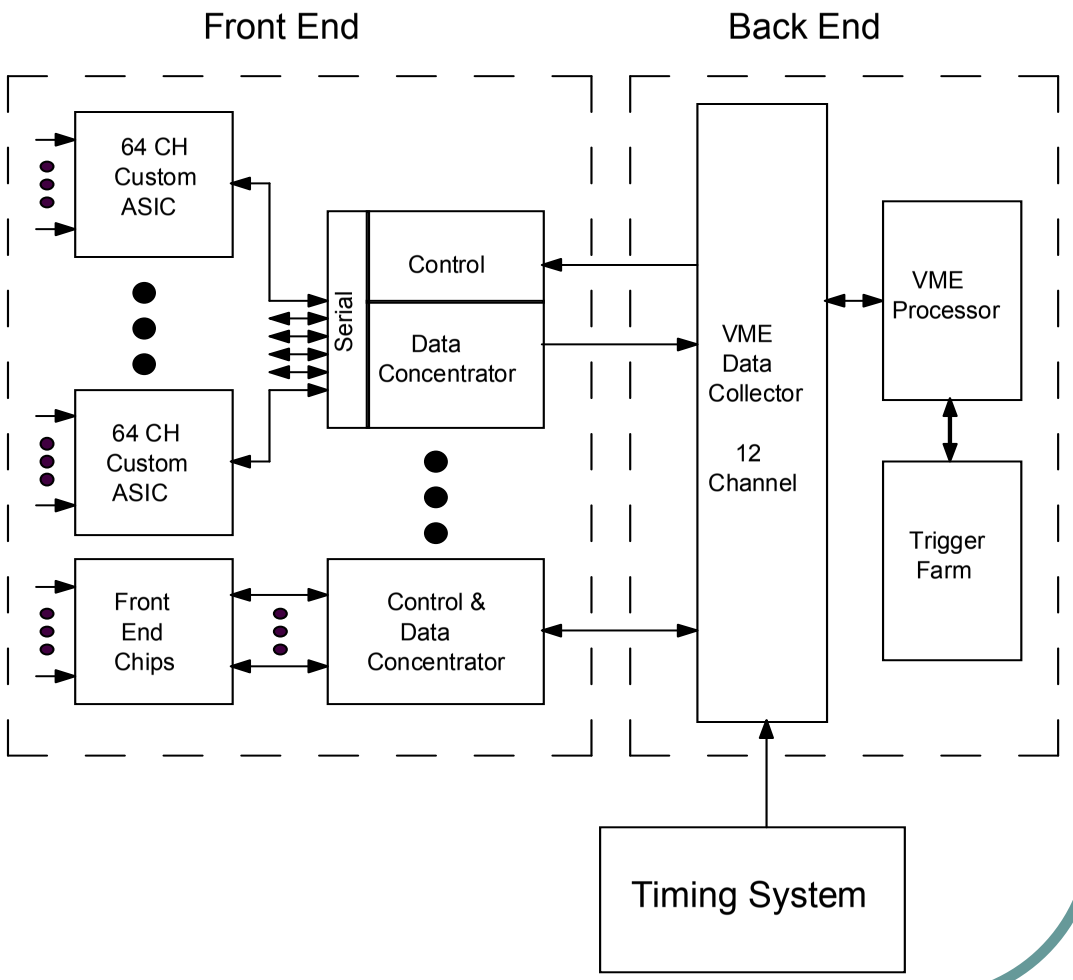
- *RPC ASIC* Resides *ON* Detector
- *Data Concentrator* Funnels Data From Several Front End Chips
- *VME Data Collector* Funnels Data from Several Data Concentrators

➢ Goal: Reduce Number of Expensive VME Crates & Cards



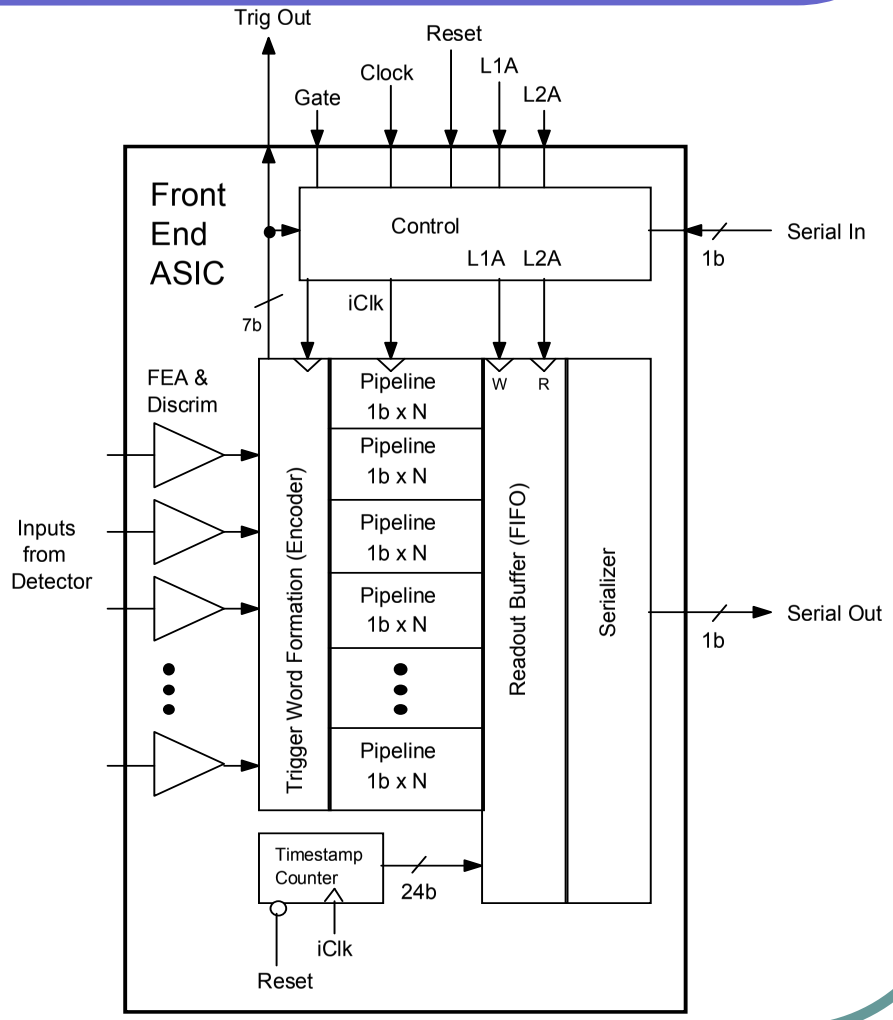
Overview of DAQ system

- Discriminates hits from detector
- Timestamps hits in front-end
- Stores timestamps in local buffers
- Concentrates data from single plane (low event rates)
- Super-concentrates data from several planes (faster clock)
- Uses back-end trigger processor to reconstruct hits



Front-end ASIC

- Handles 64 channels
- Resides near RPCs
- Performs Functions
  - Receive detector signals differentially
  - Timestamp hits
  - Temporary data storage
  - Serial I/O
- Captures bit-pattern when triggered



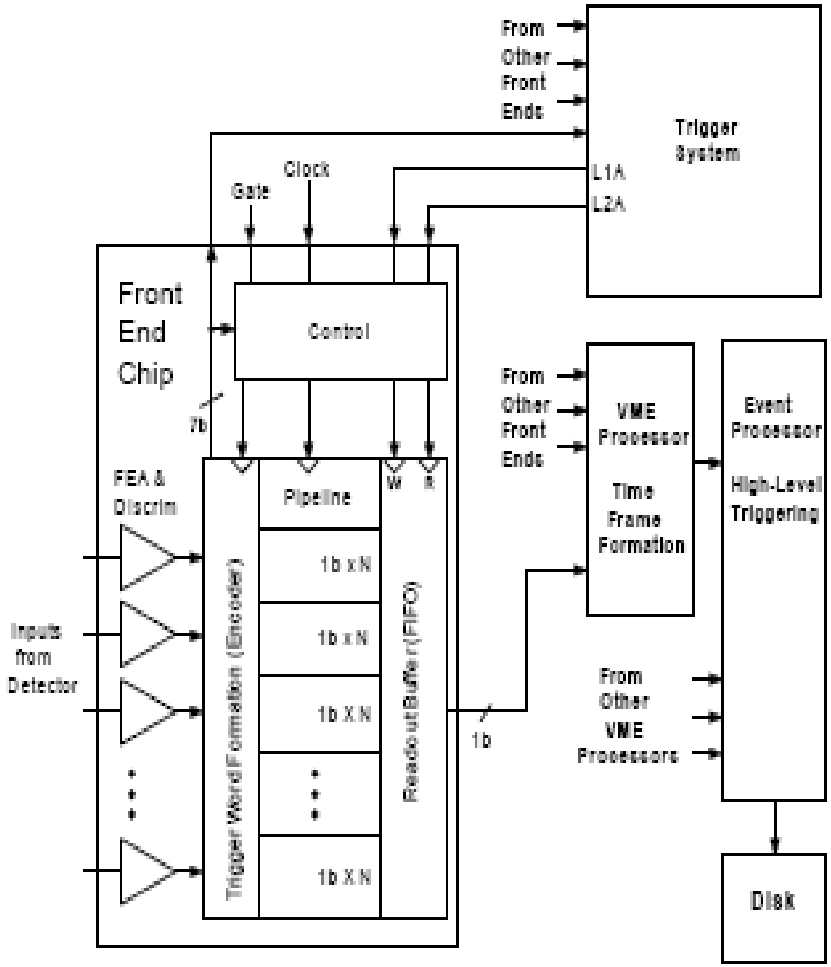
Trigger capability

- **Latch Outputs of All Discriminators on Each Clock Cycle, At Whatever Frequency Desired**
- **Put "Data Word" Into Pipeline**
- **Provide "L1" Trigger *N* nS Later to Capture data Word at End of Pipeline**
- **Store Data Word in Local Buffers, Read Out Periodically ("L2" Trigger…)**
- **Read Out Data into Higher-Level Trigger Processor to Perform Pattern Recognition**

➢ **Chip Can Provide Trigger Output, Based on Multiplicity of Hits in a Given Clock Period**

➢ **Preferred for Higher Rate Environments, or Multiple Detector Systems**

Triggered system



Without trigger capability

- **Timestamp Counter Running Inside Front End Chip**
- **Discriminator Output Latches Value of Timestamp**
- **Store Timestamps in Local Buffers, Read Out Periodically**
- **Read Out Timestamps into Trigger Processor**
- **Use Timestamps to Reconstruct Hits**

➢ **Simple Architecture**

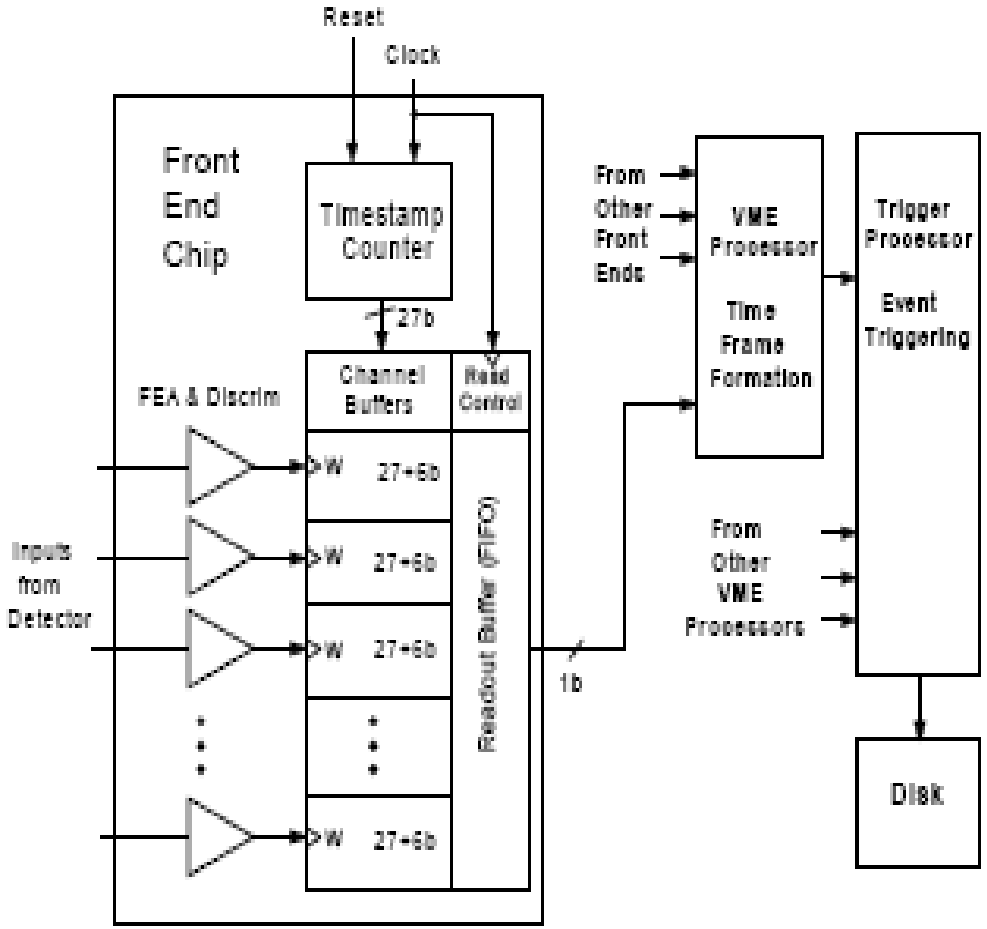
➢ **Works Well for Low Event Rates *and* Low Background & Noise Rates**

➢ **Like MINOS DAQ**

➢ **Might Be a Problem for Detectors on Surface…**

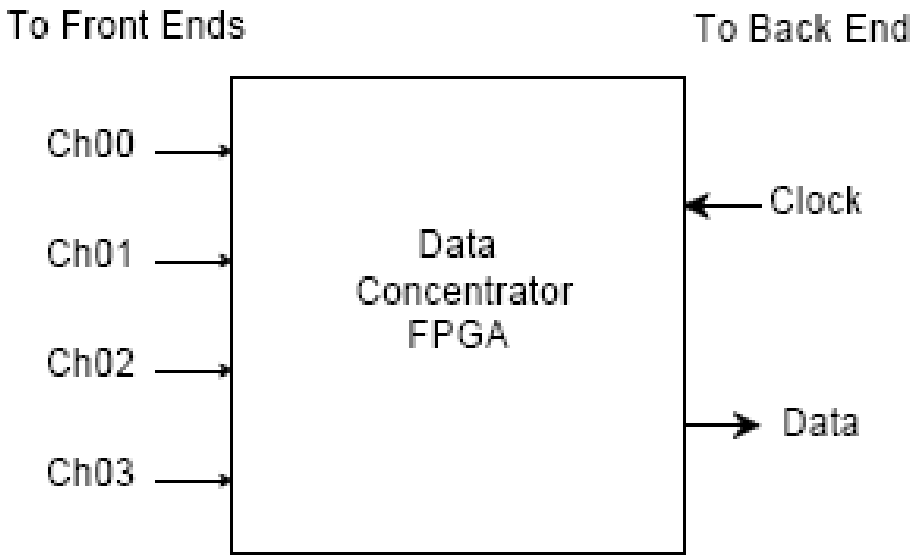
➢ **Might Be a Problem for a Testbeam…**

Trigger-less system



Data concentrator concept

- To reduce back-end costs
- Need intermediate data concentration on detector
- Multiplex data from several chips into a data stream
- Realization: FPGA



Backend readout

- Receive Serial Data Streams from Front End Data Concentrators
- Collect Data
- Form "Time Frames" (~1 Sec for MINOS)
- Send Data to Trigger Processor

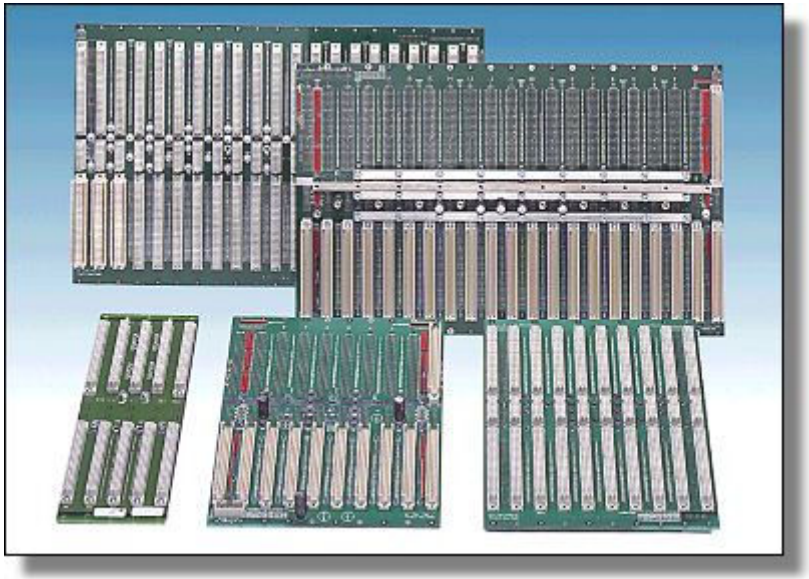
- Realization
  - Use VME Crates for Infrastructure
  - Data Collectors Receive Serial data Streams from Front Ends
  - Data Collectors Also Provide Clock & Control

Some technology standards

- Backend: VME
- Platform: Linux?
- Networking of processing nodes
- Front-end, gas system and HV control: Ethernet
- Ambient parameter monitoring: Embedded processors with Ethernet interfaces
- Web servers for operating parameter browsers
- On-fly sample data quality checks

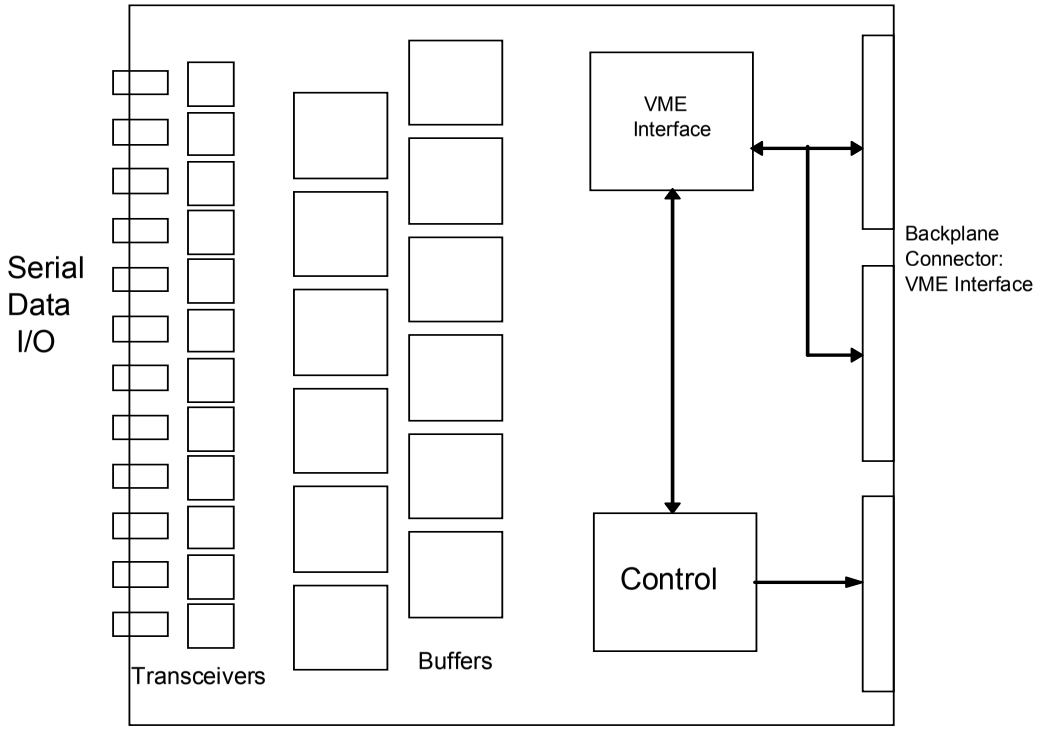
VME system hardware components

A modern fast, high density, modular, scientific instrumentation standard



Data collector module

- VME interface for readout
  - 9U x 400mm module
  - Handles 12 Inputs
- Receives data streams from concentrators
  - Fiber optic cables
- Saves data in one of the two buffers
- Reads buffers via VME bus
- Provides control for front-end systems



High voltage system

- Number of independently controllable channels?
  - 3 detector modules, 140 layers, 16m X 16m lateral size and RPC area of 2m X 2m
    - Worst case: Combine all RPCs in a layer $\rightarrow$ 420 channels
    - Best case: One channel per RPC $\rightarrow$ 27,000 channels!
    - We can settle for one channel/road/layer, for example
- Ramp rate, channel control, voltage and current monitoring are the bare minimum requirements
- Modular structure, Ethernet interface, local consoles, distributed displays, complete high voltage discharge etc are most desired features

Slow control and Monitoring

- Front-end control and monitoring
- High voltage control and monitoring of V & I
- Gas system monitoring
  - Channel control and flow monitoring
  - On-line gas sample analysis (RGA)
  - Gas leak monitoring
  - Moister level monitoring
- Ambient parameter monitoring
  - Temperature, barometric pressure, relative humidity
  - Data can be used for even for off-line corrections

Outline

- Introduction
- Basics of RPC signal formation
- Recordable parameters
- Front-end circuit design issues
- DAQ system for ICAL prototype
- DAQ schemes for INO detector
- **Course module summary**
- Acknowledgements & References

Summary

- ICAL detector monolithic (only RPCs); simpler DAQ architecture
- Main requirement for its DAQ system is large scale integration
- Front-end circuits' design crucial
- Deployment of FPGA, ASIC devices
- Monitoring of ambient, RPC and system parameters crucial

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Acknowledgements

- Gary Drake, ANL & Charlie Nelson, FNAL
- Flavio Loddo, INFN, Bari
- My INO colleagues

References

- NuMi Off-axis workshop, Stanford meeting
- INFN, Bari (Italy) group
- Belle experiment
- Monolith experiment (Proposal)
- LHC experiments (CMS in particular)