Regulated Cascode based Frontend ASIC "Anusparsh-II" for glass Resistive Plate Chamber (RPC) readout in the ICAL detector

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The ICAL detector will use glass Resistive Plate Chambers (RPCs) operating in the avalanche mode. As the detector requires readout of about 3.6 million signals, a multichannel, low power solution is desirable. A low power, fast frontend ASIC "Anusparsh" is designed successfully in 0.35µm mixed CMOS process using regulated cascode trans-impendence topology for the first time for readout of RPCs. A sub-nanosecond timing accuracy is required for precision leading time measurement, which is used for determining the directionality of muons in the ICAL experiment. The frontend ASIC is designed with very fast rise time for processing the RPC detector's pickup strip signals.

The "Anusparsh" ASIC is an eight channel differential input frontend readout ASIC, each channel comprising of a regulated cascode preamplifier, two stages of differential amplifiers with common mode feedback followed by a fast discriminator with LVDS outputs. The input stage is a regulated cascode (RGC) trans-impedance pre-amplifier that is coupled to the RPC detector pickups of characteristic impedance of 50Ω, exhibiting nearly matching impedance over a wide frequency range. The simulated S_{11} parameter at the pre-amplifier input is less than -11dB up to 1GHz for source impedance of 50Ω. The signals from all the eight channels are multiplexed to a common analog output buffer to monitor the detector pulse profile. The analog buffer is designed to drive 50Ω || 10pF load, maintaining the amplifier's sub-nanosecond response. The ASIC provides maximum trans-impedance gain of 7 mV/µA and consumes 50 mW/channel power using 3.3V supply. It can also be operated in the low power mode consuming 38mW/channel by disabling the output buffer. The ASIC has an input referred noise spectral density of 145 pA/$\sqrt{Hz}$.

This paper describes the design approach for development of the frontend ASIC in order to meet the stringent specifications of gain, timing, drive, swing and power consumption. Preliminary results on the chip validation and performance studies on the ICAL RPC detector will also be presented.

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