Trigger Latency Estimation for the ICAL Detector Module

(Version 0.1 Dated May 28, 2011)

The proposed trigger scheme for the ICAL detector module consists of a distributed and hierarchical architecture. Local trigger is generated at the segment level by the Local Trigger Module (LTM) and the local triggers from all constituent segments of the detector module are combined together by the Global Trigger Module (GTM) to produce global trigger at the module level. An estimate of the worst-case latency involved in trigger generation is essential for determining parameters like minimum width of shaped strip pulses, full scale range of TDC etc. This is also necessary in order to fix the width of coincidence window in different levels of trigger generation. Two alternate schemes for the placement of LTMs are being pursued now and the estimation of trigger latency and coincidence window width has been discussed for both.

1. Scheme A

Fig.1 shows the placement of LTM and GTM under scheme A. LTMs are placed on the front as well as back face of the detector. The GTM is placed along with the back-end at one corner of the detector module.

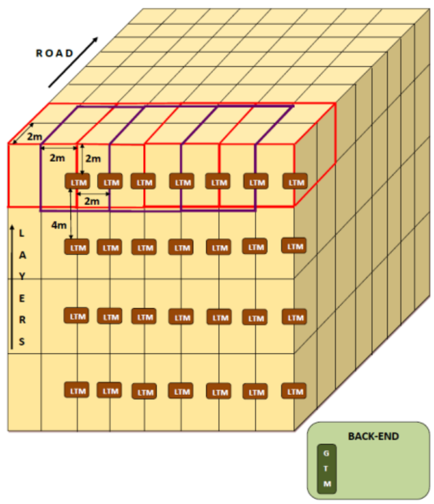

Fig.1. Placement of Local Trigger Module (LTM) and Global Trigger Module (GTM) under Scheme A

1.1. Trigger Latency

Maximum routing and processing delays involved in different stages of the generation of local trigger are listed in table 1. Henceforth, two different approaches have been taken into consideration.

PATH	**DELAY (ns)**
RPC cable length (Front-end to RPC-DAQ board) : 3m	15
Processing delay in RPC-DAQ board	10
Cable length from RPC-DAQ board to LTM : 10m	50
Processing delay in LTM	20
Delay introduced for de-glitching	10
Track-length (diagonal-length for a volume of 4mx4mx1m) : 6m	20
Cable length for fan-out to neighboring segment : 4m	20
Processing delay in generating fan-out	10
Tolerance	15
Net delay in local trigger generation	**170**

Table 1. Various delays incorporated in local trigger generation for Scheme A

1.1.1. Local Trigger

The local trigger generated at the segment level is fed back to all the constituent RPCs of that segment as well as the neighboring segments for the purpose of latching the strip hit signals and timing measurement by the TDC. One segment can have a maximum of 26 neighboring segments and hence generation of a single local trigger signal will initiate latching of data in 27 segments.

Two different cases have been considered in handling the segments.

1.1.1.1. Case I

The segments along half-a-road of the detector module are assumed to be handled independently by the LTMs positioned on either face of the detector. Due to some mechanical constraints, there is no LTM for segments lying across the half-road and no interconnection exists between segments lying on opposite halves of the road. Table 2 displays the worst trigger latency in such a scenario.

PATH	**DELAY (ns)**
Generation of local trigger	170
Return path to RPC-DAQ board : 16m	80
Tolerance	50
Local trigger latency	**300**

Table 2. Local Trigger latency for Case I of Scheme A

The concept of dividing the detector into two independent halves along the road may help to avoid a lot of mechanical issues but also poses a serious risk towards loss of some genuine events which may be distributed over segments lying across the half-road.

1.1.1.2. Case II

It is assumed that segments across half-a-road can be dealt with by the same LTM by overcoming the mechanical constraints. The maximum cable length from RPC-DAQ board to LTM sitting on the detector face, in this case, would be 14m i.e. net delay in generating local trigger would be 190ns. Maximum length of the return path of local trigger from LTM output to RPC-DAQ board can be 32m or 48m depending on whether the cable is routed through the detector or around the detector. The maximum trigger latency in this case is shown in table 3.

PATH	**DELAY (ns)**
Generation of local trigger	190
Return path to RPC-DAQ board : 32m / 48m	160 / 240
Tolerance	50
Local trigger latency	**400 / 480**

Table 3. Local Trigger latency for Case II of Scheme A

Some issues have to be taken care of in both the afore-mentioned cases.

I. Multiple segments may generate local trigger in case of a long track and hence multiple triggers may be fed to one RPC-DAQ board for the same event. The system should be capable of handling such a situation.
II. Propagation of the local trigger from LTM output back to all the RPC-DAQ boards have to be completely synchronized so that there is no relative delay between the paths as it is very critical for proper timing measurement by the TDC.
III. Lots of interconnections between adjacent LTMs have to be routed carefully.

1.1.2. Global Trigger

Global trigger generated at the module level by combining local triggers from all the constituent segments of the detector module is fed back to each RPC of the module for strip hit latch and recording of timing information by the TDC. In order to calculate the worst-case latency, it is assumed that the GTM is placed at one corner of the detector module and in this case, longest path for the local trigger from LTM output to GTM input or the return path of the GTM output will be approximately 50m. Table 4 shows the trigger latency in such a condition.

This scheme also requires complete synchronization of the propagation of global trigger from GTM output back to all RPC-DAQ boards. Use of global trigger offers higher trigger latency than local trigger but is advantageous due the fact that it avoids the need of interconnection between adjacent segments and thereby eliminates a lot of routing issues.

PATH	**DELAY (ns)**
Generation of local trigger	190
Propagation of local trigger from LTM output to GTM input : 50m	250
Processing delay in GTM	10
Return path to RPC-DAQ board : 50m	250
Tolerance	50
Global trigger latency	**750**

Table 4. Global Trigger latency for Scheme A

1.2. Coincidence Window

It is necessary to fix this parameter at the LTM as well as GTM level.

1.2.1. LTM Level

Maximum relative delay between different input signals for a LTM, incorporated in different stages of propagation of trigger signal from the output of RPC-DAQ board up to the input of LTM, is shown in table 5. It is evident that coincidence window of width 125-150 ns should eliminate the need for delay compensation for the LTM input signals.

PATH	**DELAY (ns)**
Cable length difference from RPC-DAQ board to LTM : 6m (horizontal) + 6m (vertical) = 12m	60
Track-length (diagonal-length for a volume of 4mx4mx1m) : 6m	20
Fan-out delay	10
Tolerance	10
Net relative delay between LTM inputs	**100**

Table 5. Maximum Relative delay between LTM input signals for Scheme A

1.2.2. GTM Level

Maximum relative delay between different input signals for the GTM, incorporated in different stages of propagation of trigger signal from the output of RPC-DAQ board up to the input of GTM, is shown in table 7. Thus, a width of 350-400 ns should be sufficient for the coincidence window at the GTM level without going for any delay compensation for the GTM input signals.

PATH	**DELAY (ns)**
Cable length difference from RPC-DAQ board to LTM for different LTMs : 6m	30
Cable length difference from LTM output to GTM input : 50m	250
Tolerance	50
Net relative delay between GTM inputs	**330**

Table 6. Maximum Relative delay between GTM input signals for Scheme A

2. Scheme B

Implementation of scheme A should ensure that it does not offer any obstruction to the movement of RPCs in and out of the detector which makes the available physical space for positioning the LTMs too much stringent. Moreover, there would be a no. of mechanical issues in handling the segments lying across the half-road. An alternative scheme is to place the LTMs along with other back-end modules at one side of the detector as illustrated in Fig.2. This scheme offers much more flexibility towards the physical placement of the LTMs and simplifies the mechanical issues but at the expense of driving the pre-trigger signals over a much longer distance.

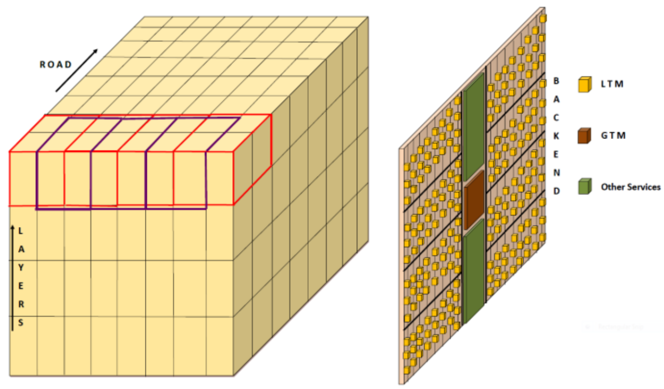

Fig.2. Placement of Local Trigger Module (LTM) and Global Trigger Module (GTM) under Scheme B

2.1. Trigger Latency

Various routing and processing delays involved in the generation of local trigger are listed in table 7. Hereafter, two different approaches are considered, similar to scheme A.

PATH	DELAY (ns)
Processing delay in RPC-DAQ board	10
Cable-length from RPC-DAQ board to LTM input : 40m	200
Processing in LTM	20
Delay introduced for de-glitching	20
Track-length (diagonal length for a volume of 4mx4mx1m) : 6m	20
Cable length for fan-out : 8m+4m = 12m	60
Fan-out generation	20
Tolerance	50
Net delay in local trigger generation	**400**

Table 7. Various delays incorporated in local trigger generation for Scheme B

2.1.1. Local Trigger

Table 8 shows the worst-case trigger latency when the local trigger generated at the LTM output is fed back to the all the constituent RPCs of that segment as well as the neighboring segments for the purpose of latching the strip hit signals and recording timing information by the TDC.

PATH	DELAY (ns)
Generation of local trigger	400
Return path to RPC-DAQ board : 45m	225
Tolerance	50
Local trigger latency	**675**

Table 8. Local Trigger latency for Scheme B

A no. of issues associated with the use of local trigger, as mentioned under scheme A, are likely to arise here too.

2.1.2. Global Trigger

The worst-case trigger latency when the global trigger produced at the GTM output is transmitted back to each RPC of the detector module is shown in table 9. The figures in table 8 and 9 reveal that the latency for local and global trigger are almost comparable under this scheme and hence the global trigger can be preferred over local trigger since it eliminates a lot of interconnection issues.

PATH	DELAY (ns)
Generation of local trigger	400
Propagation of local trigger from LTM output to GTM input : 13m	65
Processing in GTM	20
Return path to RPC-DAQ board : 45m	225
Tolerance	50
Global trigger latency	**760**

Table 9. Global Trigger latency for Scheme B

Nevertheless, complete synchronization of the return path of the trigger signal is absolutely necessary for proper timing measurement. This can be achieved either by active or passive delay compensation techniques but it has to be ensured that they do not introduce a jitter of more than 100ps since the TDC resolution would be 200ps. Another alternative is to estimate the delay offsets for the different paths through an intensive calibration process using test signals and incorporating the same in analysis. However, issues related to reliability and implementation of these techniques need to be explored thoroughly.

2.2. Coincidence Window

2.2.1. LTM Level

Maximum relative delay between different input signals for a LTM, incorporated in different stages of propagation of the trigger signal from the output of RPC-DAQ board up to the input of LTM, is shown in table 10. Hence, the need for delay compensation for the LTM input signals can be eliminated by choosing coincidence window of width 150ns.

PATH	DELAY (ns)
Cable length difference from RPC-DAQ board to LTM : 8m+4m = 12m	60
Track-length (diagonal-length for a volume of 4mx4mx1m) : 6m	20
Fan-out delay	20
Tolerance	20
Net relative delay between LTM inputs	**120**

Table 10. Maximum Relative delay between LTM input signals for Scheme B

2.2.1. GTM Level

Maximum relative delay between different input signals for a GTM, incorporated in different stages of propagation of the trigger signal from the output of RPC-DAQ board up to the input of GTM, is shown in table 11 and coincidence window of width 250ns seems to be acceptable without going for any delay compensation for the GTM input signals.

PATH	DELAY (ns)
Cable length difference from RPC-DAQ board to LTM for different LTMs : 4m+12m+4m = 20m	100
Cable length difference from LTM output to GTM input : 12m	60
Tolerance	50
Net relative delay between GTM inputs	**210**

Table 11. Maximum Relative delay between GTM input signals for Scheme B