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TIFR, July 2010

Readout Procedure for TPH monitoring System

For convenience, the various mnemonics are reproduced below from Pg 7 of AD7923 datasheet.

Pin No.	Mnemonic	Function
1	SCLK	Serial Clock. Logic Input. SCLK provides the serial clock for accessing data for the part. This clock input is also used as the clock source for the AD7923 conversion process.
2	DIN	Data In. Logic Input. Data to be written to the control register is provided on this input and is clocked into the register on the falling edge of SCLK (see the Control Register Descriptions section).
3	CS	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7923 and framing the serial data transfer.
4, 8, 13, 16	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7923. All analog input signals and any external reference signal should be referred to this AGND voltage. All AGND pins should be connected together.
5, 6	AVDD	Analog Power Supply Input. The AVDDrange for the AD7923 is from 2.7V to 5.25V. For the 0V to 2 × REFINrange, AVDDshould be from 4.75V to 5.25V.
7	REFIN	Reference Input for the AD7923. An external reference must be applied to this input. The voltage range for the external reference is 2.5 V ± 1% for specified performance.
12 to 9	VIN0 to VIN3	Analog Input 0 through Analog Input 3. Four single-ended analog input channels that are multiplexed into the on-chip track-and-hold. The analog input channel to be converted is selected by using the Address Bits ADD1 and ADD0 of the control register. The address bits in conjunction with the SEQ1 and SEQ0 bits allow the sequencer to be programmed. The input range for all input channels can extend from 0 V to REFIN or from 0V to 2 × REFINas selected via the range bit in the control register. Any unused input channels must be connected to AGND to avoid noise pickup.
14	DOUT	Data Out. Logic Output. The conversion result from the AD7923 is provided on this output pin as a serial data stream. The AD7923 serial data stream consists of two leading 0s, and two address bits indicating which channel the conversion result corresponds to, followed by 12 bits of conversion data, MSB first. The output coding can be selected as straight binary or twos complement via the coding bit in the control register. The data bits are clocked out of the AD7923 on the SCLK falling edge.
15	VDRIVE	Logic Power Supply Input. The voltage supplied at this pin determines at which voltage the serial interface operates.

Of these, only SClk, CSbar, Din and Dout are used to communicate with the MCU.

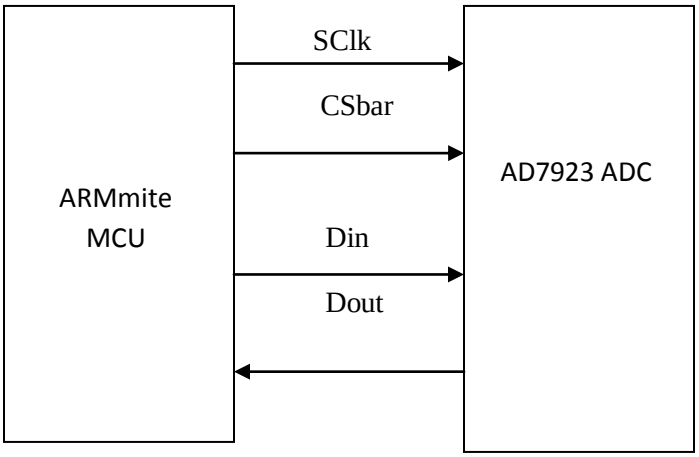
Readout is done in two stages:

1) Initialization stage. Here we configure the ADC for the readout by loading the control register with the required bits. For this stage, Din is sent in from MCU to the ADC, and Dout is ignored.
2) Readout Stage. Here we transfer ADC readings from the ADC. Din is kept low, which causes the ADC to ignore it; and Dout values are loaded.

In both cases, the process starts with CSbar, Sclk, Din set high. CSbar is then dropped low to initiate a conversion (which we will ignore for initialization) and also initiate a data transfer to/from the ADC. At the end of the data transfer CSbar is again set to high.

SClk alternates between high and low, and data is transferred at the high to low transition. To allow time for signals to stabilize, for initialization the MCU sets Dout on the preceding low to high transition; and for readout, the MCU reads Dout at the following low to high transition.

16 clock cycles are required to complete the transfer. As seen from the timing diagram of the AD7923 (Page 24, normal mode operation, Fig 20), Dout is zero for the first two of the bits, followed by the channel number for the next two bits, and twelve bits of data.



The timings diagram for our particular readout system is as below. The MCU use a one microsecond delay to control timing, so one clock cycle is 2μsec (1μsec high, 1μsec low).

The initialization diagram shows the Din values as currently sent. As Dout is ignored, it is not shown.

The readout diagram shows the times at which Dout transitions. The actual bits vary, thus both possible values are shown for each cycle. As Din is ignored, it is not shown

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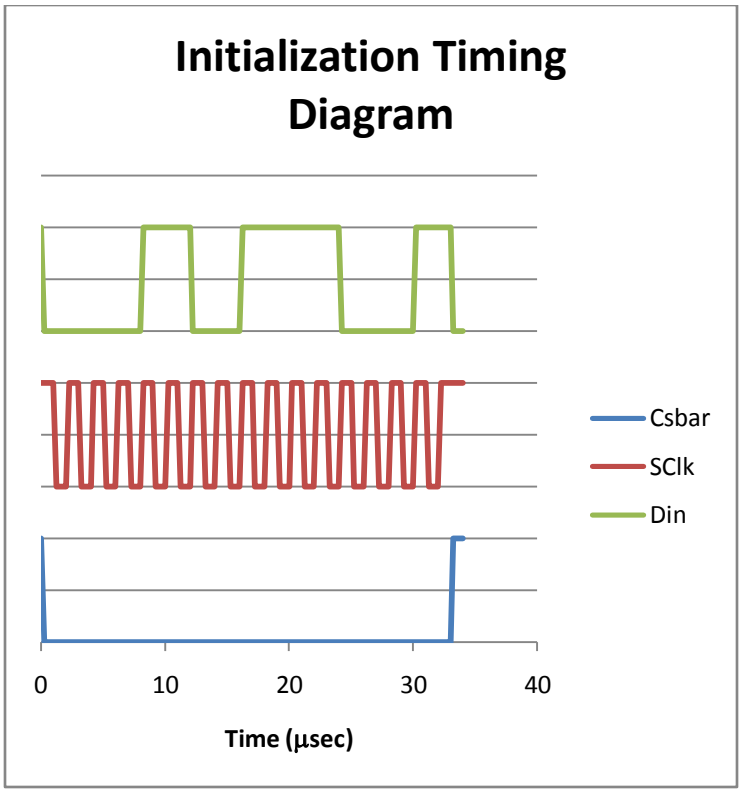
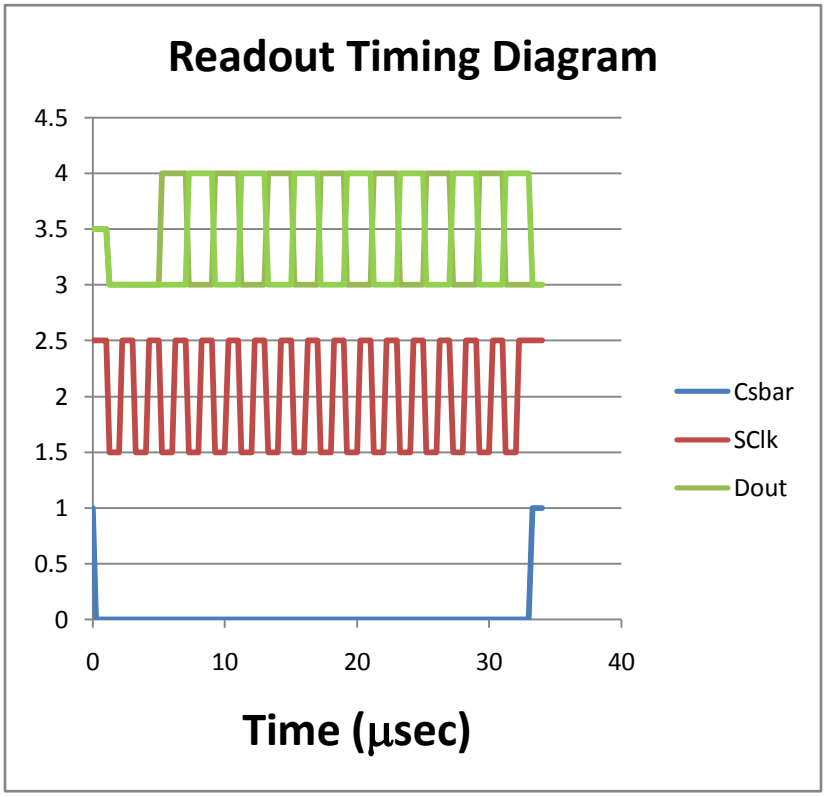




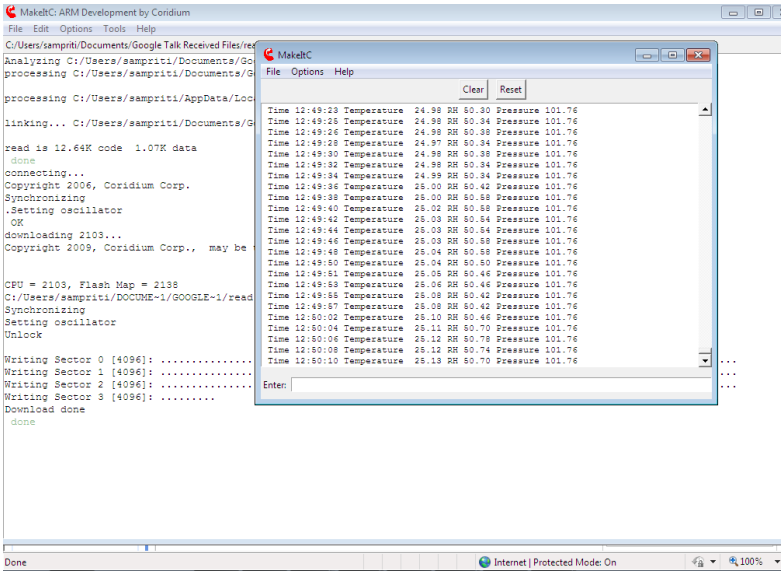
For setting the control register, the following table (as referred from datasheet of AD7923 Page 12) is to be used:

Bit	Name	Description
11	WRITE	The value written to this bit of the control register determines whether the following 11 bits are loaded to the control register. If this bit is a 1, the following 11 bits are written to the control register. If it is a 0, the remaining 11 bits are not loaded to the control register and it remains unchanged.
10	SEQ1	The SEQ1 bit in the control register is used with the SEQ0 bit to control the use of the sequencer function (see Table 9).
7–6	ADD1 ADD0	These two address bits are loaded at the end of the present conversion and select which analog input channel is converted in the next serial transfer, or they can also be used to select the final channel in a consecutive sequence, as described in Table 9. The selected input channel is decoded, as shown in Table 7. The next channel to be converted on is selected by the mux on the 14th SCLK falling edge. Channel address bits corresponding to the conversion result are also output on the DOUT serial data stream prior to the 12 bits of data (see the Serial Interface section).
5, 4	PM1 PM0	Power management bits. These two bits decode the mode of operation of the AD7923, as shown in Table 8.
3	SEQ0	The SEQ0 bit in the control register is used with the SEQ1 bit to control the use of the sequencer function. (See Table 9).
2, 9–8	DONTC	Don't care.
1	RANGE	This bit selects the analog input range to be used on the AD7923. If it is set to 0, the analog input range extends from 0 V to 2 × REFIN. If it is set to 1, the analog input range extends from 0 V to REFIN (for the next conversion). For the 0 V to 2 × REFIN range, AVDD = 4.75 V to 5.25 V.
0	CODING	This bit selects the type of output coding the AD7923 uses for the conversion result. If this bit is set to 0, the output coding for the part is twos complement. If this bit is set to 1, the output coding from the part is straight binary (for the next conversion).

For our program, the control register data is as follows: Bits 11, 10, 7, 6, 5, 4, 3, and 0 are on. Rest are 0. This explains our Din during initialization process. The program feeds in the bits by shifting bits already loaded to the left. The first part of the program deals with initialization, second is conversion of data output and finally readout on the Terminal Screen

.In this respect, it is useful to mention the procedure of start up and running our present MCU device in order to readout the data. The FRC cable should be used connection the TPH board with the MCU board. The "Make it C" is started in the PC. From the tab File →Choose main→Read.c (it is saved on Desktop). Next, go to Serial port and check if the right communication port is selected. Then go to Tools→Build

and Run. If the building is successful, a pop up message appears saying “C program is now running”. Click OK. And go to Tools→Terminal. You should see the Readout Window as below. If you are working on debugging mode, types Yes in the Tcl window, else type No or just hit return. Debugging allows quick readouts whereas normal mode would give a single readout per minute. This can be changed in the program. Please enter the present hour and minutes at the start up, so that the data in Tcl window appears corresponding to time.



Important References for Readout

Datasheet of AD7923; Link: http://www.analog.com/static/imported-files/data_sheets/AD7923.pdf.

ARMexpress GCC help files: http://www.coridiumcorp.com/Support.php

Refer to documentation on “A Low Cost High precision Temperature Pressure Humidity monitoring system for INO detector” by Sampriti Bhattacharyya for further details on the system.