# MEASUREMENT OF MUON LIFE TIME USING COSMIC RAY MUONS STOPPED IN A PLASTIC SCINTILLATOR DETECTOR

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1.INTRODUCTION

Leptons are a class of fundamental building blocks of matter as proposed by the Standard Model of Particle Physics. There are three generations of leptons with the electron and electron neutrino(1st generation), muon and muon neutrino (2nd generation) and tau and tau neutrino (3rd generation). These are all fermions with spin ½, and all particles other than neutrinos carry one unit of negative charge, where as the corresponding anti-particles carry one unit of positive charge.

Muon has a mass of 105.66MeV/c^2 and interact only via weak and electromagnetic interactions. Due to this large mass, it is unstable.While passing through matter it can undergo either of the following interactions: capture of muon by nuclei or spontaneous decay as follows, which is a weak decay:

$$\mu^- \rightarrow e^- + \nu_\mu + \bar{\nu}_e$$
$$\mu^+ \rightarrow e^+ + \bar{\nu}_\mu + \nu_e \qquad (1)$$
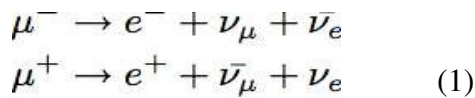
The later decay is made use of in doing this experiment, since a plastic scintillator (hydrocarbon) and since the muon capturing probability is small for low Z materials. Muon decay times are distributed as follows:

$$N(t) = N(0)\exp(-t/\tau) \quad (2),$$

where, N (0) = initial population of muons,
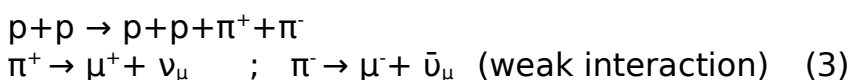
  N(t) = remaining muons at time t,

  τ = the muon life time.

This expression is the same as for the general radioactive decays of nuclei and decays of all unstable elementary particles. Muon life time ahs been measured accurately as, $\tau = 2.19703$ μs.

2.COSMIC RAY MUONS

Secondary cosmic rays are used as the source of muons in this experiment. The total secondary flux at the ground level, consists of 75% muons (+ve and -ve) and 25% electrons (e$^+$ and e$^-$). Muon flux at sea level is 1cm^{-2}min^{-1}.

Cosmic rays are high-energy particles that fall on the earth from the space. Primary cosmic rays consist of protons(by far the highest proportion), electrons,positrons,neutrinos,and gamma ray photons of very high energies ranging from 10^8 eV to 10^{20} eV. On entering the earth's atmosphere, they collide with oxygen and nitrogen nuclei producing secondary cosmic rays, consisting mainly of elementary particles and gamma-ray photons. A single high energy particle can produce a large shower of secondary particles. The reactions leading to the production of cosmic ray muons are as follows:

$$p+p \rightarrow p+p+\pi^+ +\pi^-$$
$$\pi^+ \rightarrow \mu^+ + \nu_\mu \quad ; \quad \pi^- \rightarrow \mu^- + \bar{\nu}_\mu \text{ (weak interaction)} \quad (3)$$

$$\pi^0 \rightarrow 2\gamma \text{ (electromagnetic interaction)}$$

The spontaneous decay of muon is as follows:

$$\mu^- \rightarrow e^- + \bar{\nu}_e + \nu_\mu \quad ; \quad \mu^+ \rightarrow e^+ + \bar{\nu}_\mu + \nu_e \qquad (4)$$
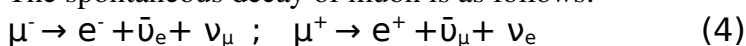
Muon decay time has been calculated accurately as τ =2.19704 μs. Lets say that muon life time is approximately 2.2 μs. This is the value as measured in a reference frame at rest wrt the muon. Using Newtonian mechanics, if the muons travel with velocity ~ c, then they should travel approximately 660m after their creation and should not be detected at the ground level. Only relativistic time dialation can explain the detection of muons at the ground level. By the Lorentz transformation equation,

$$t = t' / \sqrt{\left(1 - v^2/c^2\right)} = \gamma t' \quad (5)$$

t=time measured in the lab system
t'=time measured in the rest frame of the system
v=velocity of the system
c=speed of light
For v~0.99c, γ=7.08, τ =2.2 μs, γτ = 15.58 μs is the life time of muons, relative to an observer on earth. So the average distance travelled by muons as measured by an observer on earth :
 d = γτv = 15.58 X 10^{-6} X 0.99 X 3 X 10^8 m = 4.627km.

3.EXPERIMENTAL SETUP

 Fig.2.Block diagram representing the experimental setup
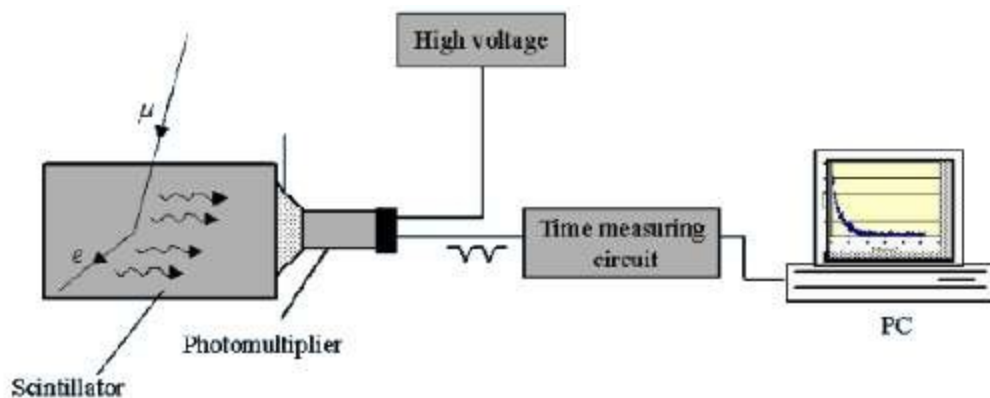
The components of this set up are a plastic scintillator, photomultiplier tube (PMT), a time measuring circuit and a PC.Photo tubes are used to guide the scintillator signals to the PMT.

3.1.PLASTIC SCINTILLATOR : A scintillator is a type of particle detector in which a flash of light (scintillation),
usually in the near blue or below UV region of electromagnetic spectrum, is emitted

when an excited atom returns to its ground state, having been excited by a photon or a charged
particle. The relaxing period of the scintillator is very short with a typical decay time

of the order of nano seconds. Refractive index of the scintillator material should be near to that of glass(~1.5) to permit efficient coupling of
scintillation light to a photomultiplier tube or other light detector.

A plastic scintillator of refractive index 1.58 and dimensions (24 cm X 24 cm X 14.5 cm) , (wrapped first by white tyrek paper to avoid the scintillation light from escaping out, and then by black tedler paper to avoid external light form entering into the detector) is the muon detector used here.

3.2.PHOTOMULTIPLIER TUBE (PMT):The light output of a scintillator is converted into electrical signals and amplified
using a photomultiplier tube (PMT).
A typical photomultiplier tube consists of a
photoemissive cathode (photocathode) followed by focusing electrodes , an electron multiplier (with dynodes) and an electron collector (anode) in a vacuum tube.
A PMT is shown in Fig.3.

Fig.3.Structure of a photo multiplier tube.
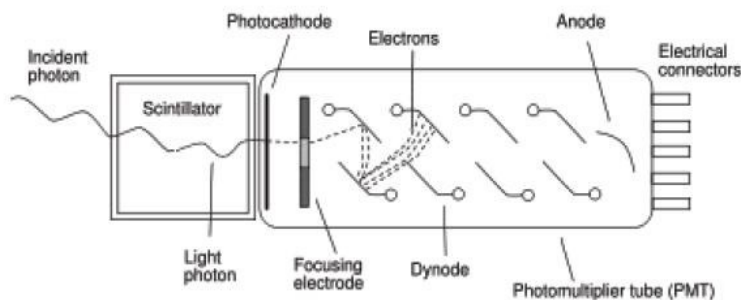
When light enters the
photocathode, the photocathode emits photoelectrons into the vacuum. The number of electrons produced is determined by the quantum efficiency of the photocathode and the number of electrons thus produced is very small. The signal produced by the photo cathode is then focused on dynodes, where secondary emission of electrons proportional to the incident electron energy takes place. The final charges are accumulated and collected at the anode which gives rise to a sharp and strong electrical output. Because of secondary emission multiplication, photomultiplier tubes provide extremely high sensitivity and exceptionally low noise.

The overall spectral response, i.e., the sensitivity of the photocathode is expressed in

terms of quantum efficiency, Q.E.,

Q.E. = (no:of photoelectrons emitted) / (no:of incident photons on the photocathode)
 (6)

For ideal photocathode, Q.E. = 100%, but practically it is 20 – 30%.It is a strong
 function of the wavelength of the incident light and the photocathode
 material.

 The efficiency of a dynode is determined by the overall multiplication factor (δ),

δ = (no:of emitted secondary electrons) / (no:of incident primary electrons) (7)

A 2 inch diameter PMT, with a 21 pin base (9807B, manufactured by Electron Tubes Ltd) , operated at a high voltage of about 1.7 kV by means of high voltage dc to dc converter (E20-HVDCDC) was used for this experiment.The rise time of the pulse obtained is a few nanoseconds.

3.3.TIME MEASUREMENT CIRCUIT: A stopped muon decaying inside a scintillator gives rise to two signals; one due to itself and the other due to the electron into which it decays. The time measurement circuit is used to determine the delay between the two signals and then it is passed to a PC.
PMT pulse: When the muon passes through the detector, it produces a light signal, which is fed to a PMT, to produce a negative analog pulse. The decay electron also gives a similar pulse, but of smaller height. The two pulses are shown in Fig.4.

Fig.4. PMT pulses. Note the deeper pulse for muon.
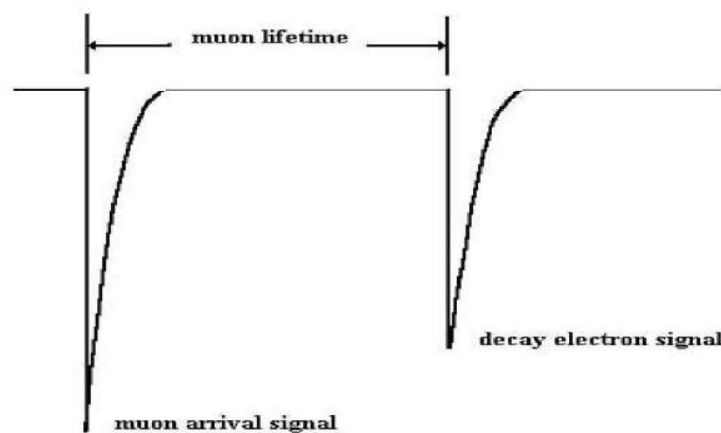
The time difference between the entering of a muon into the detector and its decay into the subsequent products should be measured. For this a 'clock' is needed. The electronic circuit designed for this purpose is shown in Fig.5.

Fig.5. Time measurement circuit (top one). The 2 circuits at the bottom of the figure are the voltage regulators for providing voltages to IC's (+5V and -5V) and PMT base (rated 1.65 kV)
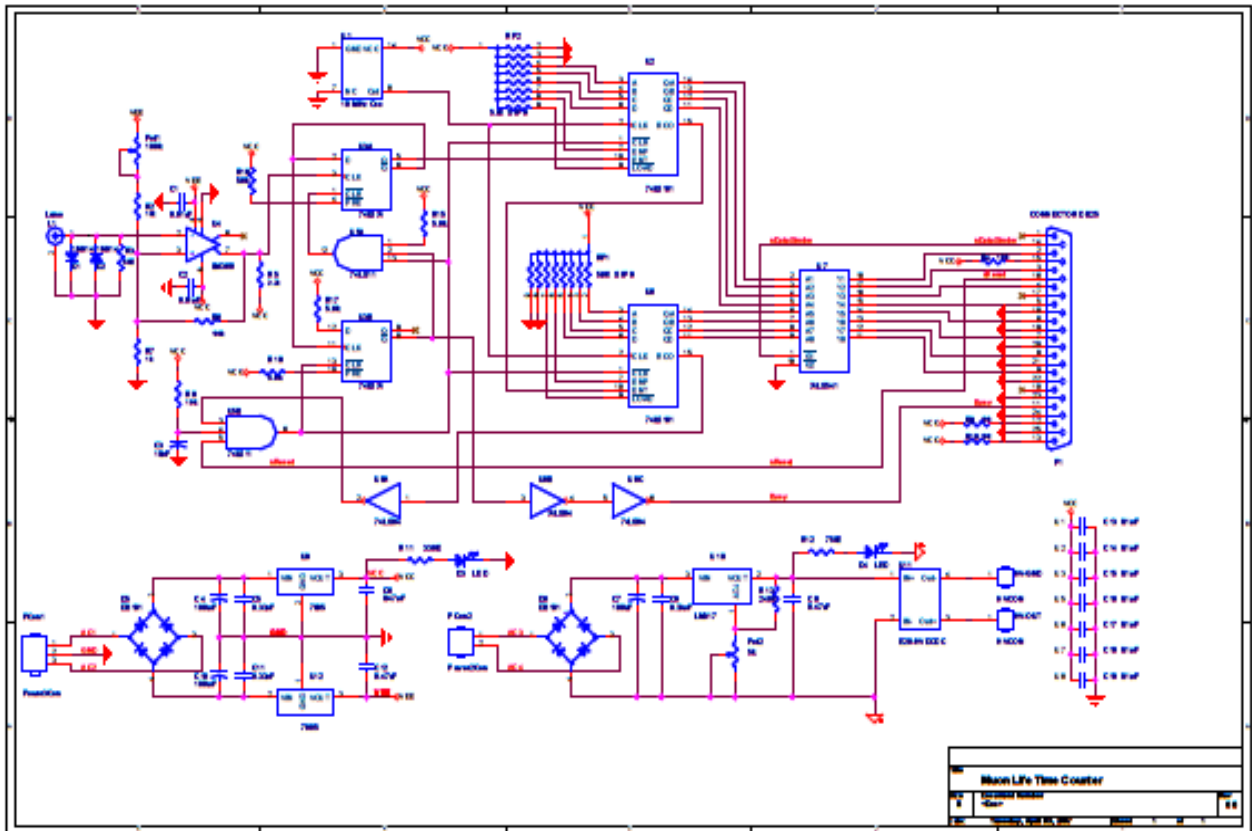
The main components of this circuit are the following:
a) Comparator b) Flip-flops c) Counters d) Oscillator e) Latches f) a buffer IC and
g) a standard Parallel Port interfacing with the computer where the data is recorded.
The names and uses of the different ICs used in this circuit are listed in the following table.
Table.1.ICs (A description of these ICs is given in the appendix.)

IC name	Description
LM360 (8 PINS)	COMPARATOR
74LS74 (14 PINS)	D-FLIP FLOP
74LS161 (16 PINS)	COUNTER
74LS541 (20 PINS)	BUFFER
74LS11 (14 PINS)	AND GATE
74LS04 (14 PINS)	NOT GATE
7805 (3PINS)	POSITIVE VOLTAGE REGULATOR
7905 (3 PINS)	NEGATIVE VOLTAGE REGULATOR
LM317	POSITIVE VOLTAGE REGULATOR
DB103 (4 PINS)	BRIDGE RECTIFIER

A CRYSTAL OSCILLATOR (4 PINS) of frequency 10 MHz is used to generate the clock for both

LSB and USB counters, thus giving the resolution of 0.1μs.
The working of this circuit is described below:
 The small light pulse produced when a muon stops in the sintillator is detected and ampified by the PMT, the output of which is fed to a comparator. The comparator acts as a noise filter, which will allow only sigals with amplitudes greater than a certain threshold value to pass through. Once there is a signal at the comparator output, it starts a counter, which counts at a rate of 10MHz, giving a resolution of 0.1μs. If a second pulse from a decaying muon arrives soon after the first, the counter is stoped and the PC is signalled that the data is to be read. The PC, after reading the data, resets the circuit ready for more decays. If there's is no second pulse following the first pulse after a certain period, the circuit resets itself and waits for the second pulse to come.

The LM360 high speed comparator is the first stage of the electronic circuit. A potential divider is used to set the threshold for the comparator. The comparator filters out noise by allowing only those

signals which have a voltage higher than the reference voltage, of 42mV, set at the non-inverting terminal of the IC,to generate a high logic pulse. The output of the comparator is a positive high (the negative input signal is fed to the inverting terminal)
 digital pulse (TTL) of 5 Volts.
 This pulse acts as the clock of the first D-F/F.
          Two flip-flops are used in this circuit. In the cleared state, the Q o/p is low and Q' o/p is high. Q' o/p of the 1st F/F is connected to its D-i/p. when the clock comes, Q goes high and Q' goes low. The positive high o/p of the LM360 comparator acts as the clock for the 1st F/F. When the clock is present, the Q o/p of the 1st F/F goes high, goes to the ENT of the 1st 4-bit synchronous counter and starts counting at 10MHz. The Q' o/p goes low and is fed to the clock of the 2nd F/F. Since the clock is low, Q o/p of 2nd F/F is low and its Q' o/p is high.

     There are two cases.
Case 1: Muon decays into an electron

  When a muon decays into an electron, a 2nd pulse comes from the PMT and passes through the comparator soon after the first. Now, the 1st F/F's Q o/p goes low and stops the counter. Meanwhile the Q' o/p, which is the clock of the 2nd F/F, goes high, making the Q o/p of the 2nd F/F high and its Q' o/p low. This low Q' o/p clears the 1st F/F as well as the counter. The low Q' is read as the time when the data from the buffer (IC-74LS541) is to be read by the interfacing program. Q' after buffering is sent to the BUSY pin of the PC parallel port. On receiving the BUSY signal, the DATA_STROBE is pulled low to enable the data buffer, which passes the count from the counter to the PC, which reads the data. After reading data, the DATA_STROBE line goes high and the RESET line is pulled low for a few microseconds. This clears the F/F back to the waiting state and the counter is ready for the next PMT signal.

Case 2: Muon doesn't decay into an electron

 The counter will count upto 255, ie. if a second pulse is not received within
25.5μs, the RCO (Ripple Carry Output) goes high. This is inverted to clear the counter and the F/Fs, to wait for the next PMT pulse.

DATA ANALYSIS
     Data analysis requires fitting of the data with appropriate functions. Measured quantity is the

time lag between the start event and stop event. For time distribution, tha data is sampled, events binned and then fitted. A correction for background events is needed, since there are background sources like other radioactive sources, light leakage through the scintillator or a muon decaying before the decay of the previous one. The background events which are produced due to start from

one muon and stop from another one will be very small as the flux reaching down at sea level is very small
when compared to the 25.5μsecs window used for counting.
The background for the data is assumed to be constant over a
period of time. Then, the function
    $N(t) = N_0 \exp(-t/\tau) + b$ (8)
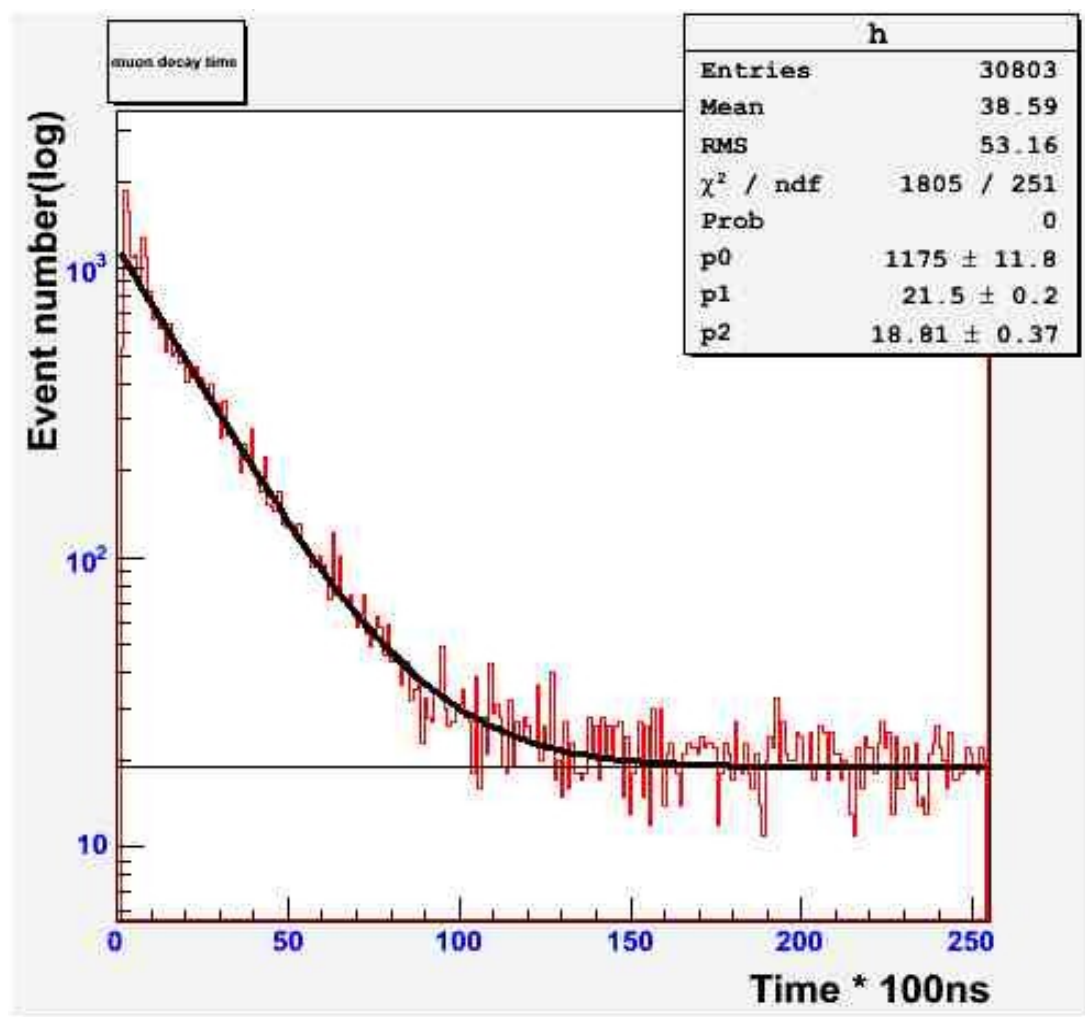is fitted using ROOT. The fitting parameters obtained are:

Fig 6: Log of event number vs time. Straight line gives the background.

NO.	NAME	VALUE	ERROR	SIZE	DERIVATIVE
1	p0	1.17507e+03	1.17805e+01	-1.63446e-03	1.03881e-07
2	p1	2.14951e+01	1.81382e-01	2.34723e-05	-1.04836e-05
3	p2	1.88115e+01	3.71917e-01	1.20655e-05	-4.29021e-06

        b = 18.8115
The fitted parameters are obtained as:
N(0) = 1175.07 ± 11.78

τ = (21.49 ± 0.18) X 100ns ~ (21.5 ± 0.2) x 100ns
b = 18.81 ± 0.37

So, the mean muon life time is determined approximately as, *(2.15 ± 0.02)μs*.

FERMI COUPLING CONSTANT

The universal constants for a process provides a tool to validate experimental results. The muon decay is an
electroweak process and the coupling constant is the Fermi Coupling constant (G). In the theory of muon
decay the expression for average life time of muon is expressed as

$$\tau = (192\pi^3) / (G^2 m_\mu^5) \quad (9)$$

Substituting the value of τ obtained from this experiment, in this equation, the value of Fermi coupling constant is obtained as:

$G_F = 1.1753 \times 10^{-5} (GeV)^{-2}$

Here, the conversion relation $1 GeV^{-1} = 6.58 \times 10^{-25} s$, has been used.

APPENDIX I : ELECTRONIC COMPONENTS

LM360 : It is an 8-pin configuration IC with a very high speed differential input, complementary TTL output voltage
comparator which has been optimized for greater speed, input impedance and fan-out, and lower input
offset voltage. Typically delay varies only 3 ns for overdrive variations of 5 mV to 400 mV.

  The connection diagram is shown in metal can package and dual-in line
package.

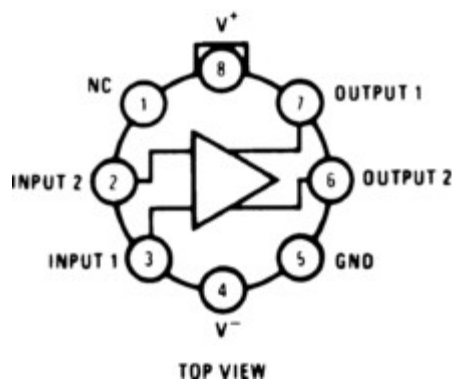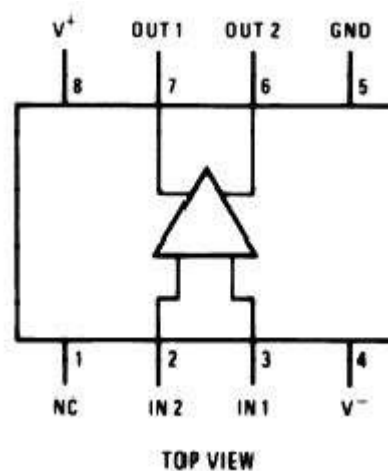Fig I: Metal Can Package   Fig II: Dual-In-Line Package

Features of LM360:

- Tight delay matching on both outputs
- Guaranteed high speed: 20 ns max
- Complementary TTL outputs
- High input impedance
- Low speed variation with overdrive variation
- Fan-out of 4
- Low input offset voltage
- Series 74 TTL compatible
- Positive Supply Voltage : +8V
- Negative Supply Voltage: −8V
- Peak Output Current   20 mA
- Differential Input Voltage ±5V
- Input Voltage   V+ ≥VIN≥ V−
- Operating Temperature Range 0°C to +70°C
- Storage temperature range -65°C to +150°C

74LS74 : A dual edge triggered flip-flop that utilizes Schottky TTL circuitry to produce high speed
D-type flip – flops. Each flip-flop has individual clear and set inputs,and also complementary Q

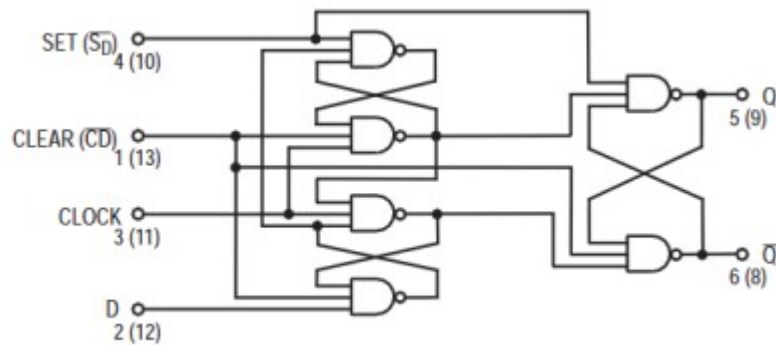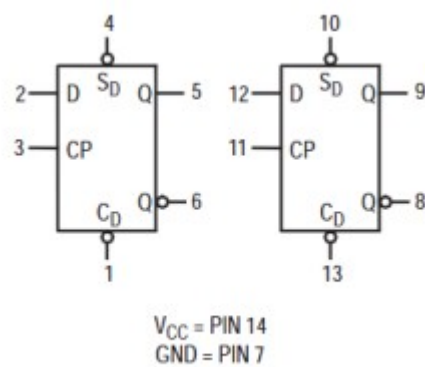and Q' outputs.

Fig III: Logic diagram(Individual Flip-Flop)

Fig 1V: Logic symbol

V_{CC} = PIN 14
GND = PIN 7

The information at the D i/p is transferred to the Q o/p on the +ve going edge of the clock pulse.Clock
 trigering occurs at a particular voltage level of the clock pulse and is not directly related to the transition time of the
 +ve going pulse.When the clock i/p is either at HIGH or LOW level,the D input signal has no effect.
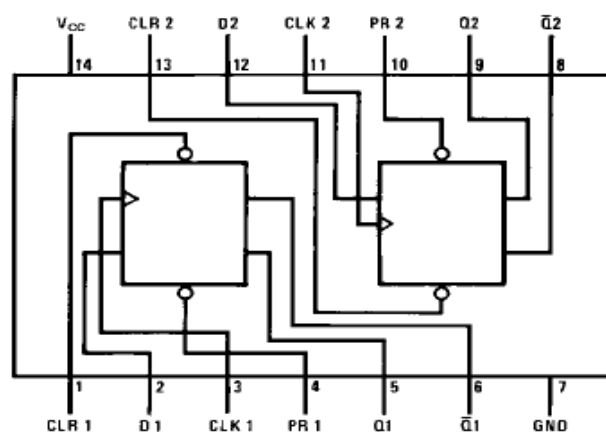
Fig V: Connection diagram

Fig VI : Truth table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q_0}$

where,

X = LOW or HIGH Logic Level

H = HIGH Logic Level

L = LOW Logic Level

↑ = Positive-going Transition

Q_0 = The output logic level of Q before the indicated i/p conditions were established.

Note: This configuration is unstable, i.e. it will not persist when either the preset and/or clear inputs

return to their inactive (HIGH) level.

74LS161: Ahigh speed 4-bit synchronous counter with 16 pin configuration.

Fig VII: 74LS161- Connection diagram
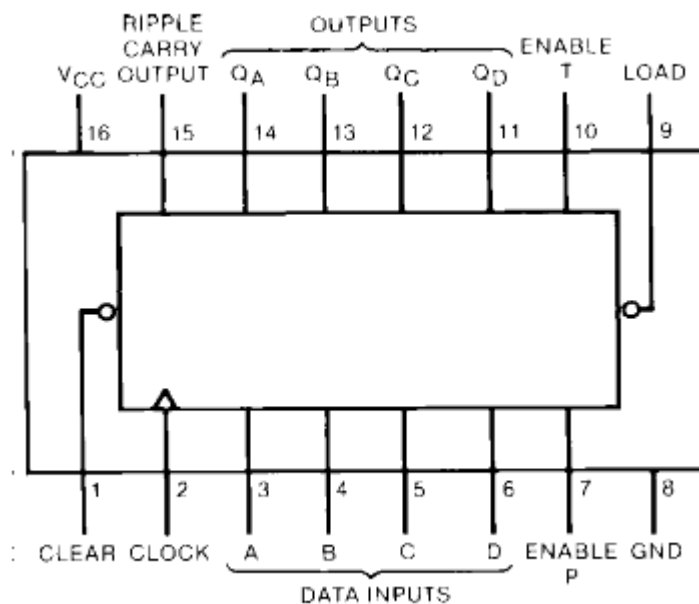
The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal

counting mode of operation. Synchronous operation is provided by having all flip-flops clocked

simultaneously, so that the outputs change coincidently with each other, when so
instructed by the count-enable inputs and internal gating.

A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input
waveform. These counters are fully programmable, i.e. the outputs may be preset to either level. As
presetting is synchronous,setting up a low level at the load input disables the counter and causes the outputs
to agree with the setup data after the next clock pulse, regardless of the levels of the enable input. The clear
function for the DM74LS161A is asynchronous. A low level at the clear input sets all four of the flip-
flop outputs LOW, regardless of the levels of clock,load, or enable inputs.

The carry look-ahead circuitry provides cascading for counters for n-bit synchronous applications

without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a
ripple carry output. Both count-enable inputs (P and T) must be HIGH to count,and input T is fed forward
to enable the ripple carry output.The ripple carry output thus enabled will produce a highlevel output pulse
with a duration approximately equal to the high-level portion of the QA output. This high-level overflow
ripple carry pulse can be used to enable successive cascaded stages. HIGH-to-LOW level transitions at the
enable P or T inputs may occur, regardless of the logic level of the clock.

Table I: Guaranteed Operating Ranges

Parameter	Symbol	Min	Type	Max	Unit
Supply Voltage	Vcc	4.75	5	5.25	V
Operating Ambient		0	2.5	70	^{0}C

Temperature range	T_A				
Output current High	I_{OH}			- 0.4	mA
Output current Low	I_{OL}			8	mA

74LS541: An octal buffer with 20 pin configuration.It takes 4 bit output from each counter and

gives 8 bit output to the PC.
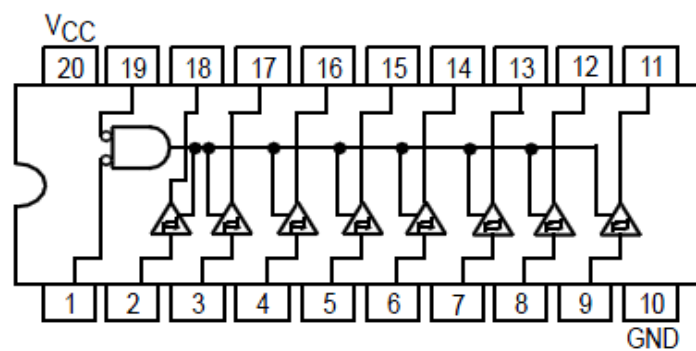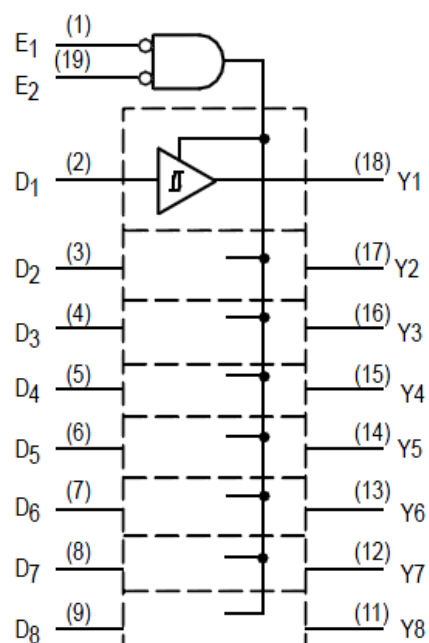
Fig VIII: Connection diagram

Fig IX: Logic diagram

Fig X: Truth table

INPUTS			OUTPUTS
E$_1$	E$_2$	D	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance

74LS11:A 14 pin configuration IC consisting of triple three-input AND gates.
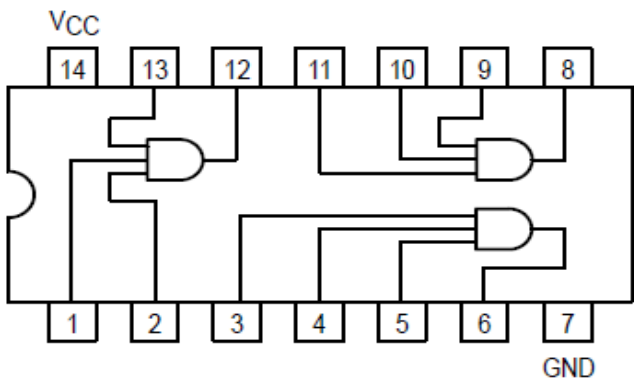Fig XI: Pin diagram

Fig XII: Truth table

Y = ABC

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = HIGH Logic Level

L = LOW Logic Level

X = Either LOW or HIGH Logic Level

Table II: Features

Symbol	Parameter	Min	Nom	Max	Unit
Vcc	Supply Voltage	4.75	5	5.25	V
T_A	Operating Ambient Temperature Range	0		70	^{0}C
I_{OH}	Output current - High			-0.4	mA
I_{OL}	Output current-Low			8	mA
V_{IH}	Input Voltage-High	2			V
V_{IL}	Input Voltage-Low			0.8	V
V_{OH}	Output Voltage - High	2.7			V
V_{OL}	Output Voltage-Low			0.5	V
I_{IH}	Input High Current			0.1	mA
I_{IL}	Input Low Current			-0.4	mA

74LS04: A triple 3-input AND gate with 14 pins.

Fig XIII: Connection diagram
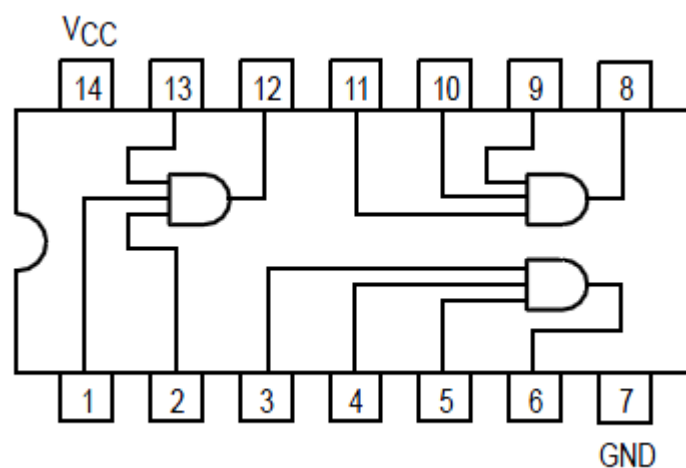
7805 : It is a three terminal 1A positive voltage regulator which employs internal current limiting, thermal
 shut down and safe operating area protection,making it essentially indestructible. If adequate heat sinking is
 provided, they can deliver over 1A output current.

Table III:Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Input voltage (for V_0 =5V to 18V)	V_I	35	V
Input voltage (for V_0 =24V)	V_I	40	V
Thermal Resistance Junction Cases (T O 220)	$R_{\theta JC}$	5	^{0}C/W
Thermal Resistance JunctionAir (TO220)	$R_{\theta JC}$	65	^{0}C/W
Operating Temperature Range (KA78XX)	T_{OPR}	0 ~ +125	^{0}C
Storage Temperature Range	T_{STG}	65 ~ +150	^{0}C

7905
: It is a three terminal negative voltage regulator with thermal overload
 protection and short circuit protection.

Table IV: Absolute maximum ratings

Parameter	Symbol	Value	Unit
Input voltage (for V_0 =5V to 18V)	V_I	-35	V
Input voltage (for V_0 =20V,24V)	V_I	-40	V
Output Current	I_{OUT}	Internally limited	
Power Dissipation	P_O	Internally limited	W
Operating Temperature	T_{OPR}	0 ~ 150	^{0}C

Range (KA78XX)			
Storage Temperature Range	T_{STG}	65 ~ +150	^0C

LM317

: An adjustible three terminal positive voltage regulator designed to supply more than 1.5A of load current with an output voltage adjustible over 1.2 to 37V. It employs internal current limiting, thermal shutdown and safe area compensation.

Table V: Absolute maximum ratings

Parameter	Symbol	Value	Unit
Input output Voltage: Differential	V_i V_o	40	V
Lead temperature	T_{lead}	230	^0C
Power dissipation	P_D	Internally limited	W
Operating junction temperature range	T_J	0- 125	^0C
Temperature coefficient of Output voltage	$\Delta V_0/\Delta T$	±0.02	%/ ^0C
Storage Temperature Range	T_{STG}	65 ~ +150	^0C