High Speed CMOS Comparator for INO Front-end Electronics: A Simulation Study

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Objective:

To design a fast CMOS ASIC comparator for detecting signals for Resistive Plate Chambers and providing TTL/CMOS compatible outputs.

Basic voltage comparator schematic:

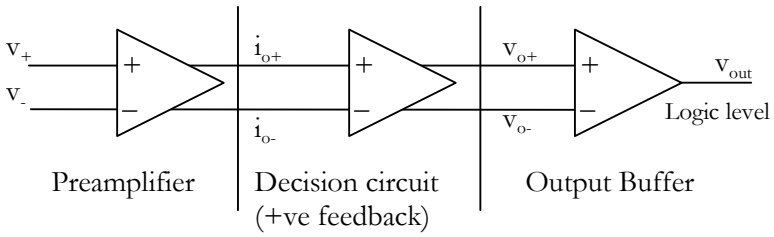

Fig. 1 Basic fast comparator schematic

- **The preamplifier**
  The preamplifier increases the input sensitivity and isolates the input side from the switching noise originating from the +ve feedback stage.

- **Positive feedback stage (decision making circuit)**
  This stage id used to determine which of the input signals is larger

- **Output buffer**
  The output buffer amplifies the information and outputs a corresponding digital signal.

Design Issues:

A typical RPC pulse shape is shown in Fig. 2. It is a –ve pulse with a amplitude of 50mV- 100mV with a HIGH – LOW transition time of 1ns and a LOW-HIGH transition time of 20ns. The comparator should be abele to output a TTL/CMOS compatible LOGIC signal in the presence of such a small pulse at the input. The comparator should therefore have HIGH GAIN with little DELAY and HIGH slew rate for driving off the chip load capacitance.

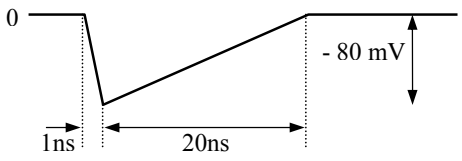

Fig. 2 Typical RPC signal shape

The architecture chosen is shown in Fig.2 below. The first stage is a low gain differential amplifier

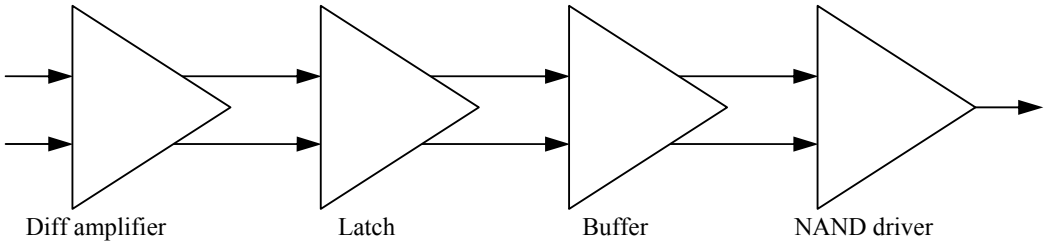

Fig. 3 Schematic representation of the simulated comparator

followed by a +ve feedback stage (latch). The last two stages buffer and NAND driver were included for providing high current for driving off the chip capacitive loads.

Specifications (simulated):

Technology	**SCL 1.2 µm CMOS N-well**
Power supply	**±2.5 V**
PSRR	**55 dB – 65 dB**
Average power consumption (idle)	**VDD =0.85 mW/ch** **VSS =0.85 mW/ch**
Peak power consumption (C_L=5pf)	**VDD = 100 mW/ch** **VSS = 140 mW/ch**
Voltage gain	**100 dB**
Input offset voltage	**= 80 µV** (typical)
Prop delay (Low-High) (C_L=5pf, overdrive= 40mv)	**6.5ns (typical)** (can be improved with higher overdrive)
Rise Time (Low-High)	**825 ps (typical)**
Fall Time (High- Low)	**625 ps (typical)**
Max. operating frequency (sinusoidal with C_L=5pf)	**150 MHz**

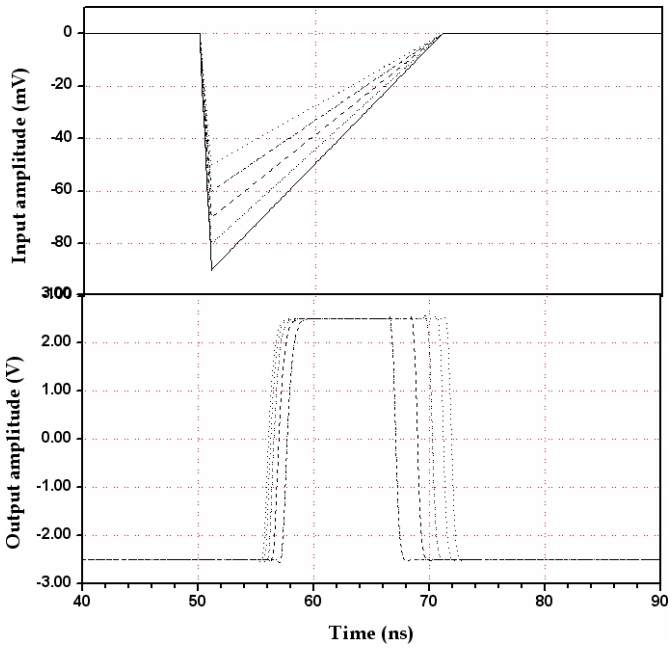

Fig. 4 Simulated transition delay for overdrive of 20mV, 30mV, 40mV, 50mV and 60mV

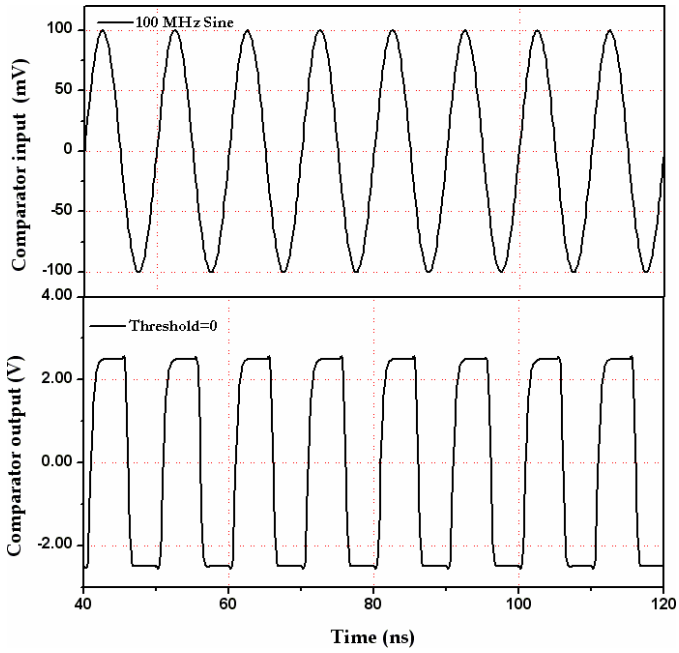

Fig. 5 Typical transient response of the comparator to a 100MHz sinusoidal input

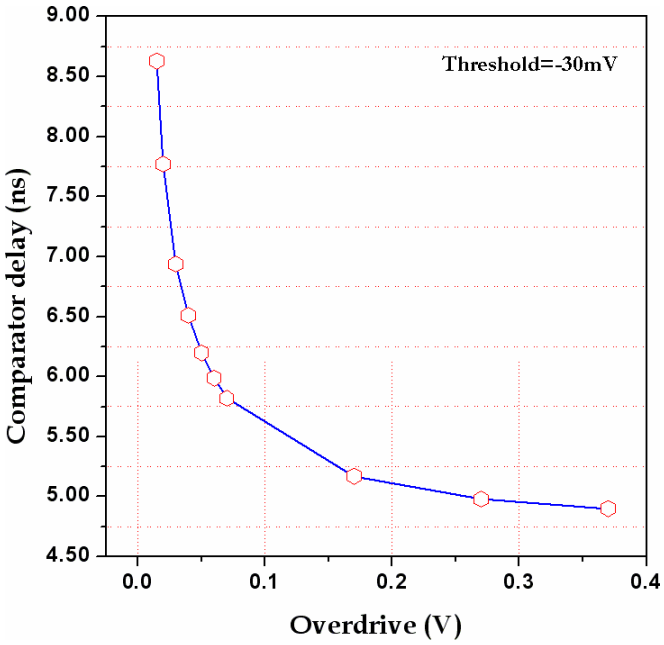

Fig. 6 Variation of propagation delay as a function of overdrive

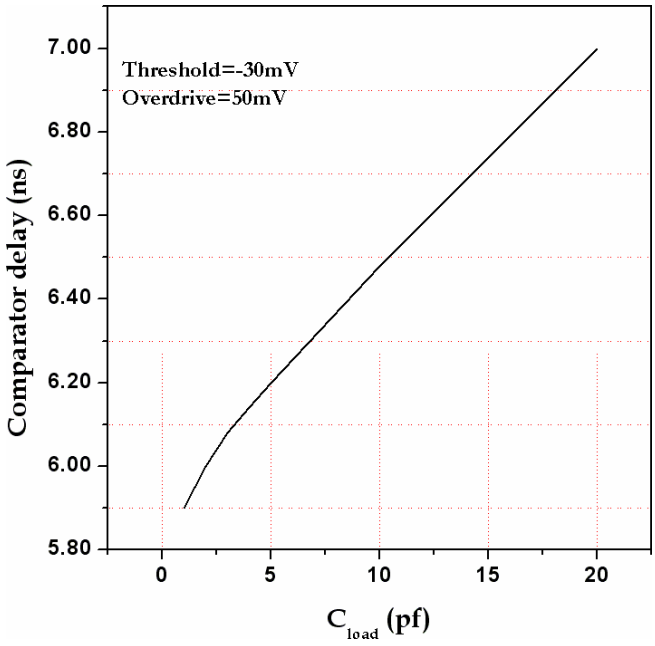

Fig. 7 Variation of propagation delay as a function of load capacitance

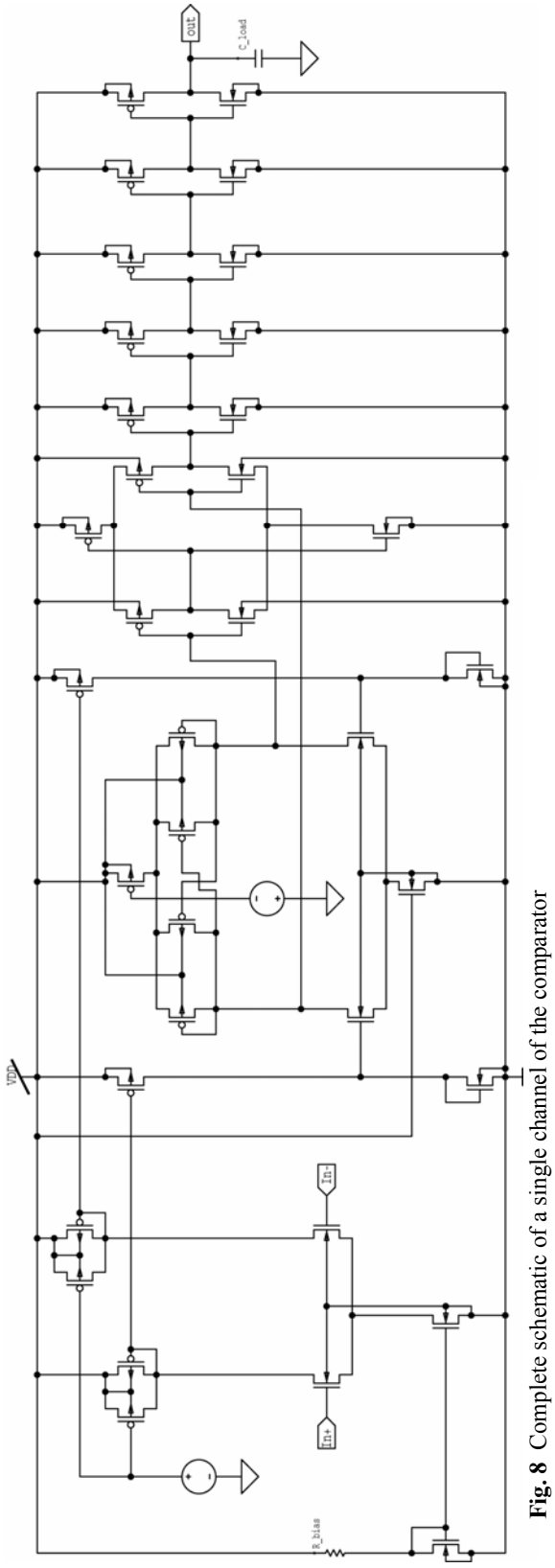

Fig. 8 Complete schematic of a single channel of the comparator