Specifications of the ICAL TDC device

Revision history:			
	Version 0.0	Created by B.Satyanarayana	May 26, 2011
	Version 0.1	Modified based on the feedback from the collaboration	June 5, 2011

Parameter	Specification
1. Number of channels	8 or 16
2. Least count	200ps
3. Dynamic range	2µs (essential), 32µs (desirable)
4. Number of bits	14 (essential), 18 (desirable)
5. Type	Common stop
6. Hits	Single hit (essential), multi hit (desirable)
7. Double hit resolution	5-10ns
8. Readout buffer size	128 words (maximum)
9. Signal and control inputs	LVDS and LVTTL respectively
10. DNL/INL	100ps (typical)
11. Power rail	3.0 to 3.6V (suggested)
12. Control and readout interface	SPI (essential), SPI + parallel (desirable)

Notes:

1. 128 channels (64 each from X & Y planes) are to be readout from an ICAL RPC. Groups of eight channels are ORed for the purpose of TDC readout. So, we need 8 TDC channels per plane. Depending on whether one DAQ board per RPC mounted on top of the RPC or two separate boards for two planes mounted near two corners of an RPC (preferred scheme at present), 16 or 8 channel devices will be preferred respectively.
2. This value is chosen based on the physics requirements as well as the RPC signal characteristics.
3. This value is essentially decided by the trigger latency, which in turn depends on the electronics processing time, integration issues of the trigger system and signal transmission delays. Current estimate of the trigger latency is about 1µs. This is based on the currently preferred scheme where segment trigger stations as well as the final trigger station are located on the detector face parallel to the RPC roads. 2µs is chosen as a safe value. A much higher dynamic range (32µs) is desirable for looking at some of the other physics signatures.
4. These values are arrived at based on the dynamic range and least count specifications.
5. In ICAL electronics architecture, trigger signal reaches the DAQ elements much later than the signal(s) from the hit channels. It is therefore natural (especially if it is a single hit TDC) in common stop mode.
6. Our studies have shown that on a TDC channel with a mean random counting rate of 50Hz (we do not know what the strip counting rate going to be underground), the fraction of multiple hit events with a 1µs pre-trigger window is about 0.01%, which is reasonably low. Based on this, one might conclude that a single hit type TDC might do

the job, even though more detailed studies are underway. But, it is desirable to have a multi hit TDC to be able to record the rising and falling edges (and hence the time-over-threshold width) of an un-stretched (leading edge) discriminator signals. This information could be very useful for (offline) time-walk correction of the timing data. In general, a multi hit TDC might be able to address future requirements of the detector better than the single hit type. Multi hit record capability of up to eight hits (both edges of four signals) should be adequate.

7. This is somewhat a generic specification, not strictly based on physics reasons.
8. This size is arrived at by considering a multi hit (8 hits) device supporting 16 inputs. For other designs, an appropriate size could be obtained.
9. In the current scheme of things, the discriminators produce LVDS signals, which are driven to the RPC-DAQ board. The TDC device receives these un-stretched signals through appropriate signal receivers/buffers. Therefore, it is preferred to have the inputs designed on LVDS. It is suggested that we follow LVTTL logic for the control signals, in order to minimise the power consumption.
10. This specification is gleaned from literature.
11. This specification is suggested in keeping in view of the power supply requirement of other devices on the RPC-DAQ board. However, even other voltage rails, especially lower than these can be easily accommodated.
12. It is planned to interface all the functional devices on the RPC-DAQ board with on-board controller on SPI bus (essential). But, having the parallel interface in addition will provide flexibility to interface the TDC chip with other type of controllers or designs (desirable). However, it was felt many collaborators that it is better do away with parallel interface in order to reduce the pins and save power.