Proposed Frontend Chip for INO
(DRAFT dt. May 18, 2004)

Requirements:

1. Leading Edge Comparator for RPC
2. Single/Multiple channel (pref. 16 channels)
3. Serial/Parallel out  
4. Clocked/Non clocked  

Important design issues:

Foundry  
(pref. SCL, Chandigarh)
Technology  
(pref. 1.2µm CMOS)
Input offset  
Necessary for setting gain of the comparator

Propagation delay (max.)  
The time difference the input $v^+$ crossing the ref. voltage $v^-$ and the output changing state

Hysteresis  Yes/No  
Necessary for slow varying signals and for noisy environment

Power consumption (max.)  
Supply voltage  
(typical ±2.5 for 1.2µm CMOS)
Slew rate (min.)  
When the clock enables the system the comparator functions as usual and when the clock disables the system the comparator stops comparing and remains latched to the previous state.

Topology  
1. Open loop comparators (uncompensated OPAMPs) – faster
2. Regenerative comparators (uses +ve feedback) – lesser propagation delay and higher sensitivity.
Basic voltage comparator schematic:

- **The preamplifier**
  The preamplifier increases the input sensitivity and isolates the input side from the switching noise originating from the +ve feedback stage.

- **Positive feedback stage (decision making circuit)**
  This stage is used to determine which of the input signals is larger.

- **Output buffer**
  The output buffer amplifies the information and outputs a corresponding digital signal.

Model of a comparator:

Zero order transfer curve (ideal comparator)  
First order transfer curve with offset (practical comparator)