DISCUSSION MEETING ONrical Electronics

SINP, Kolkata  April 29-30, 2011
ICAL detector and construction

Magnet coils

RPC handling trolleys

Total weight: 50Ktons

4000mm × 2000mm × 56mm low carbon iron sheets
RPC in the ICAL detector

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### Factsheet of ICAL detector

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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<tbody>
<tr>
<td>No. of modules</td>
<td>3</td>
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<tr>
<td>Module dimensions</td>
<td>$16m \times 16m \times 14.5m$</td>
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<tr>
<td>Detector dimensions</td>
<td>$48.4m \times 16m \times 14.5m$</td>
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<tr>
<td>No. of layers</td>
<td>150</td>
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<tr>
<td>Iron plate thickness</td>
<td>56mm</td>
</tr>
<tr>
<td>Gap for RPC trays</td>
<td>40mm</td>
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<tr>
<td>Magnetic field</td>
<td>1.3Tesla</td>
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<tr>
<td>RPC dimensions</td>
<td>$1,950mm \times 1,840mm \times 26mm$</td>
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<tr>
<td>Readout strip pitch</td>
<td>30mm</td>
</tr>
<tr>
<td>No. of RPCs/Road/Layer</td>
<td>8</td>
</tr>
<tr>
<td>No. of Roads/Layer/Module</td>
<td>8</td>
</tr>
<tr>
<td>No. of RPC units/Layer</td>
<td>192</td>
</tr>
<tr>
<td>No. of RPC units</td>
<td>$28,800 \ (97,505m^2)$</td>
</tr>
<tr>
<td>No. of readout strips</td>
<td>3,686,400</td>
</tr>
</tbody>
</table>

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Glass (bakelite) for electrodes
Special paint mixture for semi-resistive coating
Plastic honeycomb laminations as pick-up panel
Special plastic films for insulation
Avalanche (streamer) mode of operation
Gas: R134a+Iso-butane+SF₆ = 95.5+4.2+0.3 (R134a+Iso-butane+Argon=56+7+37)
Terminations on the non-readout end

Machined pickup strips on honeycomb panel

Preamp connections on the readout end
Post amplifier RPC pulse profile
Information to record on trigger

- Strip hit (1-bit resolution)
- Timing (200ps LC)
- Time Over Threshold (used for time-walk correction)
  - TDC can measure TOT as well.
- Pulse profile (using waveform sampler, 200ps LC)

Rates

- Individual strip background rates on surface ~300Hz
  - Underground rates differ: depth, rock radiation etc.
- Muon event rate ~10Hz (The ‘blue’ book says ~2Hz)

On-line monitor

- RPC parameters (High voltage, current)
- Ambient parameters (T, P, RH)
- D.C. power supplies, thresholds
- Gas systems and magnet control and monitoring
Expected data sizes and rates

- Strip hit - 128bits
- TDC: 16 channels (8 strips ORed), dual edges, 16 hits /ch, 16-bits - 16 x 2 x 8 x 16 = 4096bits
- **Pulse profile:** 16 channels, 50ns, 200ps LC, 8bits - 16 x 50 x 5 x 8 = 32kbits!
- RPC id - 16bits
- Event id - 32bits
- **Time stamp** - 100bits!
- Event size - 4272bits (excl. pulse profile + time stamp)
  - Assuming trigger rate to be 10Hz, event data rate = 42720bits/s
- Ambient sensors (TPH) - 3 x 16 = 48bits/s
- Noise rate data (1 second, 16 channels, 32bits) - 512bits/s
- Estimated data rate/RPC = 42720bits/s + 48bits/s + 512bits/s = 43280bits/s
- Add formatters, headers etc. - 50kbits/s/RPC
- Add data from at least 8 RPCs = 8 x 50kbits/s = 400kbits/s
- No data compression or zero suppression considered.
- Channel occupancy a few%
- **Pulse height analyser** - do we need it? Difficult to implement as online monitor routine

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8, LVDS pairs of unshaped comparator signals (I)

1, amplified & multiplexed RPC pulse on 50Ω (I)

3-bit channel address bus for multiplexer (O)

Power supplies (O)

Threshold control (d.c. or DAC bus) (O)
Amp_out

Common threshold

Ch-0

Regulated Cascode Transimpedance Amplifier

Differential Amplifier

Comparator

LVDS output driver

LVDS_out0

Channel-0

8:1 Analog Multiplexer

Output Buffer

LVDS_out7

Ch-7

Regulated Cascode Transimpedance Amplifier

Differential Amplifier

Comparator

LVDS output driver

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Features of ICAL FE ASIC

- IC Service: Europractice (MPW), Belgium
- Service agent: IMEC, Belgium
- Foundry: austriamicrosystems
- Process: AMSc35b4c3 (0.35μm CMOS)
- Input dynamic range: 18fC – 1.36pC
- Input impedance: 45Ω @350MHz
- Amplifier gain: 8mV/μA
- 3-dB Bandwidth: 274MHz
- Rise time: 1.2ns
- Comparator’s sensitivity: 2mV
- LVDS drive: 4mA
- Power per channel: < 20mW
- Package: CLCC48(48-pin)
- Chip area: 13mm²
FE ASIC evaluation board

ANUSPARSH TEST BOARD

10mv, Tr= 10ns, C+100pf ~ 100uA
VSS1 = Analog Ground
VSS = Analog Ground
DGND = DigitalGround
Separate chips for amplifier and discriminator?

Helps better to support FE for glass and bakelite versions of RPC

Also helps trying out for example, different designs for comparator. For example: CFD

Does not matter much for the FE board – it is matter of one versus two ASIC chips onboard.

Alternative: Amplifier bypass option in the current ASIC (amp+comp) chip.

Can we have analog sum of eight channels, in addition to multiplexing?
Scheme of RPC-DAQ controller

- **LM1117**: 3V3, 800mA
- **LM1117**: 5V, 800mA
- **NTA0505**: +5V & -5V, 100mA each

9V_Dc

**SPL_1**
- SCLK
- MOSI
- MISO
- CS

**SPL_2**
- SCLK
- MOSI
- MISO
- CS

**SPL_3**
- SCLK
- MOSI
- MISO
- CS

**MSP430F5438**
- Microcontroller
- 3V3

**USCI_A0**
- SCLK
- MOSI
- MISO
- CS

**USCI_A1**
- SCLK
- MOSI
- MISO
- CS

**USCI_A2**
- SCLK
- MOSI
- MISO
- CS

**ADC_12**
- A0
- A1
- A2
- Vref

**Level Shifter**
- SN10EPT28LZG
- 3V3

**Pressure**
- SMD085
- 5V

**R.Humidity**
- HIH4030
- 5V

**Temperature**
- AD8230
- +5V & -5V
- AD8629
- 5V

**Optical 1x9 Transceiver**
- 3V3

**TX+, TX-**

**RX+, RX-**

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Block diagram of MSP430F5xx
Serial Peripheral Interface (SPI)

- **Slave Data Input**: MOSI
- **Slave Data Output**: MISO
- **Chip Select Input**: SS
- **Master Clock Input**: SCK

Daisy chaining

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"Time stretcher" GHz → MHz

Inverter “Domino” ring chain (SCA)

Waveform stored

Shift Register

0.2-2 ns

IN

Out

Clock

Also ANUSMRITI ASIC: 500MHz Transient Waveform Sampler
V.B.Chandratre et al (BARC)
ASIC (3-stage interpolation technique)
- The new approach is to mix and match ASIC+FPGA techniques/architectures

FPGA (Vernier technique)

FPGA (Differential delay line technique)
- The FPGA efforts will continue
- Some issues (delay matching, routing etc.) to be solved

Good and bad of an FPGA solution

FPGA is a lesser travelled path (only used in CKM experiment, Fermilab)
Back-end issues

- VME is the ICAL’s backend standard
- Global services (trigger, clock etc.), calibration
- Data collector modules
- Computer and data archival
- On-line DAQ software
- On-line data quality monitors
- Networking and security issues
- Remote access protocols to detector sub-systems and data
- Voice and video communications
VME Interface Logic

Address Decoder

Data Router

Interrupt Gen And Handler

FPGA

LVDS I/O

Front Panel Out

Front Panel In

Piggy Board ID

Piggy Board Data

256 Deep FIFO

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Custom VME Module

- VME Interface Logic (FPGA)
- JTAG
- FPGA Configuration Logic

Connections:
- VME Data Transceiver
- VME Addr Transceiver
- Address Bus Transceiver
- Data Bus Transceiver
- VME Control Signals Buffer
- AM, DS, WR, SYSRST, IACK Buffer
- DATCK, IACKOUT, IRQs, BERR Buffer

Ports:
- On board logic analyser port
- LVDS Tx OUT
- LVDS Rx IN
- Front panel LEDs
- Interface for V1495s piggy boards
- Board Address

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Features of ICAL trigger system

- *Insitu* trigger generation
- Autonomous; shares data bus with readout system
- Distributed architecture
- For ICAL, trigger system is based only on topology of the event; no other measurement data is used
- Huge bank of combinatorial circuits
- Programmability is the game, FPGAs, ASICs are the players
1-Fold : $T_{11} = T_{01} + T_{02} + \ldots + T_{0L-1} + T_{0L}$
2-Fold : $T_{12} = T_{01}.T_{02} + T_{02}.T_{03} + \ldots + T_{0L-1}.T_{0L} + T_{0L}.T_{01}$
3-Fold : $T_{13} = T_{01}.T_{02}.T_{03} + T_{02}.T_{03}.T_{04} + \ldots + T_{0L-1}.T_{0L}.T_{01} + T_{0L}.T_{01}.T_{02}$
4-Fold : $T_{14} = T_{01}.T_{02}.T_{03}.T_{04} + T_{02}.T_{03}.T_{04}.T_{05} + \ldots + T_{0L-1}.T_{0L}.T_{01}.T_{02} + T_{0L}.T_{01}.T_{02}.T_{03}$
Segmentation of ICAL
## Proposed trigger scheme - 2

### Table

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<tr>
<th>Hspread</th>
<th>Vspread</th>
<th>Segment Size</th>
<th>Segment Type</th>
<th>T2S1_{&lt;a/3} Rate (Hz)</th>
<th>T2S2_{&lt;a/3} Rate (Hz)</th>
<th>T2S3_{&lt;a/3} Rate (Hz)</th>
<th>T2S4_{&lt;a/3} Rate (Hz)</th>
<th>T3S Rate (Hz)</th>
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<td>1.20x10^{-12}</td>
<td>7.61x10^{-13}</td>
<td>2.35x10^{-15}</td>
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<td></td>
<td></td>
<td>B</td>
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<td>2.28x10^{-15}</td>
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<td>3.90x10^{-15}</td>
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<td></td>
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<td>1.94x10^{-3}</td>
<td>3.07x10^{-15}</td>
<td>2.37x10^{-16}</td>
<td>1.94x10^{-5}</td>
</tr>
</tbody>
</table>
High voltage for RPCs
- **Voltage**: 10kV (nominal for Glass, less for Bakelite)
- **Current**: 15mA (approx., 500nA per chamber)
- **Ramp up/down, on/off, monitoring**

Low voltage for electronics
- **Voltages and current budgets still not available**

Commercial and/or semi-commercial solutions
- **Buy supplies, design distribution( and control)?**

DC-DC and DC-HVDC converters; cost considerations
DC-HVDC converters

1. E101CT, lowest cost
   - Input = +15VDC
   - Dual output is +5KV / -5KV (with a full load)
   - Output current = 0.2mA
   - Outputs are not separately controlled, but will track each other.

2. G50 [x 2units], low cost, separate control
   - Input = +12VDC
   - Output is 5KV, positive or negative (with a full load)
   - Output current is 0.3mA
   - Two units would be configured for a positive and negative output pair.
   - Units can be controlled separately.

3. Custom solution, Q101 with a centre tap, miniature package
   - Input = +5VDC (can be 12VDC)
   - Dual output is +5KV / -5KV (with a full load)
   - Output current = 50uA
   - Outputs are not separately controlled, but will track each other.
   - Note: This is a custom solution

4. Q60-5, Q60N-5, 2 units together, miniature package, separate control
   - Input = +5VDC
   - Output is +6KV / -6KV (with a full load)
   - Output current is 0.1mA
   - Two units would be configured for a positive and negative output pair.
   - Units can be controlled separately.

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Cables and interconnects

- RPC to front-end boards – the toughest!
  - Integration with pickup panel fabrication
- Front-end boards to RPC-DAQ board
  - LVDS signals (any alternatives?, prefer differential)
  - Channel address
  - Multiplexed analog pulse
  - Power supplies
- RPC-DAQ boards to trigger segment stations
  - Four pairs, Copper, multi-line, flat cable?
- RPC-DAQ boards to back-end
  - Master trigger
  - Central clock
  - Data cable (Ethernet: copper/fibre, …)
Other critical issues

- **Power requirement and thermal management**
  - If 50mW/channel → 200KW/detector
  - Front-end positioning; use absorber to good use!
  - Do we need forced, water cooled ventilation?
  - UPS, generator power requirements
    - High voltage supplies, critical controls, computers on UPS

- **Suggested cavern conditions**
  - Temperature: 20±2°C
  - Relative humidity: 50±5%
Roll of electronics industries

- Chip fabrication
- Board design, fabrication, assembly and testing
- Cabling and interconnects
- Crates and mechanics
- Slow control and monitoring
  - Control and monitoring systems for gas systems and magnet
- Industries (both public and private) are looking forward to work with INO
Software components

- RPC-DAQ controller firmware
- Backend online DAQ system
- Local and remote shift consoles
- Data packing and archival
- Event and monitor display panels
- Event data quality monitors
- Slow control and monitor consoles
- Database standards
- Plotting and analysis software standards
- OS and development platforms
Can be tested today on the RPC stacks
Front-end board with the current board’s form-factor, but using ASICs
RPC-DAQ board with:
- TDC
- Waveform sampler
- Strip-hit latch and rate monitor
- Controller + data transreceiver
- Firmware for the above
- Pre-trigger front-end
- TPH monitoring
- Pulse width monitoring
- Front-end control
- Signal buffering scheme
- and GP area or ports for accommodating new blocks
VME data concentrator module
Result: Complete readout chain is tested
Can we use this for RPC QC test stands or what?
Work packages – Part 1

- Developing thin signal pickup panels
- RPC to front-end interconnect scheme
- Front-end
  - ASIC (including two separate ASICs’ option), freeze design
  - Board design
- RPC-DAQ module design (+ signal routing/buffering)
  - TDC chip, freeze design
  - Waveform sampler chip, freeze design
  - Strip-hit latch and rate monitor (similar to prototype’s design)
  - Pre-trigger front-end (similar to prototype’s design)
  - Controller + data transreceiver (including firmware development)
  - TPH monitoring section (done?)
  - Front-end control scheme (threshold, test inputs)

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Work packages – Part 2

- Trigger system
  - Validation of the scheme
  - Segment trigger station design (do we need a crate?)
  - Locating segment trigger stations and routing of pre-trigger lines
  - Locating backend trigger station, trigger fan-out and routing
  - Global clock? Depends on TDC scheme

- DAQ backend
  - VME data concentrator module (Readout for 64 RPCs?)
  - VME crate controller
  - Location of backend VME crates, crates production
  - On R&D track: Alternate backend standard PCI/PCIe etc?

- Proof of principle effort
Work packages – Part 3

- **DAQ software**
  - Databases
  - Standardising OS, development tools, graphical tools
  - Data acquisition, packaging, archival, event display, DQMs, monitor controls, user interfaces etc.

- **Power supplies**
  - Low Voltage
  - High Voltage (commercial, DC-HVDC, semi-commercial)
  - Power supplies’ mains and distribution
  - Routing of LV, HV lines to the RPC
  - Routing of LV, HV on the magnet

- **Power requirement and thermal management**
  - Simulations of heat dissipation
  - Ventilation methods
Work packages – Part 4

- Integration issues
  - Mounting of front-ends and RPC-DAQ module on the RPC unit
  - Alternate schemes

- Production jobs
  - Boards and modules design
  - Production, programming and calibration
  - Cabling and connectorisation etc. (specifications decided by the collaboration)
  - Crates, racks and other mechanics

- Installation and commissioning

- Operation and long-term continuity considerations
Thanks

- Prof. Satyajit Saha & Dr. Subhasis Chattopadhyay for all the local arrangements despite prevailing election season
- Dr. Deepak Samuel for designing the meeting’s web page
- Prof. N.K. Mondal for approving all the expenses
- MOM writers, Deepak and Mandar Saraf
- All of you who could make it despite disruption of AI services